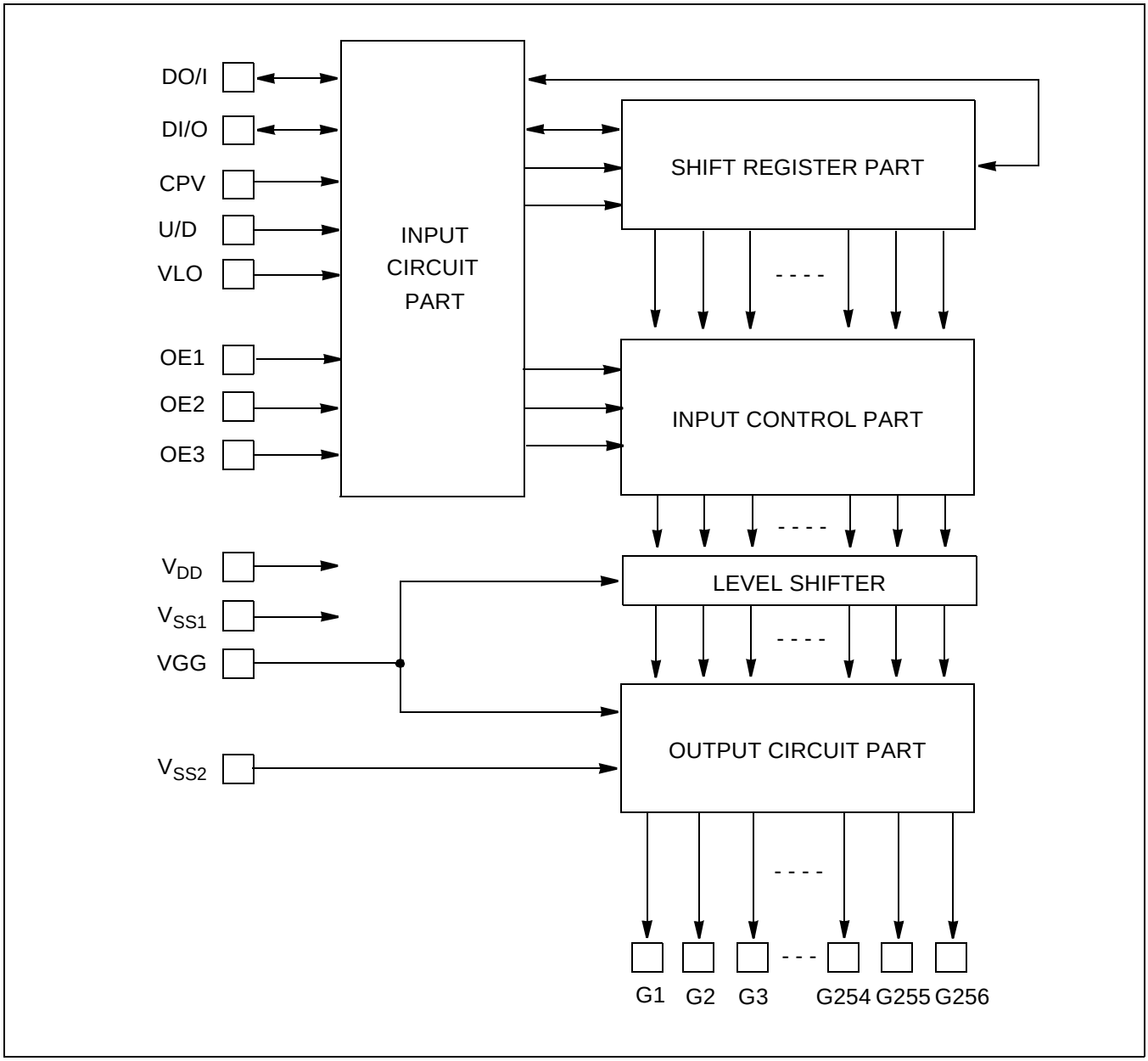
INTRODUCTION

The KS0647 is a TFT LCD gate driver, which can drive 256 output pins.
The maximum range of driving voltage is 40 V.

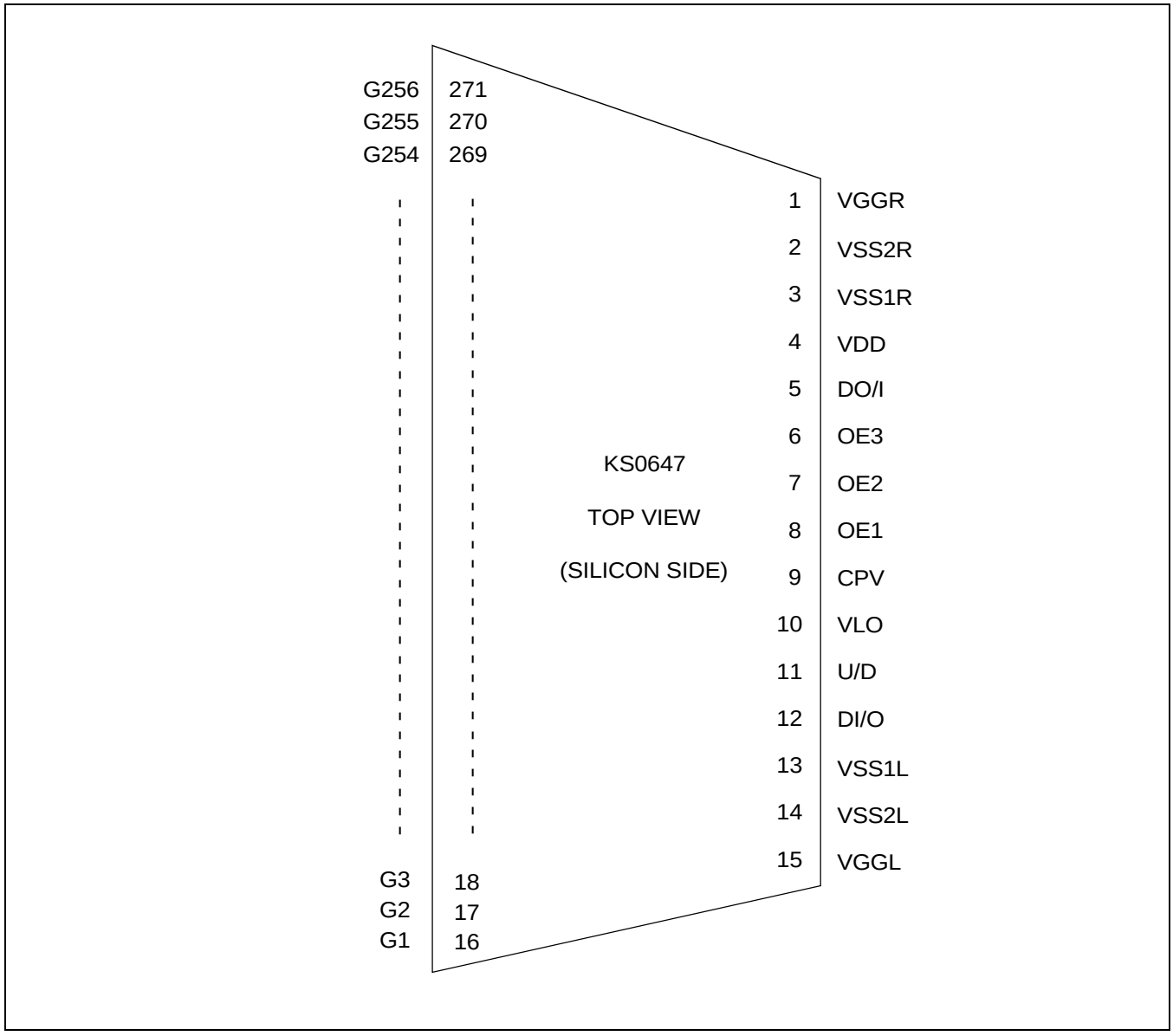
FEATURES

- ❑ Gate driver for TFT LCD
- ❑ 256 outputs
- ❑ High voltage drive: V_{SS2} + 40V (MAX.), if $V_{SS1} = V_{SS2}$
- ❑ Data transfer method: Bidirectional shift register
- ❑ Source voltage (V_{DD}-VLO): 3.0 to 5.5V
- ❑ Tape Carrier Package (TCP)

BLOCK DIAGRAM



TCP PIN CONFIGURATION



NOTE: Input pin arrangement in TCP can be modified (If the customer wants)

PIN DESCRIPTION

<table>
<tr><th>Pin Symbol</th><th>Pin Name</th><th>Description</th></tr>
<tr><td>V_{DD}</td><td>Power supply</td><td>Voltage source for internal logic operation</td></tr>
<tr><td>V_{SS}1R/L</td><td>Power supply</td><td>Voltage source for internal logic operation and LCD panel control</td></tr>
<tr><td>VGGR/L</td><td>Power supply</td><td>Voltage source for LCD panel control (plus)</td></tr>
<tr><td>VLO</td><td>Power supply</td><td>Source voltage of logic input low level</td></tr>
<tr><td>G1 to G256</td><td>Driver output</td><td>LCD panel drive output pin.
Output drive voltage is VGG or VSS2 for driving TFT LCD panel, depending on the data of shift register or the state of OE1 to 3.</td></tr>
<tr><td>V_{SS2}R/L</td><td>Analog input
(TFT gate off level)</td><td>When the data of the shift register is “L”, output drive voltage is V_{SS2}. When OE1 to 3 is “H”, output drive voltage is V_{SS2} apart from the data of the shift register.
V_{SS2} is the same power as V_{SS1}.</td></tr>
<tr><td>DI/O

DO/I</td><td>Vertical shift data input/output</td><td>Depending on the state of U/D, The functions of these two pins are determined as follows:
<table>
<tr><th>U/D</th><th>DI/O</th><th>DO/I</th></tr>
<tr><td>“H” (V_{DD})
“L” (V_{SS1} to VLO)</td><td>Input
Output</td><td>Output
Input</td></tr>
</table>
Input: Input data which is transferred to these pins is stored in the first shift register at the rising edge of CPV.
Output: Output data which is changing at the falling edge of CPV is transferred to the input pin of the next IC, which is cascaded.</td></tr>
<tr><td>U/D</td><td>Select pin of the shift data direction</td><td>Data in the shift register is synchronized with the rising edge of CPV and is transferred to the next register as follows:
<table>
<tr><th>U/D</th><th>Shift direction</th></tr>
<tr><td>“H” (V_{DD})
“L” (V_{SS1} to VLO)</td><td>G1 → G2 → G3 → G4..... → G256
G256 → G255 → G254 →..... → G1</td></tr>
</table>
This pin is recommended to fix the DC level</td></tr>
<tr><td>CPV</td><td>Clock input</td><td>Vertical shift clock of shift register</td></tr>
<tr><td>OE1 to 3</td><td>Output enable pin</td><td>These pins control the state of output drive pins (G1 to G256).
OE1 to 3 = “L”: Output level is VGG or V_{SS2} corresponding to the data.
OE1 to 3 = “H”: Output level is V_{SS2}</td></tr>
</table>

OPERATION DESCRIPTION

OPERATION METHOD

The input shift data (DI) of DI/O (When U/D is “H”) or DO/I (When U/D is “L”) is synchronized with the rising edge of CPV and stored in the first shift register.
While stored data is transferred to the next register at the next rising edge of CPV, new data of DI (Input shift data) is stored simultaneously.
The output pin (G1 to G256) supplies VGG voltage or V_{SS2} voltage to the TFT LCD panel depending on the data of the shift register.
The output shift data (DO) of DO/I (When U/D is “H”) or DI/O (When U/D is “L”) is synchronized with the falling edge of CPV, and DO of the last register (G1 or G256) is transferred to the next IC.
The output voltage level of DO is V_{DD} with “H” data, V_{SS1} with “L” data.

Mutual relationship of U/D and shift data I/O pin is as follows:

U/D pin	Shift data I/O		Data transfer direction
	Input	Output	
“H” (V_{DD})	DI/O	DO/I	G1 → G2 → G3 → G4 → G5 →..... → G256
“L” (V_{SS1} to VLO)	DO/I	DI/O	G256 → G255 → G254 → G253 →..... → G1

OUTPUT PIN (G1 TO G256)

If the data of the shift register to an output drive pin is “H”, VGG voltage is output.
Otherwise, V_{SS2} voltage is output.
But, when OE1 to 3 to an output drive pin is “H”, V_{SS2} voltage is output irrespective of the data of the shift register.

Condition		Control pin to LCD panel	
Pin	State	Output pin by OE signal	Output
OE1	“H”	G1,G4,G7, ... G250,G253,G256	V_{SS2}
OE2		G2,G5,G8, ... G251,G254	
OE3		G3,G6,G9, ... G252,G255	
OE1	“L”	G1,G4,G7, ... G250,G253,G256	Normal output (VGG/V_{SS2})
OE2		G2,G5,G8, ... G251,G254	
OE3		G3,G6,G9, ... G252,G255	

VOLTAGE BIAS

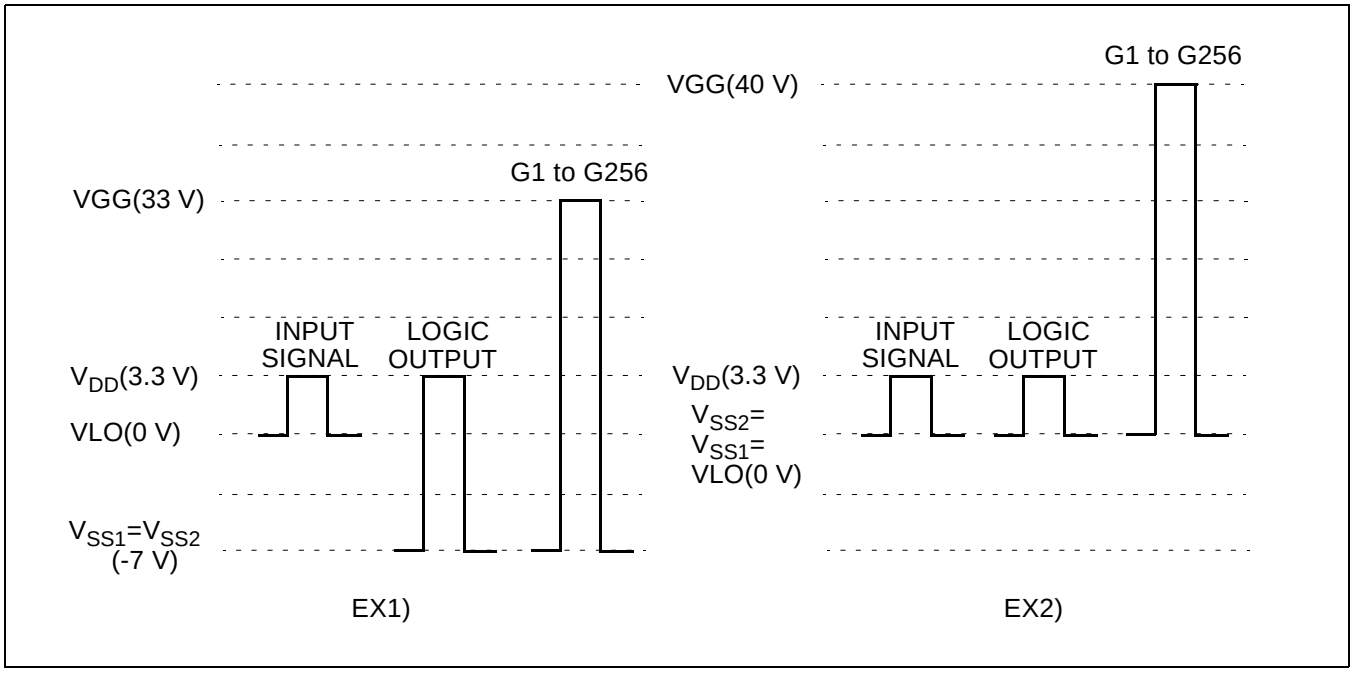
V_{SS2} which is the “L” level of the LCD output drive voltage, is the same power as V_{SS1}.

EX1) Negative output voltage mode
Logic input: Input switching level is from 0 V to V_{DD} (3.3V)
Power voltage:
VGG = 33V
V_{DD} = 3.3V
VLO = 0V
V_{SS2} = −7V
V_{SS1} = −7V

LCD output drive voltage:
“H” level = VGG (33V)
“L” level = V_{SS2} (-7V)

EX2) Positive output voltage mode
Logic input: Input switching level is from 0V to V_{DD} (3.3 V)
Power voltage:
VGG = 40V
V_{DD} = 3.3V
V_{SS2} = V_{SS1} = VLO = 0V

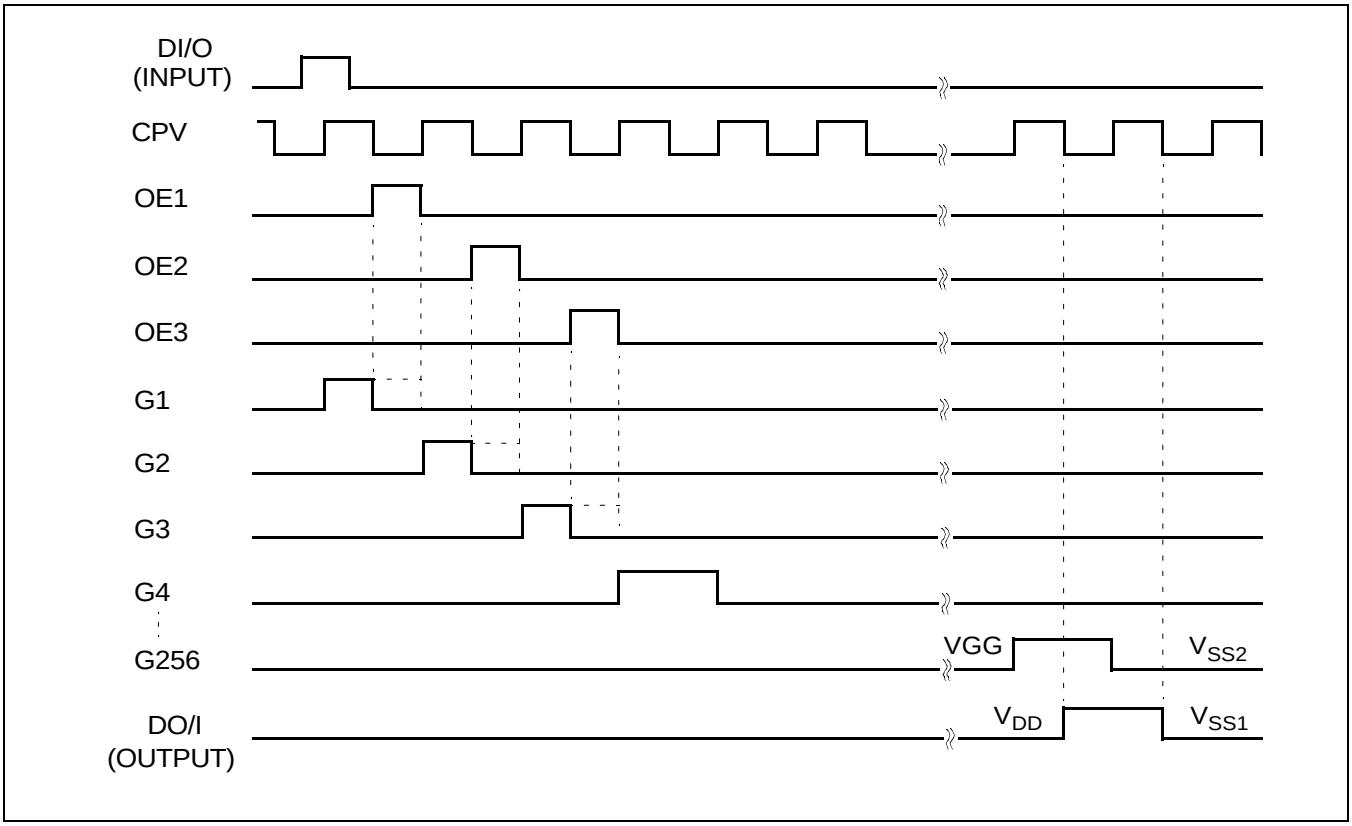
LCD output drive voltage:
“H” level = VGG (40V)
“L” level = V_{SS2} (0V)



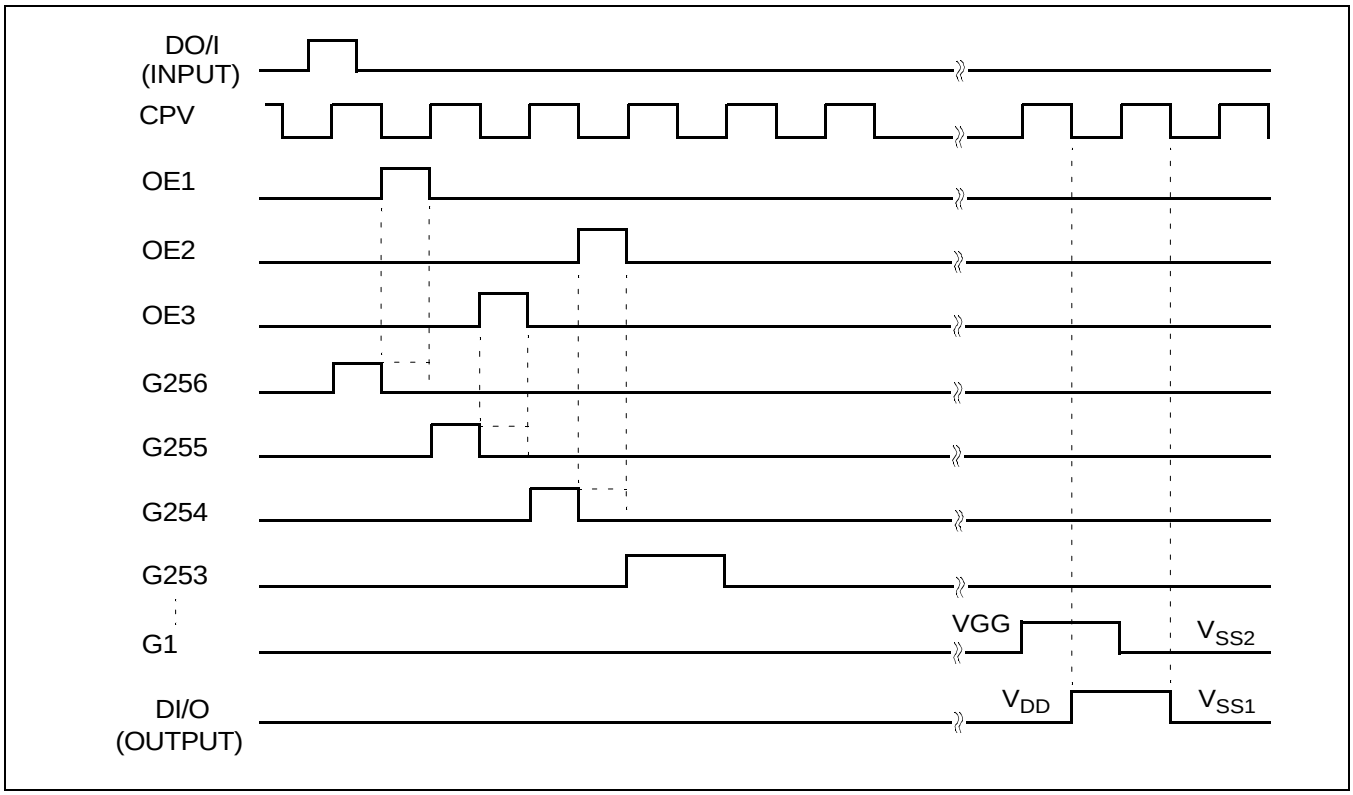
— Input signal (DI/O, DO/I, CPV, OE1 to 3) swings from VIL to VIH.

RECOMMENDED TIMING

UP MODE (When U/D = "H")



UP MODE (When U/D = “L”)



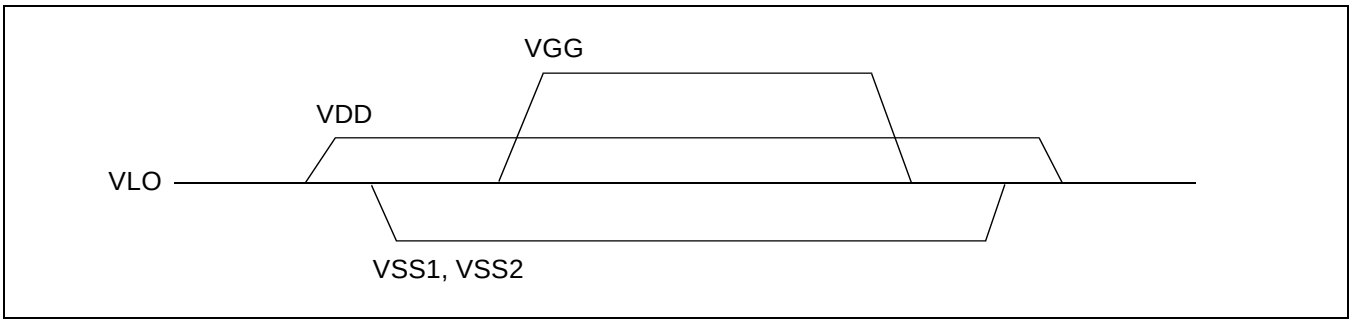
MAXIMUM ABSOLUTE LIMIT

(V_{SS1} = V_{SS2} = 0 V)

Characteristic	Symbol	Value	Unit	Application pin
Power supply voltage (1)	V_{GG}	–0.3 to 45.0	V	-
Power supply voltage (2)	V_{DD}	–0.3 to 21.0	V	-
Power supply voltage (3)	V_{LO}	–0.3 to VDD+0.3	V	-
Input voltage	V_{IN}	–0.3 to VDD+0.3	V	-
Operation temperature	T_{OPR}	–20 to 75	°C	-
Storage temperature	T_{STG}	–55 to 150	°C	-

Power ON/OFF sequence
Turn on power order: VLO → V_{DD} → V_{SS1}, V_{SS2} → control signal input → VGG
Turn off power order: VGG → control signal input → V_{SS1}, V_{SS2} → V_{DD} → VLO

If LSIs are used beyond the above maximum absolute limits, they may be permanently destroyed.



RECOMMENDED OPERATING RANGE

(V_{SS1} = V_{SS2} = 0 V)

Characteristic	Symbol	Value	Unit	Remark
Power supply voltage (1)	VGG	20.0 to 40.0	V	–
Power supply voltage (2)	V_{DD}	3.0 to 19.0	V	–
Power supply voltage (3)	VLO	V_{DD}-5.5 to V_{DD}-3.0	V	VLO ≥ V_{SS1}
Operation frequency	fCPV	DC to 100	kHz	–
Output load	CL	500 (MAX)	pF/PIN	–

DC CHARACTERISTICS

(Ta=-20 to +75°C, VGG-V_{SS1}=20 to 40 V, V_{DD}-V_{SS1}=3 to 19 V, V_{SS1}=V_{SS2}=0 V, V_{DD}-VLO=3.0 to 5.5 V)

Characteristic	Symbol	Condition	Value		Unit	Application pin
			Min.	Max.		
Low input voltage	VIL	*1	VSS1	VLO+0.1VX	V	*2
High input voltage	VIH		VLO+0.9VX	VDD	V	
Low output voltage	VOL	IOL = 40 µA	VSS1	VSS1+0.4	V	DI/O, DO/I *3
High output voltage	VOH	IOH = -40 µA	VDD-0.4	VDD	V	
Low output resistance	ROL	VOUT = 0.5 V VGG = 40 V VSS1=VSS2 = 0 V	–	500	Ω	G1 to G256
High output resistance	ROH	VOUT=VGG-0.5 V VGG = 40 V VSS1=VSS2 = 0 V	–	500	Ω	G1 to G256
Input leakage current	ILK	–	–5	5	µA	*2
Power supply current (1)	IGG	No output load	–	400	µA	VGG
Power supply current (2)	IDD	VDD-VSS1=3.3 V	–	400	µA	VDD *2, *4
		VDD-VSS1=19 V	–	1000		

NOTES:

1. VX = V_{DD} - VLO
2. DI/O, DO/I, CPV, OE1 to 3, U/D
3. When these pins are used as an output pin
4. Input swing voltage is V_{DD} to V_{DD}-3.3 V

AC CHARACTERISTICS

(Ta=-20 to +75°C, VGG-V_{SS1}=20 to 40 V, V_{DD}-V_{SS1}=3 to 19 V, V_{SS1}=V_{SS2}=0 V, V_{DD}-VLO=3.0 to 5.5 V)

Characteristic	Symbol	Condition	Value		Unit
			Min.	Max.	
Operation frequency	tCPV	–	10	–	µs
Clock pulse width	tCPVH, tCPVL	duty = 50%	4	–	
Output enable width	twOE	–	1	–	
Data setup time	tsDI	–	700	–	ns
Data hold time	thDI	–	700	–	
Output delay time (1)	tpdDO	CL=30 pF	–	800	
Output delay time (2)	tpdG	CL=300 pF	–	800	
Output delay time (3)	tpdOE	CL=300 pF	–	800	

AC TIMING DIAGRAM