INTRODUCTION

The KS0644 is a 384/402-channel output, TFT-LCD source driver for 256 gray scale displays.
Data input is a digital input consisting of 8 bits by 6 dots, and can display a full-color (16,700,000 colors) by output of 256 values γ-corrected.

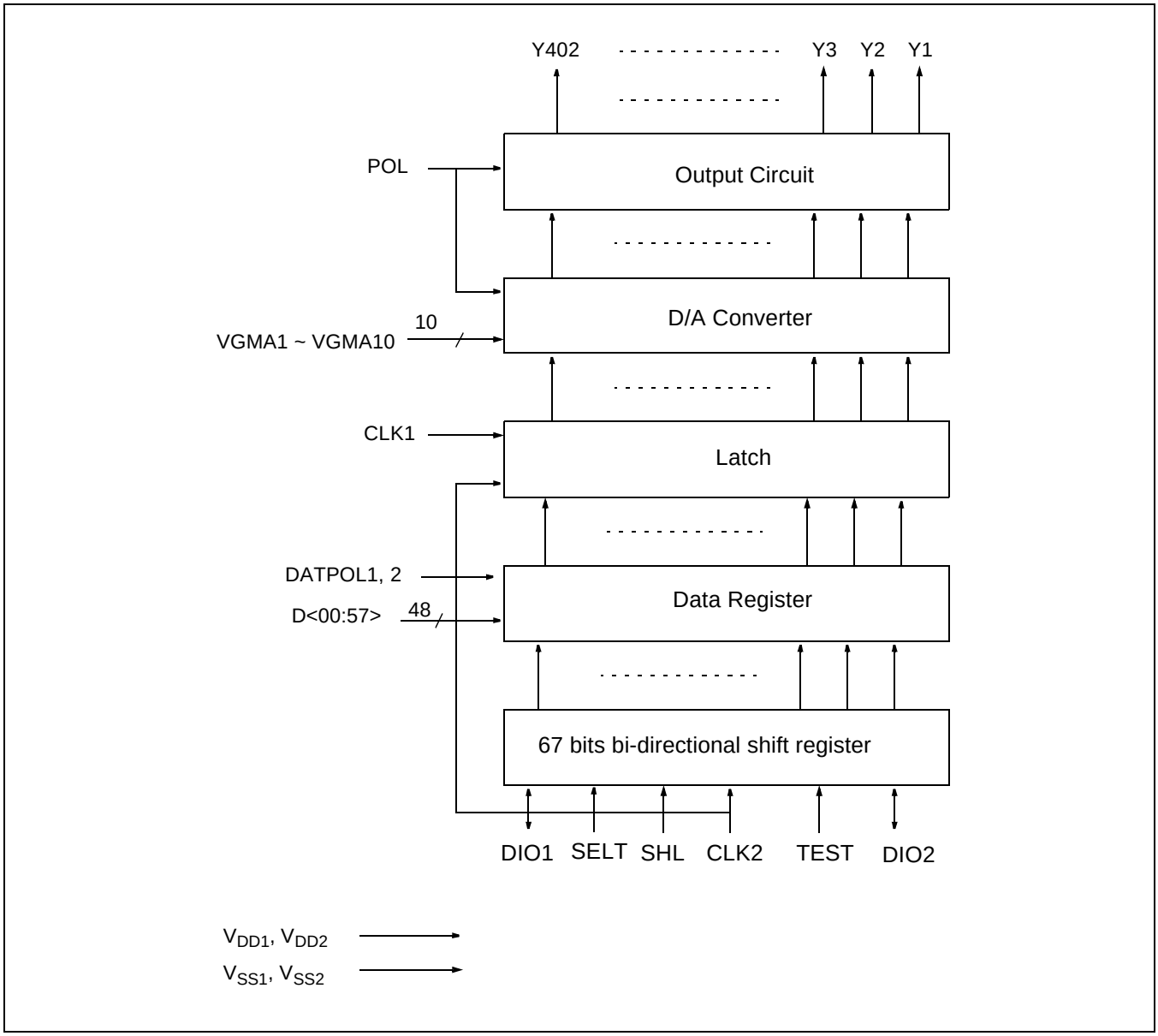
In this device each output has an internal D/A (digital-to-analog) converter which uses 10 (5×2) external power supplies. The output dynamic range is as large as 7.8 to 14.8 Vp-p, so it is unnecessary to operate level inversion of the LCD's common electrode.
It is able to deal with dot line inversion when mounted on a single side, and 256 gray scale voltages with different polarity can be output to the odd number output pins and even number output pins.

The KS0644 can be adjusted to larger panel, and SHL (Shift direction selection) pin makes use of the LCD panel connection convenient. Maximum operation clock frequency is 65MHz at a 2.5V logic operation and it can be applied to the TFT LCD panel of XGA to UXGA standards

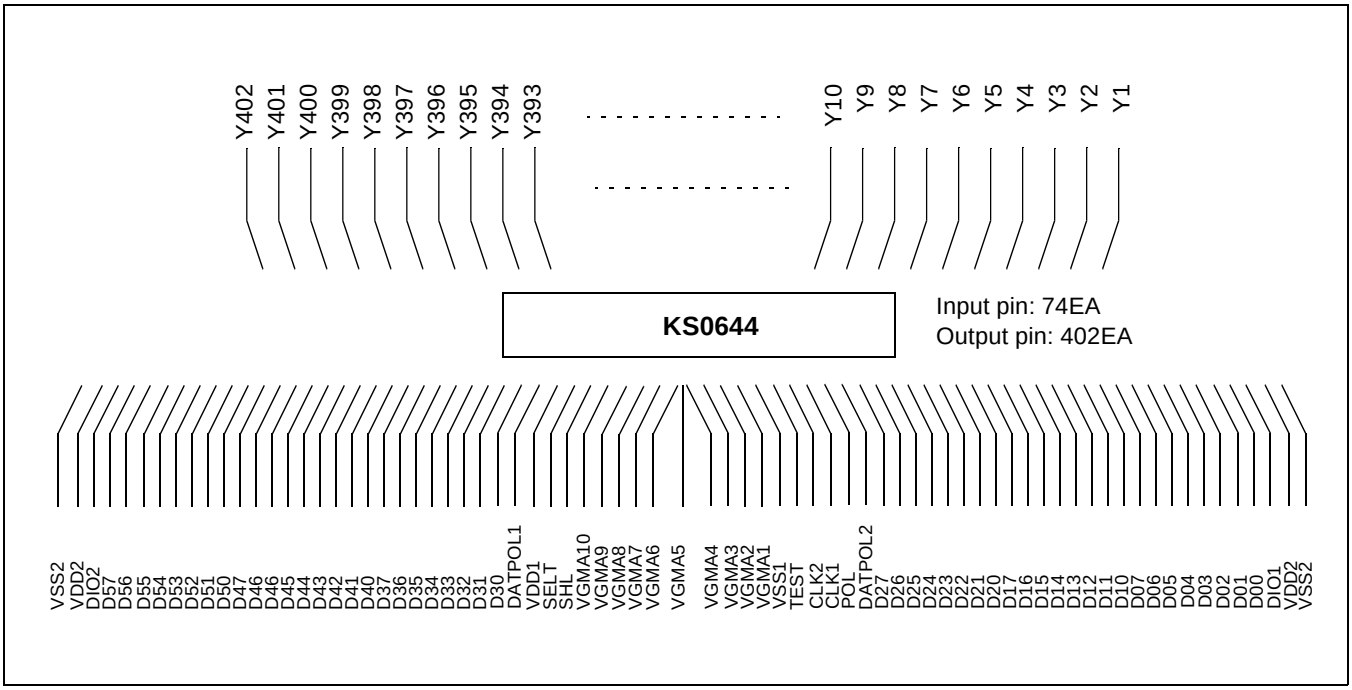
FEATURES

- ❑ TFT active matrix LCD source driver LSI
- ❑ 256 outputs are possible through 10 (5×2) external power supply and D/A converter
- ❑ Dot/Column inversion display is possible
- ❑ CMOS level input
- ❑ 8-bit (G/S data) $\times$ 6-dot (RGB) input
- ❑ Input data inversion function (DATPOL1, 2)
- ❑ Logic supply voltage: 2.5 to 3.6V
- ❑ LCD drive supply voltage: 8.0 to 15.0 Vp-p
- ❑ Output dynamic range: 7.8 to 14.8 Vp-p
- ❑ Maximum operation clock frequency :
  fmax = 65MHz (internal data transmission rate at 2.5V operation)
- ❑ Output: 384/402 outputs
- ❑ Slim TCP

BLOCK DIAGRAM



PIN CONFIGURATION



NOTES:

1. This figure does not specify the dimensions of the TCP package.
2. In actual panel application, the power should be supplied through all the V_{DD2} and V_{SS2} pins simultaneously.

PIN DESCRIPTION

Symbol	Name	Description
V_{DD1} V_{DD2}	Logic Power Driver Power	2.5V to 3.6V 8.0V to 15.0V
V_{SS1} V_{SS2}	Logic Ground Driver Ground	Ground (0V) Ground (0V)
Y1 to Y402	LCD Drive Output	The D/A Converted 256 G/S Analog Voltage Is Output
D0<7:0> ~ D5<7:0>	Data Input	The display data is input with a width of 48-bit, gray scale Data(8-bit) × 6dot (R, G, B) DX0: LSB, DX7:MSB
SHL	Data Shift Direction Control Input	This pin controls the direction of shift register in cascade connection. The shift direction of the shift register is as follows. SHL = H: DIO1 Input (Y1→ Y402), DIO2 Output SHL = L: DIO2 Input (Y402 → Y1), DIO1 Output
DIO1	Right Shift Start Pulse Input/Output	SHL = H: Used as the start pulse input pin SHL = L: Used as the start pulse output pin
DIO2	Left Shift Start Pulse Input/Output	SHL = H: Used as the start pulse output pin SHL = L: Used as the start pulse input pin
CLK2	Shift Clock Input	Refer to shift clock input of the shift register. The display data is loaded to the data register at the rising edge of CLK2.
CLK1	Latch input	CLK1 Latch input. Latches the data register contents as rising edge and transfers it to the D/A converter. Also, after CLK1 input, clears the internal shift register contents. After 1 pulse input on start, operates normally. CLK1 input timing refers to the “Relationship between CLK1 start pulse (DI01, DI02) and blanking period” of the switching characteristic waveform.
VGMA1 to VGMA10	γ-Corrected Reference Voltage Input	Input the γ–corrected power supplies from external source. V_{DD2}>VGMA1>VGMA2>VGMA3> ----- >VGMA9>VGMA10>V_{SS2} Keep gray scale power supply unchanged during the gray scale voltage output.
SELT	384/402 output selection input	SELT = L: 384 output (Y193 to Y210) are disabled) SELT = H: 402 output
DATPOL1, DATPOL2	Data inversion input	DATPOL1 = H: 24 data (D00 to D27) are inverted DATPOL2 = H: 24 data (D30 to D57) are inverted DATPOL1,2 = L: Display data is not inverted DATPOL1,2 are pull-down. (pd = 30kΩ)
POL	Polarity inverting input	When POL = L, The reference voltages for odd number outputs are VGMA1 to VGMA5 and those for even number outputs are VGMA6 to VGMA10. When POL = H, The reference voltages for odd number outputs are VGMA6 to VGMA10 and those for even number outputs are VGMA1 to VGMA5.
TEST	Test Pin	Lsi Test Pin Test=L : Normal Test=H : Test Mode → Op Amp Cut-Off

RELATIONSHIP BETWEEN THE INPUT DATA AND OUTPUT VOLTAGE

RELATIONSHIP # 1 BETWEEN INPUT DATA AND OUTPUT VOLTAGE

Output voltage is decided based on the input data and 10 (5×2) of **g** -corrected power supplies (VGMA1 to VGMA10). Besides, to be able to deal with dot line inversion when mounted on a single-side, gradation voltages with different polarity can be output to the odd number output pins and the even number output pins.
Among 5-by-2 **g**-corrected voltages, input gray scale voltages of the same polarity with respect to the common voltage, for the respective 5 **g**-corrected voltages of VGMA1 to VGMA5 and VGMA 6 to VGMA10.

data format: 1 PIXEL data (8 bits) × 2RGBs (6 dots)
Input width: 48 bits

- Details on display data

DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0
upper bits							lower bits

- Relationship between shift direction and output data

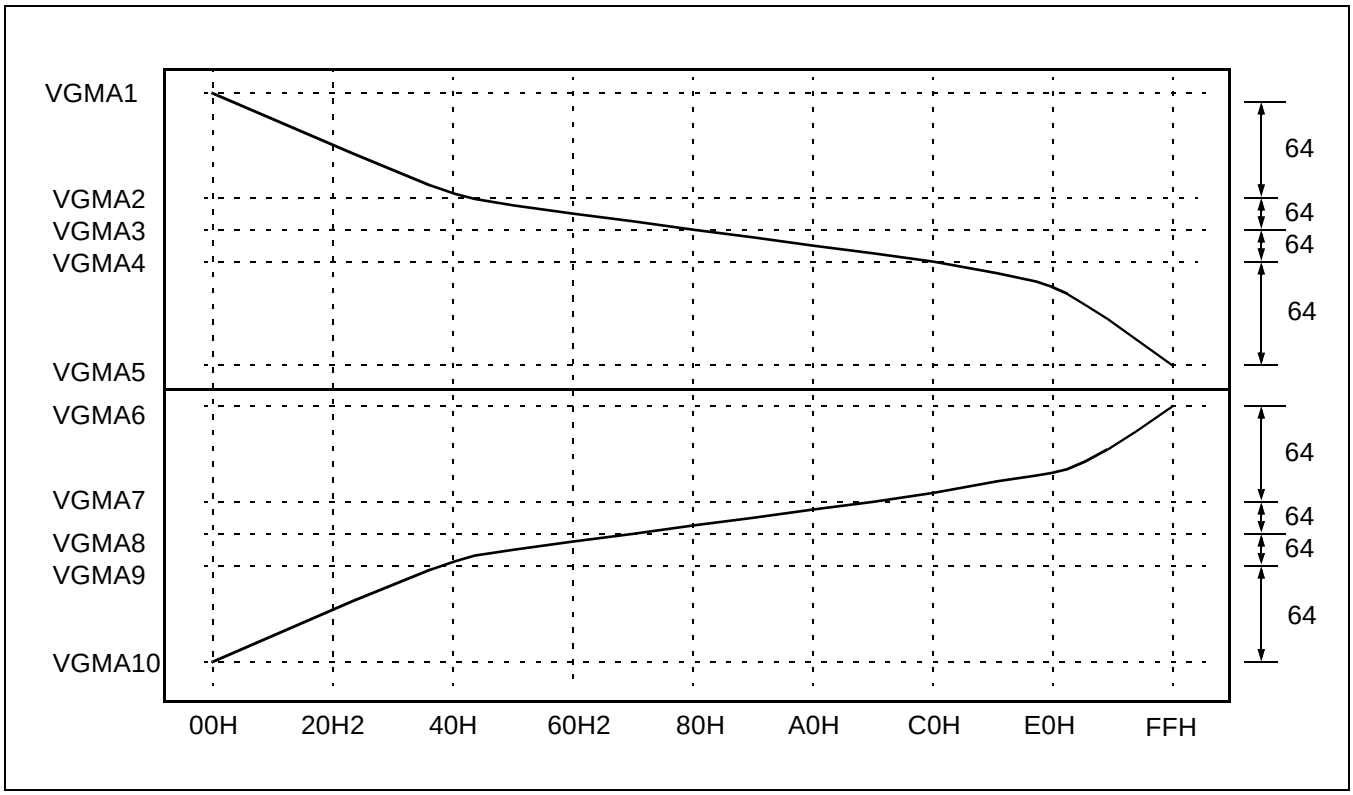
SHL = “H” (Right shift)

Output	Y1	Y2	Y3	…. ..	Y400	Y401	Y402
–	First			→	Last		
DATA	D00 to D05	D10 to D15	D20 to D25	…. ..	D30 to D35	D40 to D45	D50 to D57

SHL= “L” (Left shift)

Output	Y1	Y2	Y3	…. ..	Y400	Y401	Y402
–	Last			←	First		
DATA	D00 to D05	D10 to D15	D20 to D25	…. ..	D30 to D35	D40 to D45	D50 to D57

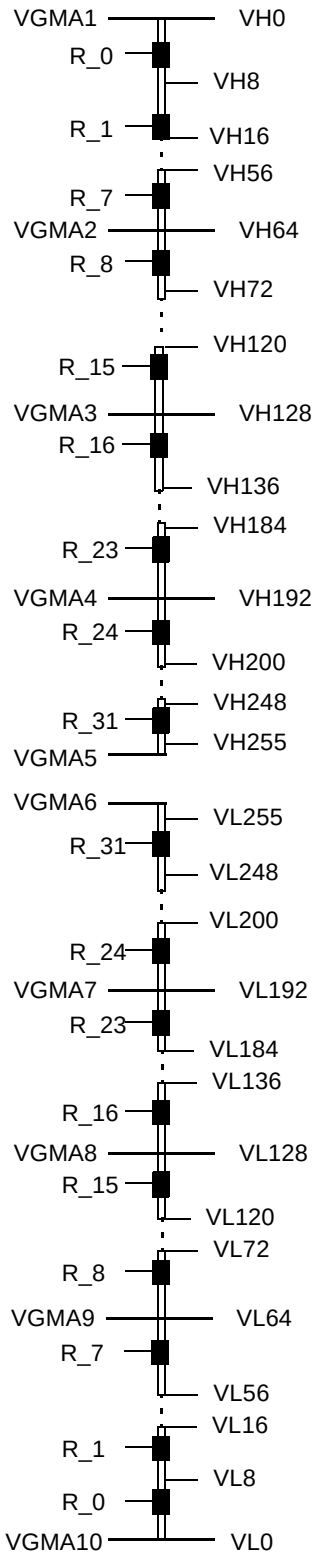
g - Correction Characteristic Curve



6-4 g-Corrected Power Circuit and Relationship Input Data and Output Voltage.

* Ladder Resistance Value (R0 to R255, Unit: W)

Name	Value	Name	Value	Name	Value	Name	Value
R0	80	R32	46	R64	32	R96	32
R1	80	R33	46	R65	32	R97	32
R2	80	R34	46	R66	32	R98	32
R3	80	R35	46	R67	32	R99	32
R4	80	R36	46	R68	32	R100	32
R5	80	R37	46	R69	32	R101	32
R6	80	R38	46	R70	32	R102	32
R7	80	R39	46	R71	32	R103	32
R8	68	R40	40	R72	32	R104	34
R9	68	R41	40	R73	32	R105	34
R10	68	R42	40	R74	32	R106	34
R11	68	R43	40	R75	32	R107	34
R12	68	R44	40	R76	32	R108	34
R13	68	R45	40	R77	32	R109	34
R14	68	R46	40	R78	32	R110	34
R15	68	R47	40	R79	32	R111	34
R16	60	R48	36	R80	32	R112	34
R17	60	R49	36	R81	32	R113	34
R18	60	R50	36	R82	32	R114	34
R19	60	R51	36	R83	32	R115	34
R20	60	R52	36	R84	32	R116	34
R21	60	R53	36	R85	32	R117	34
R22	60	R54	36	R86	32	R118	34
R23	60	R55	36	R87	32	R119	34
R24	52	R56	34	R88	32	R120	36
R25	52	R57	34	R89	32	R121	36
R26	52	R58	34	R90	32	R122	36
R27	52	R59	34	R91	32	R123	36
R28	52	R60	34	R92	32	R124	36
R29	52	R61	34	R93	32	R125	36
R30	52	R62	34	R94	32	R126	36
R31	52	R63	34	R95	32	R127	36



Name	Value	Name	Value	Name	Value	Name	Value
R128	36	R160	44	R192	56	R224	86
R129	36	R161	44	R193	56	R225	86
R130	36	R162	44	R194	56	R226	86
R131	36	R163	44	R195	56	R227	86
R132	36	R164	44	R196	56	R228	86
R133	36	R165	44	R197	56	R229	86
R134	36	R166	44	R198	56	R230	86
R135	36	R167	44	R199	56	R231	86
R136	38	R168	48	R200	64	R232	94
R137	38	R169	48	R201	64	R233	94
R138	38	R170	48	R202	64	R234	94
R139	38	R171	48	R203	64	R235	94
R140	38	R172	48	R204	64	R236	94
R141	38	R173	48	R205	64	R237	94
R142	38	R174	48	R206	64	R238	94
R143	38	R175	48	R207	64	R239	94
R144	40	R176	48	R208	72	R240	118
R145	40	R177	48	R209	72	R241	118
R146	40	R178	48	R210	72	R242	118
R147	40	R179	48	R211	72	R243	118
R148	40	R180	48	R212	72	R244	118
R149	40	R181	48	R213	72	R245	118
R150	40	R182	48	R214	72	R246	118
R151	40	R183	48	R215	72	R247	118
R152	42	R184	52	R216	80	R248	230
R153	42	R185	52	R217	80	R249	230
R154	42	R186	52	R218	80	R250	230
R155	42	R187	52	R219	80	R251	230
R156	42	R188	52	R220	80	R252	230
R157	42	R189	52	R221	80	R253	230
R158	42	R190	52	R222	80	R254	230
R159	42	R191	52	R223	80	R255	540

Name	Value
R_0	640
R_1	544
R_2	480
R_3	416
R_4	368
R_5	320
R_6	288
R_7	272
R_8	256
R_9	256
R_10	256
R_11	256
R_12	256
R_13	272
R_14	272
R_15	288
R_16	288
R_17	304
R_18	320
R_19	336
R_20	352
R_21	384
R_22	384
R_23	416
R_24	448
R_25	512
R_26	576
R_27	640
R_28	688
R_29	752
R_30	944
R_31	2150

RELATIONSHIP #2 BETWEEN INPUT DATA AND OUTPUT VOLTAGE (1)

Input Data	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	Output Voltage	
00H	0	0	0	0	0	0	0	0	V0	VGMA1
01H	0	0	0	0	0	0	0	1	V1	VGMA1+(VGMA2-VGMA1)(80 × 1)/3328
02H	0	0	0	0	0	0	1	0	V2	VGMA1+(VGMA2-VGMA1)(80 × 2)/3328
08H	0	0	0	0	1	0	0	0	V8	VGMA1+(VGMA2-VGMA1)(80 × 8)/3328
09H	0	0	0	0	1	0	0	1	V9	VGMA1+(VGMA2-VGMA1)(640+68 × 1)/3328
10H	0	0	0	1	0	0	0	0	V16	VGMA1+(VGMA2-VGMA1)(640+68 × 8)/3328
11H	0	0	0	1	0	0	0	1	V17	VGMA1+(VGMA2-VGMA1)(1184+60 × 1)/3328
18H	0	0	0	1	1	0	0	0	V24	VGMA1+(VGMA2-VGMA1)(1184+60 × 8)/3328
19H	0	0	0	1	1	0	0	1	V25	VGMA1+(VGMA2-VGMA1)(1664+52 × 1)/3328
20H	0	0	1	0	0	0	0	0	V32	VGMA1+(VGMA2-VGMA1)(1664+52 × 8)/3328
21H	0	0	1	0	0	0	0	1	V33	VGMA1+(VGMA2-VGMA1)(2080+46 × 1)/3328
28H	0	0	1	0	0	0	0	0	V40	VGMA1+(VGMA2-VGMA1)(2080+46 × 8)/3328
29H	0	0	1	0	0	0	0	1	V41	VGMA1+(VGMA2-VGMA1)(2448+40 × 1)/3328
30H	0	0	1	1	1	0	0	0	V48	VGMA1+(VGMA2-VGMA1)(2448+40 × 8)/3328
31H	0	0	1	1	1	0	0	1	V49	VGMA1+(VGMA2-VGMA1)(2768+36 × 1)/3328
38H	0	0	1	1	1	0	0	0	V56	VGMA1+(VGMA2-VGMA1)(2768+36 × 8)/3328
39H	0	0	1	1	1	0	0	1	V57	VGMA1+(VGMA2-VGMA1)(3056+34 × 1)/3328
3FH	0	0	1	1	1	1	1	1	V63	VGMA1+(VGMA2-VGMA1)(3056+34 × 7)/3328
40H	0	1	0	0	0	0	0	0	V64	VGMA2
41H	0	1	0	0	0	0	0	1	V65	VGMA2+(VGMA3-VGMA2)(32 × 1)/2112
42H	0	1	0	0	0	0	1	0	V66	VGMA2+(VGMA3-VGMA2)(32 × 2)/2112
67H	0	1	1	0	0	1	1	1	V103	VGMA2+(VGMA3-VGMA2)(32 × 39)/2112
68H	0	1	1	0	1	0	0	0	V104	VGMA2+(VGMA3-VGMA2)(32 × 40)/2112
69H	0	1	1	0	1	0	0	1	V105	VGMA2+(VGMA3-VGMA2)(1280+34 × 1)/2112
78H	0	1	1	0	1	1	0	0	V120	VGMA2+(VGMA3-VGMA2)(1280+34 × 16)/2112
79H	0	1	1	0	1	1	0	1	V121	VGMA2+(VGMA3-VGMA2)(1824+36 × 1)/2112
7FH	0	1	1	1	1	1	1	1	V127	VGMA2+(VGMA3-VGMA2)(1824+36 × 7)/2112
80H	1	0	0	0	0	0	0	0	V128	VGMA3

Input Data	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	Output Voltage	
81H	1	0	0	0	0	0	0	1	V129	VGMA3+(VGMA4-VGMA3)(36 × 1)/2784
88H	1	0	0	0	1	0	0	0	V136	VGMA3+(VGMA4-VGMA3)(36 × 8)/2784
89H	1	0	0	0	1	0	0	1	V137	VGMA3+(VGMA4-VGMA3)(288+38 × 1)/2784
90H	1	0	0	1	0	0	0	0	V144	VGMA3+(VGMA4-VGMA3)(288+38 × 8)/2784
91H	1	0	0	1	0	0	0	1	V145	VGMA3+(VGMA4-VGMA3)(592+40 × 1)/2784
98H	1	0	0	1	1	0	0	0	V152	VGMA3+(VGMA4-VGMA3)(592+40 × 8)/2784
99H	1	0	0	1	1	0	0	1	V153	VGMA3+(VGMA4-VGMA3)(912+42 × 1)/2784
A0H	1	0	1	0	0	0	0	0	V160	VGMA3+(VGMA4-VGMA3)(912+42 × 8)/2784
A1H	1	0	1	0	0	0	0	1	V161	VGMA3+(VGMA4-VGMA3)(1248+44 × 1)/2784
A8H	1	0	1	0	1	0	0	0	V168	VGMA3+(VGMA4-VGMA3)(1248+44 × 8)/2784
A9H	1	0	1	0	1	0	0	1	V169	VGMA3+(VGMA4-VGMA3)(1600+48 × 1)/2784
B8H	1	0	1	1	1	0	0	0	V184	VGMA3+(VGMA4-VGMA3)(1600+48 × 16)/2784
B9H	1	0	1	1	1	0	0	1	V185	VGMA3+(VGMA4-VGMA3)(2368+52 × 1)/2784
BFH	1	0	1	1	1	1	1	1	V191	VGMA3+(VGMA4-VGMA3)(2368+52 × 7)/2784
C0H	1	1	0	0	0	0	0	0	V192	VGMA4
C1H	1	1	0	0	0	0	0	1	V193	VGMA4+(VGMA5-VGMA4)(56 × 1)/6710
C8H	1	1	0	0	1	0	0	0	V200	VGMA4+(VGMA5-VGMA4)(56 × 8)/6710
C9H	1	1	0	0	1	0	0	1	V201	VGMA4+(VGMA5-VGMA4)(448+64 × 1)/6710
D0H	1	1	0	1	0	0	0	0	V208	VGMA4+(VGMA5-VGMA4)(448+64 × 8)/6710
D1H	1	1	0	1	0	0	0	1	V209	VGMA4+(VGMA5-VGMA4)(960+72 × 1)/6710
D8H	1	1	0	1	0	0	0	0	V216	VGMA4+(VGMA5-VGMA4)(960+72 × 8)/6710
D9H	1	1	0	1	0	0	0	1	V217	VGMA4+(VGMA5-VGMA4)(1536+80 × 1)/6710
E0H	1	1	1	0	0	0	0	0	V224	VGMA4+(VGMA5-VGMA4)(1536+80 × 8)/6710
E1H	1	1	1	0	0	0	0	1	V225	VGMA4+(VGMA5-VGMA4)(2176+86 × 1)/6710
E8H	1	1	1	0	1	0	0	0	V232	VGMA4+(VGMA5-VGMA4)(2176+86 × 8)/6710
E9H	1	1	1	0	1	0	0	1	V233	VGMA4+(VGMA5-VGMA4)(2864+94 × 1)/6710
F0H	1	1	1	1	0	0	0	0	V240	VGMA4+(VGMA5-VGMA4)(2864+94 × 8)/6710
F1H	1	1	1	1	0	0	0	1	V241	VGMA4+(VGMA5-VGMA4)(3616+11 × 81)/6710
F8H	1	1	1	1	0	0	0	0	V248	VGMA4+(VGMA5-VGMA4)(3616+11 × 88)/6710
F9H	1	1	1	1	0	0	0	1	V249	VGMA4+(VGMA5-VGMA4)(4560+230 × 1)/6710
FFH	1	1	1	1	1	1	1	1	V255	VGMA4+(VGMA5-VGMA4)(4560+230 × 7)/6710
-					-				-	VGMA5

Input Data	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	Output Voltage	
00H	0	0	0	0	0	0	0	0	V0′	VGMA10
01H	0	0	0	0	0	0	0	1	V1	VGMA10+(VGMA9-VGMA10)(80 × 1)/3328
02H	0	0	0	0	0	0	1	0	V2	VGMA10+(VGMA9-VGMA10)(80 × 2)/3328
08H	0	0	0	0	1	0	0	0	V8	VGMA10+(VGMA9-VGMA10)(80 × 8)/3328
09H	0	0	0	0	1	0	0	1	V9	VGMA10+(VGMA9-VGMA10)(640+68 × 1)/3328
10H	0	0	0	1	0	0	0	0	V16	VGMA10+(VGMA9-VGMA10)(640+68 × 8)/3328
11H	0	0	0	1	0	0	0	1	V17	VGMA10+(VGMA9-VGMA10)(1184+60 × 1)/3328
18H	0	0	0	1	1	0	0	0	V24	VGMA10+(VGMA9-VGMA10)(1184+60 × 8)/3328
19H	0	0	0	1	1	0	0	1	V25	VGMA10+(VGMA9-VGMA10)(1664+52 × 1)/3328
20H	0	0	1	0	0	0	0	0	V32	VGMA10+(VGMA9-VGMA10)(1664+52 × 8)/3328
21H	0	0	1	0	0	0	0	1	V33	VGMA10+(VGMA9-VGMA10)(2080+46 × 1)/3328
28H	0	0	1	0	1	0	0	0	V40	VGMA10+(VGMA9-VGMA10)(2080+46 × 8)/3328
29H	0	0	1	0	1	0	0	1	V41	VGMA10+(VGMA9-VGMA10)(2448+40 × 1)/3328
30H	0	0	1	1	0	0	0	0	V48	VGMA10+(VGMA9-VGMA10)(2448+40 × 8)/3328
31H	0	0	1	1	0	0	0	1	V49	VGMA10+(VGMA9-VGMA10)(2768+36 × 1)/3328
38H	0	0	1	1	1	0	0	0	V56	VGMA10+(VGMA9-VGMA10)(2768+36 × 8)/3328
39H	0	0	1	1	1	0	0	1	V57	VGMA10+(VGMA9-VGMA10)(3056+34 × 1)/3328
3FH	0	0	1	1	1	1	1	1	V63	VGMA10+(VGMA9-VGMA10)(3056+34 × 7)/3328
40H	0	1	0	0	0	0	0	0	V64	VGMA9
41H	0	1	0	0	0	0	0	1	V65	VGMA9+(VGMA8-VGMA9)(32 × 1)/2112
42H	0	1	0	0	0	0	1	0	V66	VGMA9+(VGMA8-VGMA9)(32 × 2)/2112
67H	0	1	1	0	0	1	1	1	V103	VGMA9+(VGMA8-VGMA9)(32 × 39)/2112
68H	0	1	1	0	1	0	0	0	V104	VGMA9+(VGMA8-VGMA9)(32 × 40)/2112
69H	0	1	1	0	1	0	0	1	V105	VGMA9+(VGMA8-VGMA9)(1280+34 × 1)/2112
78H	0	1	1	0	1	1	0	0	V120	VGMA9+(VGMA8-VGMA9)(1280+34 × 16)/2112
79H	0	1	1	0	1	1	0	1	V121	VGMA9+(VGMA8-VGMA9)(1824+36 × 1)/2112
7FH	0	1	1	1	1	1	1	1	V127	VGMA9+(VGMA8-VGMA9)(1824+36 × 7)/2112
80H	1	0	0	0	0	0	0	0	V128	VGMA8

Input Data	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	Output Voltage	
81H	1	0	0	0	0	0	0	1	V129	VGMA8+(VGMA7-VGMA8)(36 × 1)/2784
88H	1	0	0	0	1	0	0	0	V136	VGMA8+(VGMA7-VGMA8)(36 × 8)/2784
89H	1	0	0	0	1	0	0	1	V137	VGMA8+(VGMA7-VGMA8)(288+38 × 1)/2784
90H	1	0	0	1	0	0	0	0	V144	VGMA8+(VGMA7-VGMA8)(288+38 × 8)/2784
91H	1	0	0	1	0	0	0	1	V145	VGMA8+(VGMA7-VGMA8)(592+40 × 1)/2784
98H	1	0	0	1	1	0	0	0	V152	VGMA8+(VGMA7-VGMA8)(592+40 × 8)/2784
99H	1	0	0	1	1	0	0	1	V153	VGMA8+(VGMA7-VGMA8)(912+42 × 1)/2784
A0H	1	0	1	0	0	0	0	0	V160	VGMA8+(VGMA7-VGMA8)(912+42 × 8)/2784
A1H	1	0	1	0	0	0	0	1	V161	VGMA8+(VGMA7-VGMA8)(1248+44 × 1)/2784
A8H	1	0	1	0	1	0	0	0	V168	VGMA8+(VGMA7-VGMA8)(1248+44 × 8)/2784
A9H	1	0	1	0	1	0	0	1	V169	VGMA8+(VGMA7-VGMA8)(1600+48 × 1)/2784
B8H	1	0	1	1	1	0	0	0	V184	VGMA8+(VGMA7-VGMA8)(1600+48 × 16)/2784
B9H	1	0	1	1	1	0	0	1	V185	VGMA8+(VGMA7-VGMA8)(2368+52 × 1)/2784
BFH	1	0	1	1	1	1	1	1	V191	VGMA8+(VGMA7-VGMA8)(2368+52 × 7)/2784
C0H	1	1	0	0	0	0	0	0	V192	VGMA7
C1H	1	1	0	0	0	0	0	1	V193	VGMA7+(VGMA6-VGMA7)(56 × 1)/6710
C8H	1	1	0	0	1	0	0	0	V200	VGMA7+(VGMA6-VGMA7)(56 × 8)/6710
C9H	1	1	0	0	1	0	0	1	V201	VGMA7+(VGMA6-VGMA7)(448+64 × 1)/6710
D0H	1	1	0	1	0	0	0	0	V208	VGMA7+(VGMA6-VGMA7)(448+64 × 8)/6710
D1H	1	1	0	1	0	0	0	1	V209	VGMA7+(VGMA6-VGMA7)(960+72 × 1)/6710
D8H	1	1	0	1	0	0	0	0	V216	VGMA7+(VGMA6-VGMA7)(960+72 × 8)/6710
D9H	1	1	0	1	0	0	0	1	V217	VGMA7+(VGMA6-VGMA7)(1536+80 × 1)/6710
E0H	1	1	1	0	0	0	0	0	V224	VGMA7+(VGMA6-VGMA7)(1536+80 × 8)/6710
E1H	1	1	1	0	0	0	0	1	V225	VGMA7+(VGMA6-VGMA7)(2176+86 × 1)/6710
E8H	1	1	1	0	1	0	0	0	V232	VGMA7+(VGMA6-VGMA7)(2176+86 × 8)/6710
E9H	1	1	1	0	1	0	0	1	V233	VGMA7+(VGMA6-VGMA7)(2864+94 × 1)/6710
F0H	1	1	1	1	0	0	0	0	V240	VGMA7+(VGMA6-VGMA7)(2864+94 × 8)/6710
F1H	1	1	1	1	0	0	0	1	V241	VGMA7+(VGMA6-VGMA7)(3616+118 × 1)/6710
F8H	1	1	1	1	0	0	0	0	V248	VGMA7+(VGMA6-VGMA7)(3616+118 × 8)/6710
F9H	1	1	1	1	0	0	0	1	V249	VGMA7+(VGMA6-VGMA7)(4560+230 × 1)/6710
FFH	1	1	1	1	1	1	1	1	V255	VGMA7+(VGMA6-VGMA7)(4560+230 × 7)/6710
-					-				-	VGMA6

ABSOLUTE MAXIMUM RATING

(V_{SS1} = V_{SS2} = 0V)

Parameter	Symbol	Condition	Unit
Supply Voltage	V_{DD1}	–0.3 to +6.5	V
	V_{DD2}	–0.3 to +16.5	
Input Voltage	VGMA1 to 10	–0.3 to V_{DD1}+0.3	
	Other	–0.3 to V_{DD11}+0.3	
Output Voltage	DIO1, DIO2	–0.3 to V_{DD1}+0.3	
	Y1 to Y384	–0.3 to V_{DD2}+0.3	
Operation Temperature	Topr	–20 to +75	°C
Storage Temperature	Tstg	–55 to +125	
Operation Power Dissipation	Pd	300	mW

NOTES:

1. If LSIs are stressed beyond the above absolute maximum ratings, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the below recommended operating range is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. Power on sequence
   V_{DD1} → input voltage → V_{DD2} → VGMA1 to VGMA10

RECOMMENDED OPERATIONG RANGE

(Ta= –20 to +75°C, V_{SS1} = V_{SS2} = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD1}	2.5	3.3	3.6	V
	V_{DD2}	8.0	12.0	15	
γ-corrected voltage	VGMA1 to VGMA5	0.5V_{DD2}+0.2	–	V_{DD2}-0.1	
	VGMA6 to VGMA10	V_{SS2}+0.1	–	0.5V_{DD2}-0.2	
Output voltage range	Vyo	V_{SS2}+0.1	–	V_{DD2}-0.1	
Max. clock frequency	Fmax	–	–	65 (V_{DD1}=2.5V)	MHz
Output Load capacitance	CL	–	–	200	pF/PIN

NOTES:

1. V_{SS1} = V_{SS2} = 0V
2. $V_{DD1} \leq V_{DD2}$

DC CHARACTERISTICS

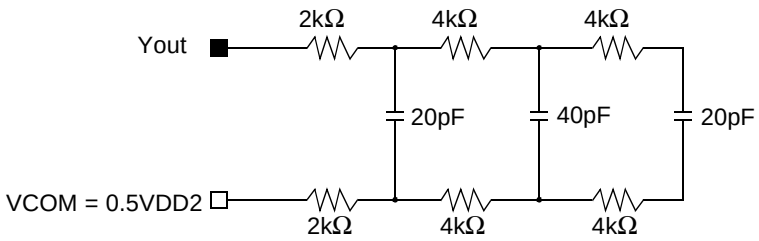
(Ta = –20 to +75°C, V_{DD1} = 2.5 to 3.6V, V_{DD2} = 8.0 to 15.0V, V_{SS1} = V_{SS2} = 0V)

Parameter	Symbol	Condition/applied Pin	Min.	Typ.	Max.	Unit
Low level input voltage	VIH	SHL, CLK2, D00 to D57, CLK1,POL, DIO1 (DIO2) DATPOL1,2 , SELT	$0.75V_{DD1}$	–	V_{DD1}	V
High level input voltage	VIL		0	–	0.25VDD1	
Input leak current	IL	D00 to D57, SHL, CLK2, CLK1, POL	–1	–	1	uA
High level output voltage	VOH	DIO1 (DIO2), IO = –1.0mA	V_{DD1}-0.5	–	–	V
Low level output voltage	VOL	DIO1 (DIO2), IO+1.0mA	-	–	0.5	V
Resister	R0 to R255	–	Rn × 0.7	–	Rn × 1.3	Ω
Driver output current	IVOH	V_{DD2} = 10.0V Vx = 3.5V, Vyo = 9.5V	–	–1.5	–0.5	mA
	IVOL	V_{DD2} = 10.0v Vx = 6.5V, Vyo=0.5V	0.5	1.5	–	
Output voltage deviation	ΔVO	:	–	± 3	–	mV
Output voltage range	VYO	:	V_{SS2}+0.1	-	V_{DD2}-0.1	V
Logic part dynamic power consumption	IDDI	V_{DD1} = 3.0V * NOTE1	–	4.0	7.0	mA
Driver part dyanmic power counsumption	IDD2	V_{DD2} = 10V * NOTE1, 2	–	10	15	

(Vyo is the output voltage of analog output pins Y1 to Y402.)
(Vx is the applied voltage of analog output pins Y1 to Y402.)

NOTES:

1. CLK1 cycle = 15µs, fCLK2 = 55MHz, data pattern = 1010…
2. Yout load condition.



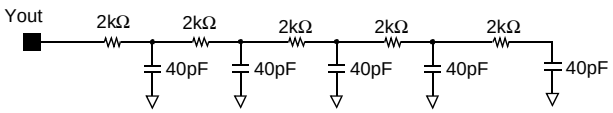
AC CHARACTERISTICS

(Ta = -20°C to +75°C, VDD1 = 2.5 to 3.6V, VDD2 = 8.0 to 15.0V, VSS1 = VSS2 = 0V)

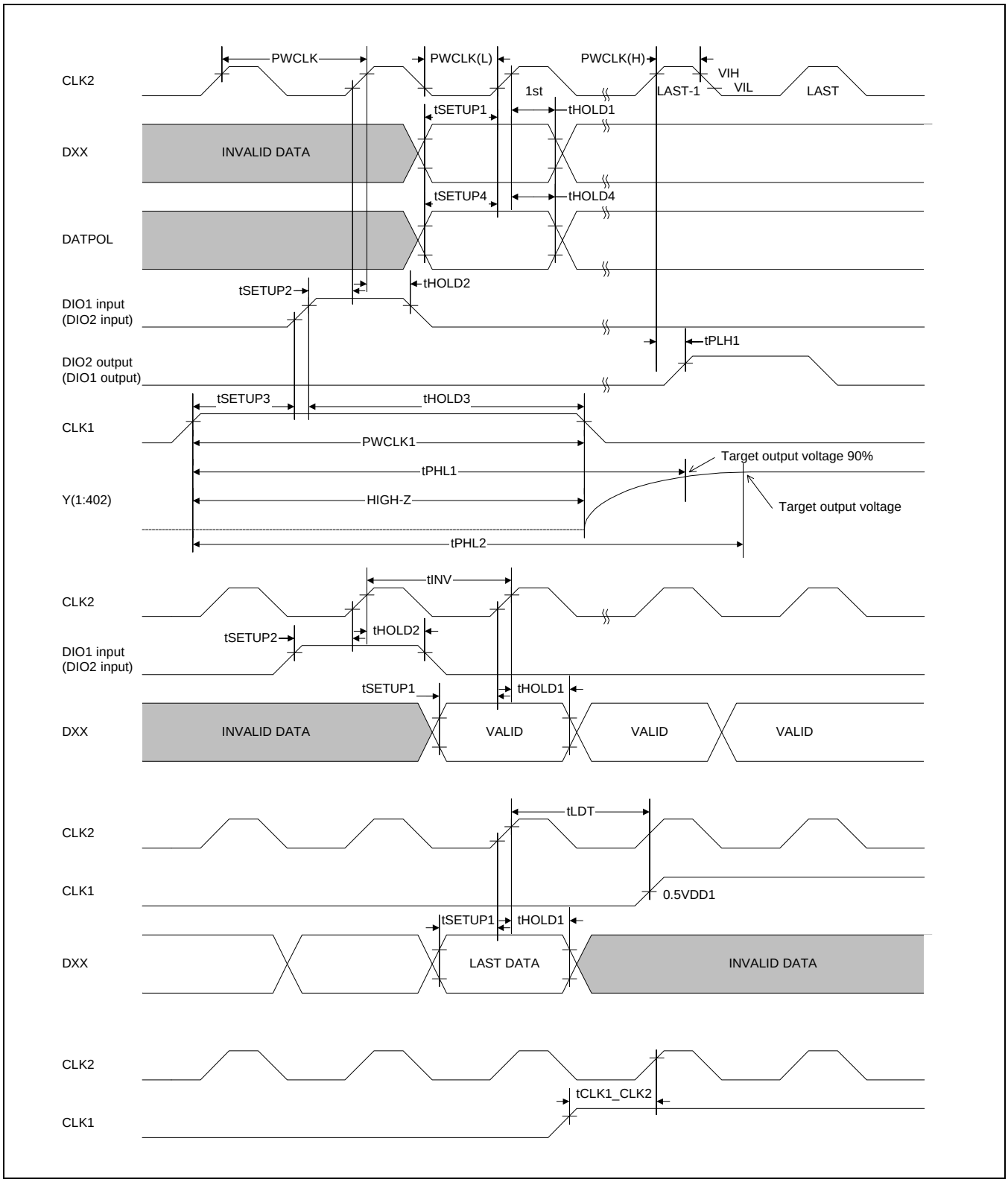
Parameter	Symbol	Conditions/ Applied Pin	Min.	Typ.	Max.	Unit
Clock pulse width	PWCLK	–	15.4	–	–	ns
Clock low period	PWCLK(L)	–	5	–	–	
Clock high period	PWCLK(H)	–	5	–	–	
Data set-up time	tSETUP1	–	5	–	–	
Data hold time	tHOLD1	–	0	–	–	
Start pulse set-up time	tSETUP2	–	5	–	–	
Start pulse hold time	tHOLD2	–	0	–	–	
DATPOL-CLK2 set-up time	tSETUP4	–	5	–	–	
DATPOL-CLK2 set-up time	tHOLD4	–	0	–	–	
Start pulse time	tPLH1	CL = 20pF	-	–	12	
CLK1 set-up time	tSETUP3	–	1	–	–	CLK2 PERIOD
CLK1 hold time	tHOLD3	–	–	–	–	
Driver output	tPHL1	Note 3	–	–	5	us
Driver output	tPHL2	Note 3	–	–	10	
CLK1 high period	PWCLK1	–	0.2	–	2	
Data invalid period	tINV	–	1	–	–	CLK2 PERIOD
Last data timing	tLDT	–	1	–	–	
CLK1-CLK2	tCLK1-tCLK2	CLK1 ↑ or ↓ → CLK2 ↑	6	–	–	ns
POL-CLK1	tPOL-tCLK1	POL ↑ or ↓ → CLK1 ↑	-9	–	–	ns
CLK1-POL	tCLK1-POL	CLK1 ↑ → POL ↑ or ↓	4	–	–	CLK2 PERIOD

NOTE:

3. Yout Load Condition



AC Waveform (VIH = 0.75V_{DD1}, VIL= 0.25V_{DD1})



Relation between CLK1 and Start pulse(DIO1,DIO2)