INTRODUCTION

64G/S 300/309CH. SOURCE DRIVER

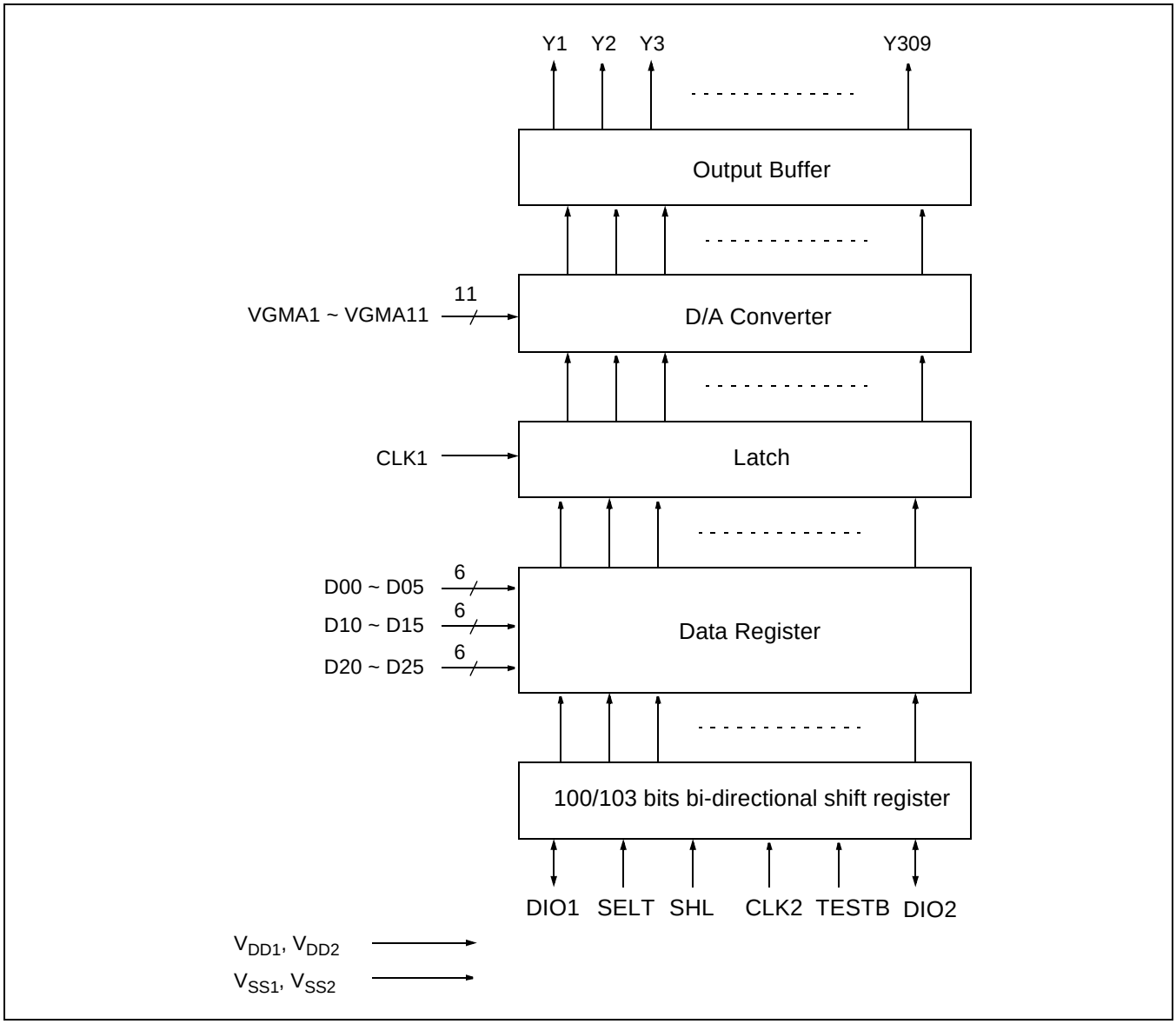
The KS0641 is a 300-channel or 309-channel output, TFT-LCD source driver for 64 gray scale displays. Data input is a digital input consisting of 6 bits by 3 dots, while can realize a full-color display of 260,000 colors by output of 64 values γ-corrected. This device has an internal D/A (digital-to-analog) converter for each output and utilizes 9 or 11 external power supplies.

The KS0641 can be adjusted to large panel, and SHL (Shift direction selection) pin makes use of the LCD panel connection convenient. Maximum operation clock frequency is 55 MHz at a 3.3 V logic operation and it can be applied to the TFT LCD panel of SVGA/XGA standards.

FEATURES

- ❑ TFT active matrix LCD source driver LSI
- ❑ 64 outputs are possible through 9 or 11 external power supply and D/A converter
- ❑ CMOS level input
- ❑ 6 bits (G/S data) × 3 dots (RGB) input
- ❑ Logic supply voltage: 3.3 V (Typ.)
- ❑ LCD drive supply voltage: 5.0 V (Typ.)
- ❑ Maximum operation clock frequency :
  fmax = 55MHz (internal data transmission rate at 3.3V operation)
- ❑ Output: 309 outputs (300 outputs are available)
- ❑ Slim TCP

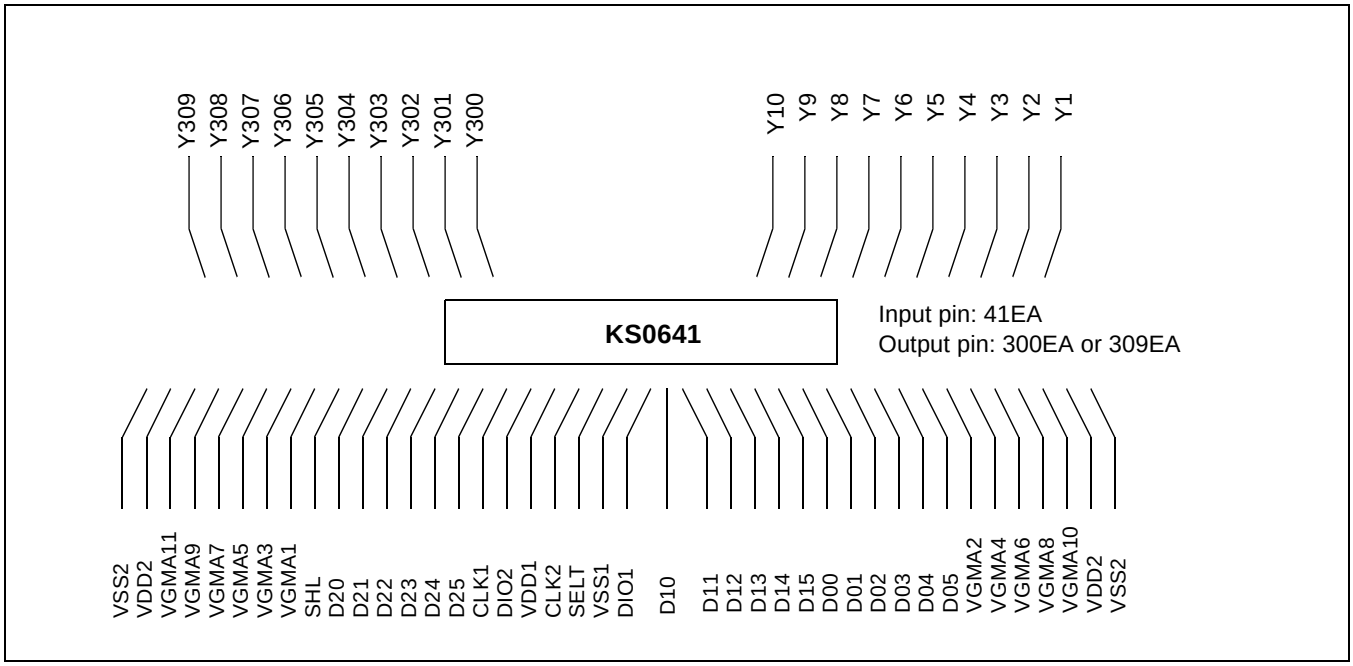
BLOCK DIAGRAM



PIN DESCRIPTION

Pin Symbol	Pin Name	Description
V_{DD1}	Logic power supply	3.0 V to 5.5V
V_{DD2}	Driver power supply	3.0V to 5.5V
V_{SS1}	Logic ground	Ground (0V)
V_{SS2}	Driver ground	Ground (0V)
Y1~Y309	Driver Output	The D/A converted 64 G/S analog voltage is output
D0<0:5> D1<0:5> D2<0:5>	Display data input	The display data is input with a width of 18 bits, gray scale data (6 bits) × 3 dots (R, G, B) DX0:LSB, DX5:MSB
SHL	Shift direction control input	This pin controls the direction of shift register in cascade connection. The shift direction of the shift register is as follows. SHL = H: DIO1 input (Y1→ Y309), DIO2 output SHL = L: DIO2 input (Y309→ Y1), DIO1 output
DIO1	Right shift start pulse input/output	SHL = H: Used as the start pulse input pin SHL = L: Used as the start pulse output pin
DIO2	Left shift start pulse input/output	SHL = H: Used as the start pulse output pin SHL = L: Used as the start pulse input pin
CLK2	Shift clock input	Refer to shift clock input of the shift register. The display data is loaded to the data register at the rising edge of CLK2.
CLK1	Latch input	Latches the data register contents as rising edge and transfers it to the D/A converter. Also, after CLK1 input, clears the internal shift register contents. After 1 pulse input on start, operates normally. CLK1 input timing refers to the Relationship between CLK1 start pulse(DIO1,DIO2) and blanking period of the switching characteristic waveform. (page 9)
VGMA1 to VGMA11	γ-corrected power supplies	Input the -corrected power supplies from external source. V_{SS2}< VGMA1≤VGMA2 ≤VGMA3≤·····≤VGMA11<V_{DD2} or V_{SS2}< VGMA11≤VGMA10 ≤·····≤VGMA1<V_{DD2} Keep gray scale power supply unchanged during the gray scale voltage output.
SELT	300/309CH output control input	This pin controls 300CH or 309CH output The number of output channel is as follows. SELT = L: Y309 output SELT = H: Y300 output → Y151 to Y159 are useless. This pin is internally pulled-up. < Rpu ≅ 30kΩ >
TESTB	Test pin	TESTB = H: Normal operation. TESTB = L: TEST mode → OP AMP cut-off This pin is internally pulled-up. < Rpu ≅ 30kΩ >

TCP PIN CONFIGURATION



NOTES:

1. This figure does not specify the dimensions of the TCP package.
2. In actual panel application, the power should be supplied through all the V_{DD2} and V_{SS2} pins simultaneously.

ABSOLUTE MAXIMUM RATINGS (V_{SS1} = V_{SS2} = 0V)

Characteristic	Symbol	Rating	Unit
Digital supply voltage	V_{DD1}	–0.3 to +6.5	V
Analog supply voltage	V_{DD2}	–0.3 to +6.5	V
Input voltage	VGMA1 to VGMA11	–0.3 to V_{DD2}+0.3	V
	Other	–0.3 to V_{DD1}+0.3	
Output voltage	DIO1, DIO2	–0.3 to V_{DD1}+0.3	V
	Y1 to Y309	–0.3 to V_{DD2}+0.3	
Operation Temperature	Topr	–20 to +75	C
Storage Temperature	Tstg	–55 to +150	C

If LSIs are stressed beyond the above absolute maximum ratings, they may be permanently destroyed.
These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the below recommended operating range is not implied.
Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

NOTE: Power on sequence : V_{DD1} → input voltage → V_{DD2} → VGMA1 to VGMA11

RECOMMENDED OPERATION RANGE (Ta = –20 to +75°C, V_{SS1} = V_{SS2} = 0V)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital supply voltage	VDD1	–	3.0	–	5.5	V
Analog supply voltage	VDD2	–	3.0	–	5.5	V
γ - corrected voltage	VGMA2 to VGMA10	–	V_{SS2}+0.2	–	V_{DD2}-0.2	V
	VGMA1	Case 1	V_{SS2}	–	VGMA2	V
		Case 2	VGMA2	–	V_{DD2}	V
	VGMA11	Case 1	VGMA10	–	V_{DD2}	V
		Case 2	V_{SS2}	–	VGMA10	V
Output voltage range	VYO	–	V_{SS2}+0.2	–	V_{DD2}-0.2	V
Max. clock frequency	*Note1. fmax	–	-	–	55	MHz
Output Load capacitance	CL	–	-	–	150	pF

NOTES:

1. V_{DD1} = 3.3V
   Case 1: V_{SS2}<VGMA1, VGMA2≤ VGMA3≤····· ≤VGMA9≤VGMA10, VGMA11<V_{DD2}
   Case 2: V_{SS2}<VGMA11, VGMA10≤ VGMA9≤····· ≤VGMA3≤VGMA2, VGMA1<V_{DD2}

DC CHARACTERISTICS

(Ta = –20 to +75°C, V_{DD1} = 3.0 to 5.0V, V_{DD2}= 3.0 to 5.0V, V_{SS1} = V_{SS2} = 0V)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	VIH	SHL, CLK2, CLK1, SELT, DIO1 (DIO2), D00 ~ D05, D10 ~ D15, D20 ~ D25	$0.7V_{DD1}$	–	V_{DD1}	V
Low level input voltage	VIL		0	–	$0.3V_{DD1}$	V
Input leak current	IL	D00~D05,D10~D15,D20~D25 SHL,CLK2, CLK1, DIO1(2)	–1	–	1	µA
Pull-up Resistance	Rpu	V_{DD1} = 3.3V, SELT, TEST	–	30	–	kΩ
High level output voltage	VOH	DIO1 (DIO2), IO = –1.0	V_{DD1}-0.5	–	–	V
Low level output voltage	VOL	DIO1 (DIO2), IO = +1.0	–	–	0.5	V
Resistance between γ-corrected voltage	RGMA1 to RGMA10	*refer to page 12 resistance ladder circuit	–	*refer to page12	–	Ω
Driver output current	IVOH	V_{DD1}=5.0V, V_{DD2}=5.0V, Vx=3.5V, Vyo=4.5V	–	–1.5	–0.5	mA
	IVOL	V_{DD1}=5.0V, V_{DD2}=5.0V, Vx=0.5V, Vyo=0.5V	0.5	1.5	–	mA
Output voltage deviation	VO	V_{DD2}=5.0V VGMA11=0.5V,VGMA10=1.0V VGMA9 = 1.5V, ··· VGMA3 = 4.0V, VGMA2, VGMA1 = 4.5V	–	±20	–	mV
Output voltage range	VYO	INPUT DATA : 00~3FH	V_{SS2}+0.2	–	V_{DD2}-0.2	V
Logic part dynamic current consumption	IDD1	*Note1, Note2. V_{DD1}=5.0V No load.	–	3.5	5.5	mA
Driver part dynamic current consumption	IDD2	*Note1, Note2, V_{DD2}=5.0V VGMA1=4.5V, VGMA11=0.5V	–	5.5	7.0	mA

(Vyo is the output voltage of analog output pins Y1 to Y309.)
(Vx is the applied voltage of analog output pins Y1 to Y309.)

NOTES:

1. CLK1 cycle = 30µs, fCLK2 = 30MHz, data pattern = 1010····· (Checkerboard pattern), Ta=25°C
2. The current consumption per driver when SVGA single-sided mounting (8units) are connected in cascade. (CL=150pF)

AC CHARACTERISTICS

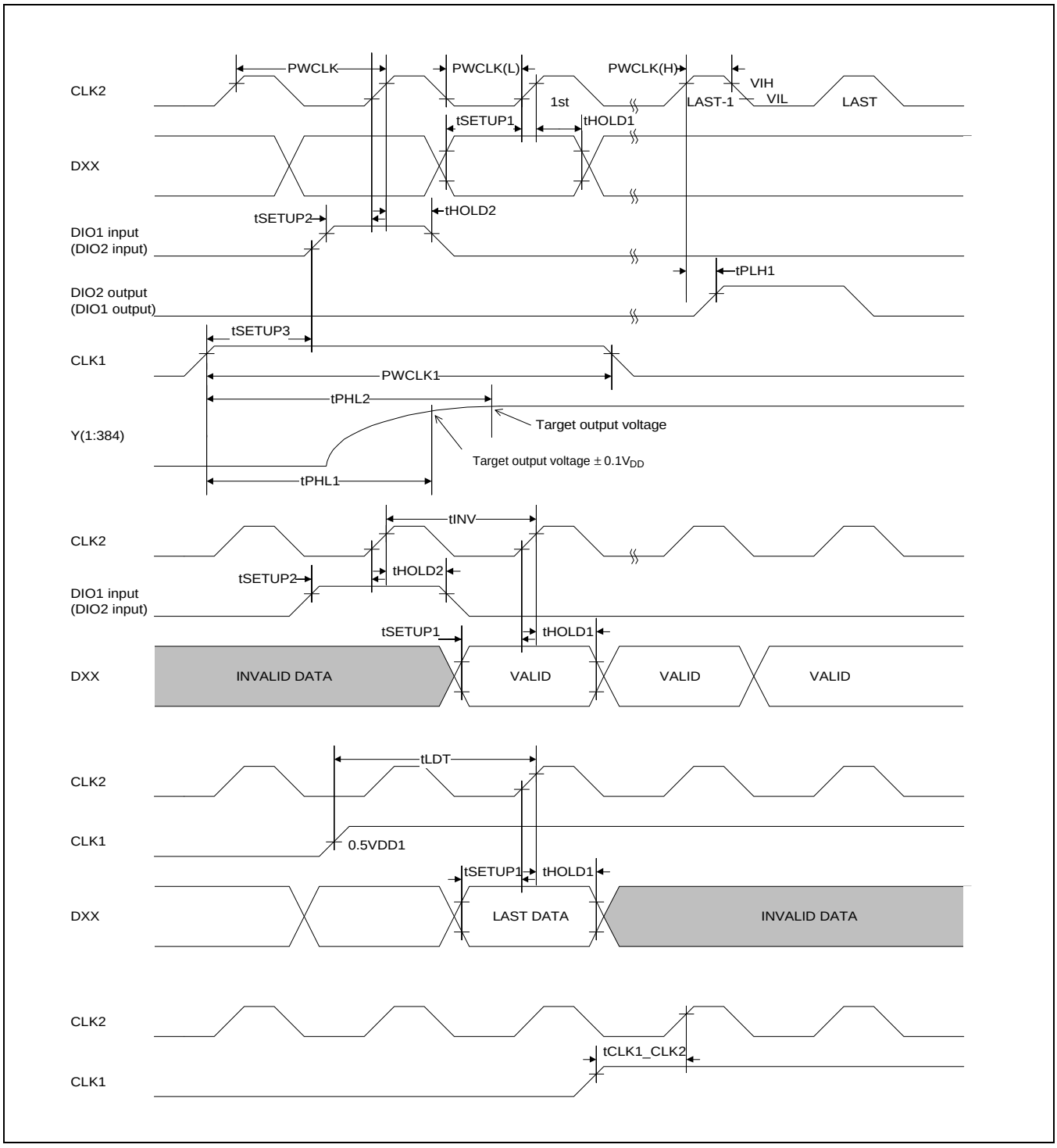
(Ta = –20 to +75°C, V_{DD1} = 3.0 to 5.5V, V_{DD2} = 3.0 to 5.5V, V_{SS1} = V_{SS2} = 0V)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse width	PWCLK	–	18	–	–	ns
Clock pulse low period	PWCLK(L)	–	4	–	–	
Clock pulse high period	PWCLK(H)	–	4	–	–	
Data setup time	tSETUP1	–	4	–	–	
Data hold time	tHOLD1	–	0	–	–	
Start pulse setup time	tSETUP2	–	4	–	–	
Start pulse hold time	tHOLD2	–	0	–	–	
Start pulse delay time	tPLH1	CL = 35pF	-	–	14	
CLK1 setup time	tSETUP3	–	1	–	–	CLK2 cycle
CLK1 high pulse width	tCLK1	–	3	–	–	
Driver output delay time(1)	tPHL1	CL=150pF, Note4.	-	–	3	µs
Driver output delay time(2)	tPHL2	CL = 150pF, Note5.	-	–	10	
Data invalid time	tINV	Note 6	1			CLK2 cycle
Last data timing	tLDT	–	-	–	1	
CLK1-CLK2 time	tCLK1-CLK2	CLK1 ↑ → CLK2 ↑	7	–	–	ns

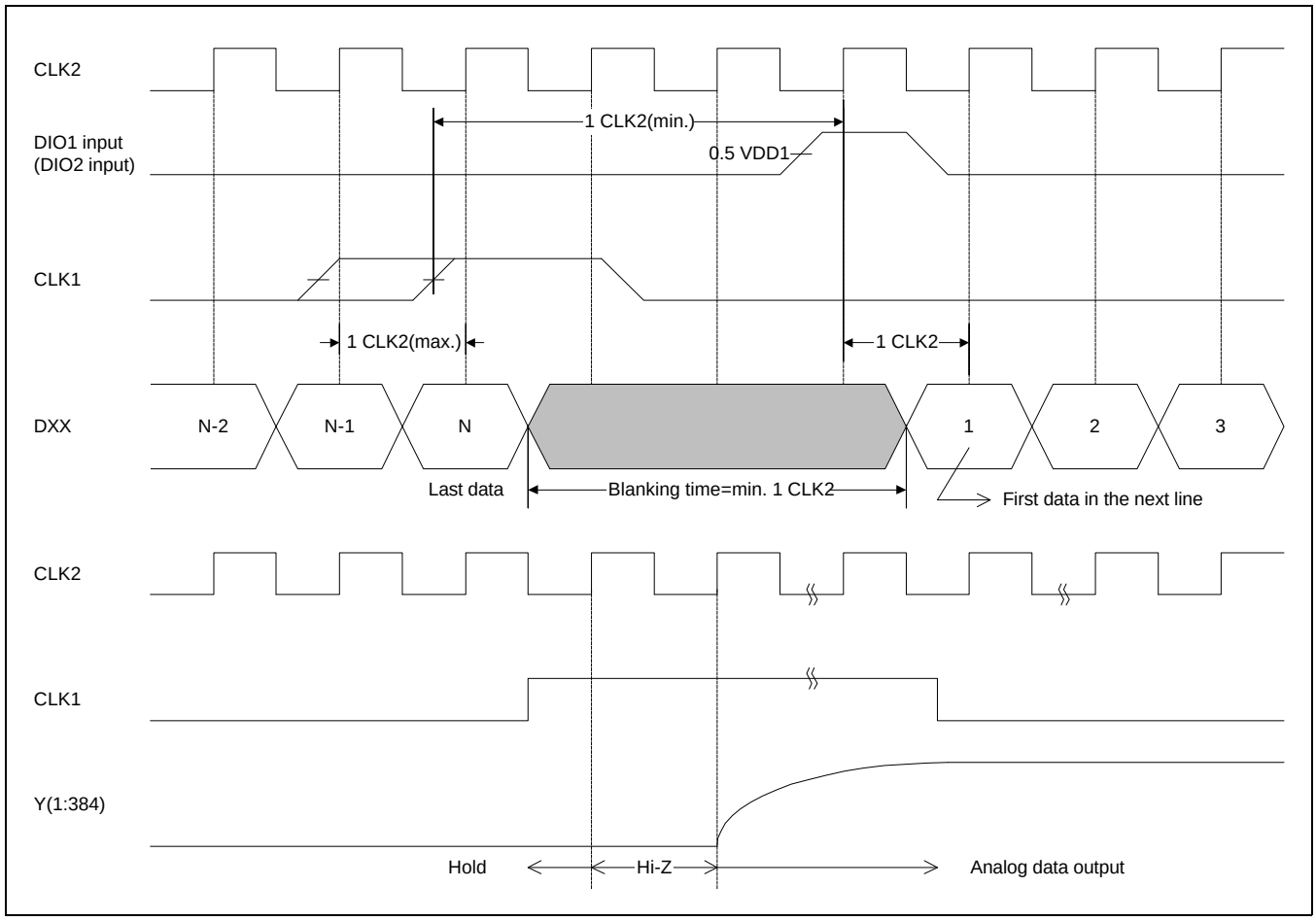
NOTES:

4. The value is specified when the drive voltage value reaches the target output voltage level of $0.1V_{DD2}$
5. The value is specified when the drive voltage value reaches the target output voltage level of 6-bit accuracy.
6. Set the rising edge of the first CLK2 after the rising edge of DIO1(or DIO2).

AC Waveform (VIH=0.7V_{DD1}, VIL=0.3V_{DD1})



Relationship between CLK1/start pulse (DIO1, DIO2) and blanking period.



DISPLAY DATA TRANSFER

DIO1 (or DIO2) = “H” is loaded into internal latch at the rising edge of CLK2, which starts the data transfer operation, and after the falling edge of DIO1 (or DIO2), display data is valid at the rising edge of CLK2.
Once all the data of 309 channels is loaded into internal latch, it goes into standby state automatically, and any new data is not accepted even though CLK2 is provided until next DIO1(or DIO2) input.
When DIO1 (or DIO2) is provided, new display data is valid at the next rising edge of CLK2 after the falling edge of DIO1 (or DIO2).

EXTENSION OF OUTPUT

Output pin can be adjusted to an extended screen by cascade connection.

- SHL = “L”
  Connect DIO1 pin of previous stage to the DIO2 pin of next stage and all the input pins except DIO1 and DIO2 are connected together in each device.

- SHL = “H”
  Connect DIO2 pin of previous stage to the DIO1 pin of next stage and all the input pins except DIO1 and DIO2 are connected together in each device.

RELATIONSHIP #1 BETWEEN THE INPUT DATA AND OUTPUT VOLTAGE

Outputs 64-level gray scale voltage generated by level 9 or 11 of γ-corrected power supplies (VGMA1 to VGMA11) and 6-bit digital data.
data format : 1 PIXEL data (6 bits) × RGB (3 dots)
input width : 18 bits.

- Details on display data

DX5	DX4	DX3	DX2	DX1	DX0
Upper bits					Lower bits

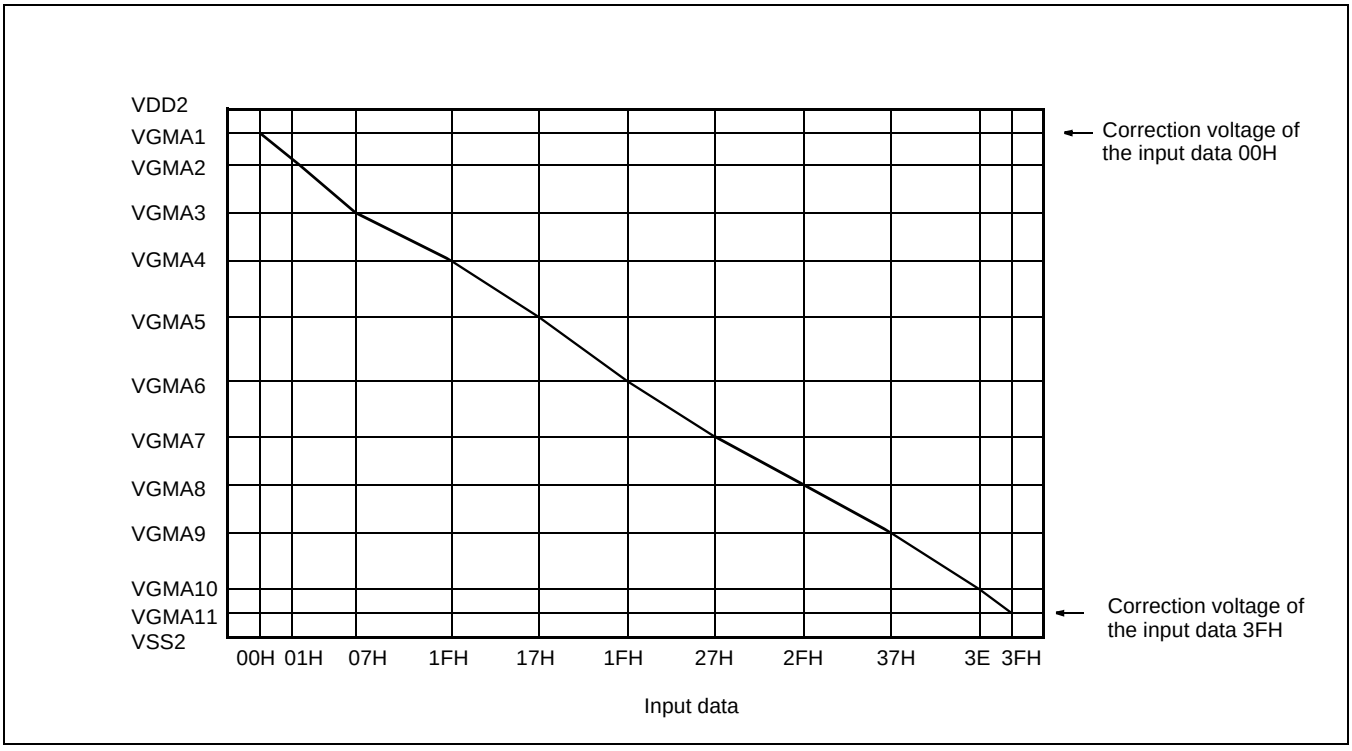
- Relationship between shift direction and output data
  SHL = H (Right shift)

Output	Y1	Y2	Y3	-------	Y307	Y308	Y309
DATA	D00 to D05	D10 to D15	D20~D25	-------	D00 to D05	D10 to D15	D20 to D25

SHL = L (Left shift)

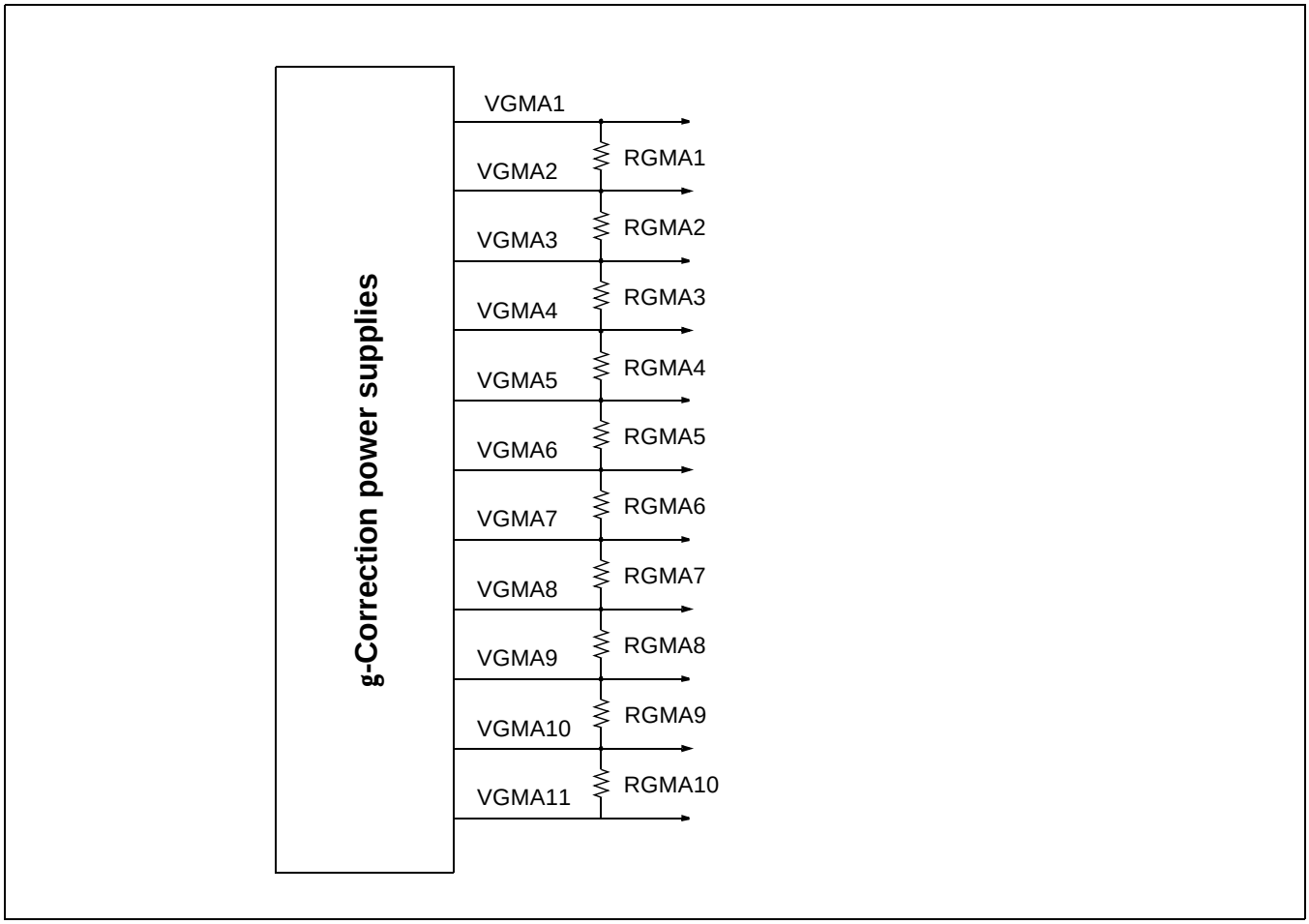
Output	Y1	Y2	Y3	-------	Y307	Y308	Y309
DATA	D00 to D05	D10 to D15	D20 to D25	-------	D00 to D05	D10 to D15	D20 to D25

γ - cOrrection Characteristic Curve



RELATIONSHIP BETWEEN THE INPUT DATA AND OUTPUT VOLTAGE

All 309outputs of the KS0641 are driven by separate 6-bit D/A converters.
The output voltage of each D/A converter, 64-level gray scale voltage, is determined by the reference voltages VGMA1 to VGMA11. The D/A converter consists of ladder resistors of which R0 to R63 are so designed that the ratios between the LCD panels g-corrected voltages and V0 to V63.



RELATIONSHIP #2 BETWEEN THE INPUT DATA AND OUTPUT VOLTAGE

In case of using 11 levels of g-corrected power supplies (VGMA1 to VGMA11)

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage	
00H	0	0	0	0	0	0	V0	VGMA1
01H	0	0	0	0	0	1	V1	VGMA3+(VGMA2-VGMA3)× 6/7
02H	0	0	0	0	1	0	V2	VGMA3+(VGMA2-VGMA3)× 5/7
03H	0	0	0	0	1	1	V3	VGMA3+(VGMA2-VGMA3)× 4/7
04H	0	0	0	1	0	0	V4	VGMA3+(VGMA2-VGMA3)× 3/7
05H	0	0	0	1	0	1	V5	VGMA3+(VGMA2-VGMA3)× 2/7
06H	0	0	0	1	1	0	V6	VGMA3+(VGMA2-VGMA3)× 1/7
07H	0	0	0	1	1	1	V7	VGMA3
08H	0	0	1	0	0	0	V8	VGMA4+(VGMA3-VGMA4)× 7/8
09H	0	0	1	0	0	1	V9	VGMA4+(VGMA3-VGMA4)× 6/8
0AH	0	0	1	0	1	0	V10	VGMA4+(VGMA3-VGMA4)× 5/8
0BH	0	0	1	0	1	1	V11	VGMA4+(VGMA3-VGMA4)× 4/8
0CH	0	0	1	1	0	0	V12	VGMA4+(VGMA3-VGMA4)× 3/8
0DH	0	0	1	1	0	1	V13	VGMA4+(VGMA3-VGMA4)× 2/8
0EH	0	0	1	1	1	0	V14	VGMA4+(VGMA3-VGMA4)× 1/8
0FH	0	0	1	1	1	1	V15	VGMA4
10H	0	1	0	0	0	0	V16	VGMA5+(VGMA4-VGMA5) × 7/8
11H	0	1	0	0	0	1	V17	VGMA5+(VGMA4-VGMA5) × 6/8
12H	0	1	0	0	1	0	V18	VGMA5+(VGMA4-VGMA5) × 5/8
13H	0	1	0	0	1	1	V19	VGMA5+(VGMA4-VGMA5) × 4/8
14H	0	1	0	1	0	0	V20	VGMA5+(VGMA4-VGMA5) × 3/8
15H	0	1	0	1	0	1	V21	VGMA5+(VGMA4-VGMA5) × 2/8
16H	0	1	0	1	1	0	V22	VGMA5+(VGMA4-VGMA5) × 1/8
17H	0	1	0	1	1	1	V23	VGMA5
18H	0	1	1	0	0	0	V24	VGMA6+(VGMA5-VGMA6) × 7/8
19H	0	1	1	0	0	1	V25	VGMA6+(VGMA5-VGMA6) × 6/8
1AH	0	1	1	0	1	0	V26	VGMA6+(VGMA5-VGMA6) × 5/8
1BH	0	1	1	0	1	1	V27	VGMA6+(VGMA5-VGMA6) × 4/8
1CH	0	1	1	1	0	0	V28	VGMA6+(VGMA5-VGMA6) × 3/8
1DH	0	1	1	1	0	1	V29	VGMA6+(VGMA5-VGMA6) × 2/8
1EH	0	1	1	1	1	0	V30	VGMA6+(VGMA5-VGMA6) × 1/8
1FH	0	1	1	1	1	1	V31	VGMA6

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage	
20H	1	0	0	0	0	0	V32	VGMA7+(VGMA6-VGMA7) × 7/8
21H	1	0	0	0	0	1	V33	VGMA7+(VGMA6-VGMA7) × 6/8
22H	1	0	0	0	1	0	V34	VGMA7+(VGMA6-VGMA7) × 5/8
23H	1	0	0	0	1	1	V35	VGMA7+(VGMA6-VGMA7) × 4/8
24H	1	0	0	1	0	0	V36	VGMA7+(VGMA6-VGMA7) × 3/8
25H	1	0	0	1	0	1	V37	VGMA7+(VGMA6-VGMA7) × 2/8
26H	1	0	0	1	1	0	V38	VGMA7+(VGMA6-VGMA7) × 1/8
27H	1	0	0	1	1	1	V39	VGMA7
28H	1	0	1	0	0	0	V40	VGMA8+(VGMA7-VGMA8) × 7/8
29H	1	0	1	0	0	1	V41	VGMA8+(VGMA7-VGMA8) × 6/8
2AH	1	0	1	0	1	0	V42	VGMA8+(VGMA7-VGMA8) × 5/8
2BH	1	0	1	0	1	1	V43	VGMA8+(VGMA7-VGMA8) × 4/8
2CH	1	0	1	1	0	0	V44	VGMA8+(VGMA7-VGMA8) × 3/8
2DH	1	0	1	1	0	1	V45	VGMA8+(VGMA7-VGMA8) × 2/8
2EH	1	0	1	1	1	0	V46	VGMA8+(VGMA7-VGMA8) × 1/8
2FH	1	0	1	1	1	1	V47	VGMA8
30H	1	1	0	0	0	0	V48	VGMA9+(VGMA8-VGMA9) × 7/8
31H	1	1	0	0	0	1	V49	VGMA9+(VGMA8-VGMA9) × 6/8
32H	1	1	0	0	1	0	V50	VGMA9+(VGMA8-VGMA9) × 5/8
33H	1	1	0	0	1	1	V51	VGMA9+(VGMA8-VGMA9) × 4/8
34H	1	1	0	1	0	0	V52	VGMA9+(VGMA8-VGMA9) × 3/8
35H	1	1	0	1	0	1	V53	VGMA9+(VGMA8-VGMA9) × 2/8
36H	1	1	0	1	1	0	V54	VGMA9+(VGMA8-VGMA9) × 1/8
37H	1	1	0	1	1	1	V55	VGMA9
38H	1	1	1	0	0	0	V56	VGMA10+(VGMA9-VGMA10) × 6/7
39H	1	1	1	0	0	1	V57	VGMA10+(VGMA9-VGMA10) × 5/7
3AH	1	1	1	0	1	0	V58	VGMA10+(VGMA9-VGMA10) × 4/7
3BH	1	1	1	0	1	1	V59	VGMA10+(VGMA9-VGMA10) × 3/7
3CH	1	1	1	1	0	0	V60	VGMA10+(VGMA9-VGMA10) × 2/7
3DH	1	1	1	1	0	1	V61	VGMA10+(VGMA9-VGMA10) × 1/7
3EH	1	1	1	1	1	0	V62	VGMA10
3FH	1	1	1	1	1	1	V63	VGMA11

- RVGMA (γ-Corrected Resistance) Ratio. (If the RGMA1 equals 1)

RGMA1	1.00	RGMA6	0.84
RGMA2	2.00	RGMA7	0.66
RGMA3	2.77	RGMA8	0.84
RGMA4	1.50	RGMA9	1.42
RGMA5	0.90	RGMA10	1.05

* RGMA1 = 2.31kΩ

In case of using 10 levels of g-corrected power supplies (VGMA1 = OPEN)

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage	
00H	0	0	0	0	0	0	V0	VGMA2
01H	0	0	0	0	0	1	V1	VGMA3+(VGMA2-VGMA3)× 6/7
02H	0	0	0	0	1	0	V2	VGMA3+(VGMA2-VGMA3)× 5/7
03H	0	0	0	0	1	1	V3	VGMA3+(VGMA2-VGMA3)× 4/7
04H	0	0	0	1	0	0	V4	VGMA3+(VGMA2-VGMA3)× 3/7
05H	0	0	0	1	0	1	V5	VGMA3+(VGMA2-VGMA3)× 2/7
06H	0	0	0	1	1	0	V6	VGMA3+(VGMA2-VGMA3)× 1/7
07H	0	0	0	1	1	1	V7	VGMA3
08H	0	0	1	0	0	0	V8	VGMA4+(VGMA3-VGMA4)× 7/8
09H	0	0	1	0	0	1	V9	VGMA4+(VGMA3-VGMA4)× 6/8
0AH	0	0	1	0	1	0	V10	VGMA4+(VGMA3-VGMA4)× 5/8
0BH	0	0	1	0	1	1	V11	VGMA4+(VGMA3-VGMA4)× 4/8
0CH	0	0	1	1	0	0	V12	VGMA4+(VGMA3-VGMA4)× 3/8
0DH	0	0	1	1	0	1	V13	VGMA4+(VGMA3-VGMA4)× 2/8
0EH	0	0	1	1	1	0	V14	VGMA4+(VGMA3-VGMA4)× 1/8
0FH	0	0	1	1	1	1	V15	VGMA4
10H	0	1	0	0	0	0	V16	VGMA5+(VGMA4-VGMA5) × 7/8
11H	0	1	0	0	0	1	V17	VGMA5+(VGMA4-VGMA5) × 6/8
12H	0	1	0	0	1	0	V18	VGMA5+(VGMA4-VGMA5) × 5/8
13H	0	1	0	0	1	1	V19	VGMA5+(VGMA4-VGMA5) × 4/8
14H	0	1	0	1	0	0	V20	VGMA5+(VGMA4-VGMA5) × 3/8
15H	0	1	0	1	0	1	V21	VGMA5+(VGMA4-VGMA5) × 2/8
16H	0	1	0	1	1	0	V22	VGMA5+(VGMA4-VGMA5) × 1/8
17H	0	1	0	1	1	1	V23	VGMA5
18H	0	1	1	0	0	0	V24	VGMA6+(VGMA5-VGMA6) × 7/8
19H	0	1	1	0	0	1	V25	VGMA6+(VGMA5-VGMA6) × 6/8
1AH	0	1	1	0	1	0	V26	VGMA6+(VGMA5-VGMA6) × 5/8
1BH	0	1	1	0	1	1	V27	VGMA6+(VGMA5-VGMA6) × 4/8
1CH	0	1	1	1	0	0	V28	VGMA6+(VGMA5-VGMA6) × 3/8
1DH	0	1	1	1	0	1	V29	VGMA6+(VGMA5-VGMA6) × 2/8
1EH	0	1	1	1	1	0	V30	VGMA6+(VGMA5-VGMA6) × 1/8
1FH	0	1	1	1	1	1	V31	VGMA6

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage	
20H	1	0	0	0	0	0	V32	VGMA7+(VGMA6-VGMA7) × 7/8
21H	1	0	0	0	0	1	V33	VGMA7+(VGMA6-VGMA7) × 6/8
22H	1	0	0	0	1	0	V34	VGMA7+(VGMA6-VGMA7) × 5/8
23H	1	0	0	0	1	1	V35	VGMA7+(VGMA6-VGMA7) × 4/8
24H	1	0	0	1	0	0	V36	VGMA7+(VGMA6-VGMA7) × 3/8
25H	1	0	0	1	0	1	V37	VGMA7+(VGMA6-VGMA7) × 2/8
26H	1	0	0	1	1	0	V38	VGMA7+(VGMA6-VGMA7) × 1/8
27H	1	0	0	1	1	1	V39	VGMA7
28H	1	0	1	0	0	0	V40	VGMA8+(VGMA7-VGMA8) × 7/8
29H	1	0	1	0	0	1	V41	VGMA8+(VGMA7-VGMA8) × 6/8
2AH	1	0	1	0	1	0	V42	VGMA8+(VGMA7-VGMA8) × 5/8
2BH	1	0	1	0	1	1	V43	VGMA8+(VGMA7-VGMA8) × 4/8
2CH	1	0	1	1	0	0	V44	VGMA8+(VGMA7-VGMA8) × 3/8
2DH	1	0	1	1	0	1	V45	VGMA8+(VGMA7-VGMA8) × 2/8
2EH	1	0	1	1	1	0	V46	VGMA8+(VGMA7-VGMA8) × 1/8
2FH	1	0	1	1	1	1	V47	VGMA8
30H	1	1	0	0	0	0	V48	VGMA9+(VGMA8-VGMA9) × 7/8
31H	1	1	0	0	0	1	V49	VGMA9+(VGMA8-VGMA9) × 6/8
32H	1	1	0	0	1	0	V50	VGMA9+(VGMA8-VGMA9) × 5/8
33H	1	1	0	0	1	1	V51	VGMA9+(VGMA8-VGMA9) × 4/8
34H	1	1	0	1	0	0	V52	VGMA9+(VGMA8-VGMA9) × 3/8
35H	1	1	0	1	0	1	V53	VGMA9+(VGMA8-VGMA9) × 2/8
36H	1	1	0	1	1	0	V54	VGMA9+(VGMA8-VGMA9) × 1/8
37H	1	1	0	1	1	1	V55	VGMA9
38H	1	1	1	0	0	0	V56	VGMA10+(VGMA9-VGMA10) × 6/7
39H	1	1	1	0	0	1	V57	VGMA10+(VGMA9-VGMA10) × 5/7
3AH	1	1	1	0	1	0	V58	VGMA10+(VGMA9-VGMA10) × 4/7
3BH	1	1	1	0	1	1	V59	VGMA10+(VGMA9-VGMA10) × 3/7
3CH	1	1	1	1	0	0	V60	VGMA10+(VGMA9-VGMA10) × 2/7
3DH	1	1	1	1	0	1	V61	VGMA10+(VGMA9-VGMA10) × 1/7
3EH	1	1	1	1	1	0	V62	VGMA10
3FH	1	1	1	1	1	1	V63	VGMA11

- RVGMA (γ-Corrected Resistance) Ratio. (If the RGMA2 equals 1)

RGMA1	–	RGMA6	0.42
RGMA2	1.00	RGMA7	0.33
RGMA3	1.39	RGMA8	0.42
RGMA4	0.75	RGMA9	0.71
RGMA5	0.45	RGMA10	0.53

* RGMA2 = 4.62kΩ

In case of using 10 levels of g-corrected power supplies (VGMA2= OPEN)

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage	
00H	0	0	0	0	0	0	V0	VGMA3+(VGMA1-VGMA3)× 7/8
01H	0	0	0	0	0	1	V1	VGMA3+(VGMA1-VGMA3)× 6/8
02H	0	0	0	0	1	0	V2	VGMA3+(VGMA1-VGMA3)× 5/8
03H	0	0	0	0	1	1	V3	VGMA3+(VGMA1-VGMA3)× 4/8
04H	0	0	0	1	0	0	V4	VGMA3+(VGMA1-VGMA3)× 3/8
05H	0	0	0	1	0	1	V5	VGMA3+(VGMA1-VGMA3)× 2/8
06H	0	0	0	1	1	0	V6	VGMA3+(VGMA1-VGMA3)× 1/8
07H	0	0	0	1	1	1	V7	VGMA3
08H	0	0	1	0	0	0	V8	VGMA4+(VGMA3-VGMA4)× 7/8
09H	0	0	1	0	0	1	V9	VGMA4+(VGMA3-VGMA4)× 6/8
0AH	0	0	1	0	1	0	V10	VGMA4+(VGMA3-VGMA4)× 5/8
0BH	0	0	1	0	1	1	V11	VGMA4+(VGMA3-VGMA4)× 4/8
0CH	0	0	1	1	0	0	V12	VGMA4+(VGMA3-VGMA4)× 3/8
0DH	0	0	1	1	0	1	V13	VGMA4+(VGMA3-VGMA4)× 2/8
0EH	0	0	1	1	1	0	V14	VGMA4+(VGMA3-VGMA4)× 1/8
0FH	0	0	1	1	1	1	V15	VGMA4
10H	0	1	0	0	0	0	V16	VGMA5+(VGMA4-VGMA5) × 7/8
11H	0	1	0	0	0	1	V17	VGMA5+(VGMA4-VGMA5) × 6/8
12H	0	1	0	0	1	0	V18	VGMA5+(VGMA4-VGMA5) × 5/8
13H	0	1	0	0	1	1	V19	VGMA5+(VGMA4-VGMA5) × 4/8
14H	0	1	0	1	0	0	V20	VGMA5+(VGMA4-VGMA5) × 3/8
15H	0	1	0	1	0	1	V21	VGMA5+(VGMA4-VGMA5) × 2/8
16H	0	1	0	1	1	0	V22	VGMA5+(VGMA4-VGMA5) × 1/8
17H	0	1	0	1	1	1	V23	VGMA5
18H	0	1	1	0	0	0	V24	VGMA6+(VGMA5-VGMA6) × 7/8
19H	0	1	1	0	0	1	V25	VGMA6+(VGMA5-VGMA6) × 6/8
1AH	0	1	1	0	1	0	V26	VGMA6+(VGMA5-VGMA6) × 5/8
1BH	0	1	1	0	1	1	V27	VGMA6+(VGMA5-VGMA6) × 4/8
1CH	0	1	1	1	0	0	V28	VGMA6+(VGMA5-VGMA6) × 3/8
1DH	0	1	1	1	0	1	V29	VGMA6+(VGMA5-VGMA6) × 2/8
1EH	0	1	1	1	1	0	V30	VGMA6+(VGMA5-VGMA6) × 1/8
1FH	0	1	1	1	1	1	V31	VGMA6

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage	
20H	1	0	0	0	0	0	V32	VGMA7+(VGMA6-VGMA7) × 7/8
21H	1	0	0	0	0	1	V33	VGMA7+(VGMA6-VGMA7) × 6/8
22H	1	0	0	0	1	0	V34	VGMA7+(VGMA6-VGMA7) × 5/8
23H	1	0	0	0	1	1	V35	VGMA7+(VGMA6-VGMA7) × 4/8
24H	1	0	0	1	0	0	V36	VGMA7+(VGMA6-VGMA7) × 3/8
25H	1	0	0	1	0	1	V37	VGMA7+(VGMA6-VGMA7) × 2/8
26H	1	0	0	1	1	0	V38	VGMA7+(VGMA6-VGMA7) × 1/8
27H	1	0	0	1	1	1	V39	VGMA7
28H	1	0	1	0	0	0	V40	VGMA8+(VGMA7-VGMA8) × 7/8
29H	1	0	1	0	0	1	V41	VGMA8+(VGMA7-VGMA8) × 6/8
2AH	1	0	1	0	1	0	V42	VGMA8+(VGMA7-VGMA8) × 5/8
2BH	1	0	1	0	1	1	V43	VGMA8+(VGMA7-VGMA8) × 4/8
2CH	1	0	1	1	0	0	V44	VGMA8+(VGMA7-VGMA8) × 3/8
2DH	1	0	1	1	0	1	V45	VGMA8+(VGMA7-VGMA8) × 2/8
2EH	1	0	1	1	1	0	V46	VGMA8+(VGMA7-VGMA8) × 1/8
2FH	1	0	1	1	1	1	V47	VGMA8
30H	1	1	0	0	0	0	V48	VGMA9+(VGMA8-VGMA9) × 7/8
31H	1	1	0	0	0	1	V49	VGMA9+(VGMA8-VGMA9) × 6/8
32H	1	1	0	0	1	0	V50	VGMA9+(VGMA8-VGMA9) × 5/8
33H	1	1	0	0	1	1	V51	VGMA9+(VGMA8-VGMA9) × 4/8
34H	1	1	0	1	0	0	V52	VGMA9+(VGMA8-VGMA9) × 3/8
35H	1	1	0	1	0	1	V53	VGMA9+(VGMA8-VGMA9) × 2/8
36H	1	1	0	1	1	0	V54	VGMA9+(VGMA8-VGMA9) × 1/8
37H	1	1	0	1	1	1	V55	VGMA9
38H	1	1	1	0	0	0	V56	VGMA10+(VGMA9-VGMA10) × 6/7
39H	1	1	1	0	0	1	V57	VGMA10+(VGMA9-VGMA10) × 5/7
3AH	1	1	1	0	1	0	V58	VGMA10+(VGMA9-VGMA10) × 4/7
3BH	1	1	1	0	1	1	V59	VGMA10+(VGMA9-VGMA10) × 3/7
3CH	1	1	1	1	0	0	V60	VGMA10+(VGMA9-VGMA10) × 2/7
3DH	1	1	1	1	0	1	V61	VGMA10+(VGMA9-VGMA10) × 1/7
3EH	1	1	1	1	1	0	V62	VGMA10
3FH	1	1	1	1	1	1	V63	VGMA11

- RVGMA (γ-Corrected Resistance) Ratio.

(If the sum of RGMA1 and RGMA2 equals 1)

RGMA1	1.00	RGMA6	0.37
RGMA2		RGMA7	0.29
RGMA3	1.21	RGMA8	0.37
RGMA4	0.66	RGMA9	0.62
RGMA5	0.39	RGMA10	0.46

RGMA1 + RGMA2 = 5.28kΩ

In case of using 9 levels of g-corrected power supplies (VGMA2, VGMA10= OPEN)

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage	
00H	0	0	0	0	0	0	V0	VGMA3+(VGMA1-VGMA3)× 7/8
01H	0	0	0	0	0	1	V1	VGMA3+(VGMA1-VGMA3)× 6/8
02H	0	0	0	0	1	0	V2	VGMA3+(VGMA1-VGMA3)× 5/8
03H	0	0	0	0	1	1	V3	VGMA3+(VGMA1-VGMA3)× 4/8
04H	0	0	0	1	0	0	V4	VGMA3+(VGMA1-VGMA3)× 3/8
05H	0	0	0	1	0	1	V5	VGMA3+(VGMA1-VGMA3)× 2/8
06H	0	0	0	1	1	0	V6	VGMA3+(VGMA1-VGMA3)× 1/8
07H	0	0	0	1	1	1	V7	VGMA3
08H	0	0	1	0	0	0	V8	VGMA4+(VGMA3-VGMA4)× 7/8
09H	0	0	1	0	0	1	V9	VGMA4+(VGMA3-VGMA4)× 6/8
0AH	0	0	1	0	1	0	V10	VGMA4+(VGMA3-VGMA4)× 5/8
0BH	0	0	1	0	1	1	V11	VGMA4+(VGMA3-VGMA4)× 4/8
0CH	0	0	1	1	0	0	V12	VGMA4+(VGMA3-VGMA4)× 3/8
0DH	0	0	1	1	0	1	V13	VGMA4+(VGMA3-VGMA4)× 2/8
0EH	0	0	1	1	1	0	V14	VGMA4+(VGMA3-VGMA4)× 1/8
0FH	0	0	1	1	1	1	V15	VGMA4
10H	0	1	0	0	0	0	V16	VGMA5+(VGMA4-VGMA5) × 7/8
11H	0	1	0	0	0	1	V17	VGMA5+(VGMA4-VGMA5) × 6/8
12H	0	1	0	0	1	0	V18	VGMA5+(VGMA4-VGMA5) × 5/8
13H	0	1	0	0	1	1	V19	VGMA5+(VGMA4-VGMA5) × 4/8
14H	0	1	0	1	0	0	V20	VGMA5+(VGMA4-VGMA5) × 3/8
15H	0	1	0	1	0	1	V21	VGMA5+(VGMA4-VGMA5) × 2/8
16H	0	1	0	1	1	0	V22	VGMA5+(VGMA4-VGMA5) × 1/8
17H	0	1	0	1	1	1	V23	VGMA5
18H	0	1	1	0	0	0	V24	VGMA6+(VGMA5-VGMA6) × 7/8
19H	0	1	1	0	0	1	V25	VGMA6+(VGMA5-VGMA6) × 6/8
1AH	0	1	1	0	1	0	V26	VGMA6+(VGMA5-VGMA6) × 5/8
1BH	0	1	1	0	1	1	V27	VGMA6+(VGMA5-VGMA6) × 4/8
1CH	0	1	1	1	0	0	V28	VGMA6+(VGMA5-VGMA6) × 3/8
1DH	0	1	1	1	0	1	V29	VGMA6+(VGMA5-VGMA6) × 2/8
1EH	0	1	1	1	1	0	V30	VGMA6+(VGMA5-VGMA6) × 1/8
1FH	0	1	1	1	1	1	V31	VGMA6

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage	
20H	1	0	0	0	0	0	V32	VGMA7+(VGMA6-VGMA7) × 7/8
21H	1	0	0	0	0	1	V33	VGMA7+(VGMA6-VGMA7) × 6/8
22H	1	0	0	0	1	0	V34	VGMA7+(VGMA6-VGMA7) × 5/8
23H	1	0	0	0	1	1	V35	VGMA7+(VGMA6-VGMA7) × 4/8
24H	1	0	0	1	0	0	V36	VGMA7+(VGMA6-VGMA7) × 3/8
25H	1	0	0	1	0	1	V37	VGMA7+(VGMA6-VGMA7) × 2/8
26H	1	0	0	1	1	0	V38	VGMA7+(VGMA6-VGMA7) × 1/8
27H	1	0	0	1	1	1	V39	VGMA7
28H	1	0	1	0	0	0	V40	VGMA8+(VGMA7-VGMA8) × 7/8
29H	1	0	1	0	0	1	V41	VGMA8+(VGMA7-VGMA8) × 6/8
2AH	1	0	1	0	1	0	V42	VGMA8+(VGMA7-VGMA8) × 5/8
2BH	1	0	1	0	1	1	V43	VGMA8+(VGMA7-VGMA8) × 4/8
2CH	1	0	1	1	0	0	V44	VGMA8+(VGMA7-VGMA8) × 3/8
2DH	1	0	1	1	0	1	V45	VGMA8+(VGMA7-VGMA8) × 2/8
2EH	1	0	1	1	1	0	V46	VGMA8+(VGMA7-VGMA8) × 1/8
2FH	1	0	1	1	1	1	V47	VGMA8
30H	1	1	0	0	0	0	V48	VGMA9+(VGMA8-VGMA9) × 7/8
31H	1	1	0	0	0	1	V49	VGMA9+(VGMA8-VGMA9) × 6/8
32H	1	1	0	0	1	0	V50	VGMA9+(VGMA8-VGMA9) × 5/8
33H	1	1	0	0	1	1	V51	VGMA9+(VGMA8-VGMA9) × 4/8
34H	1	1	0	1	0	0	V52	VGMA9+(VGMA8-VGMA9) × 3/8
35H	1	1	0	1	0	1	V53	VGMA9+(VGMA8-VGMA9) × 2/8
36H	1	1	0	1	1	0	V54	VGMA9+(VGMA8-VGMA9) × 1/8
37H	1	1	0	1	1	1	V55	VGMA9
38H	1	1	1	0	0	0	V56	VGMA11+(VGMA9-VGMA11) × 7/8
39H	1	1	1	0	0	1	V57	VGMA11+(VGMA9-VGMA11) × 6/8
3AH	1	1	1	0	1	0	V58	VGMA11+(VGMA9-VGMA11) × 5/8
3BH	1	1	1	0	1	1	V59	VGMA11+(VGMA9-VGMA11) × 4/8
3CH	1	1	1	1	0	0	V60	VGMA11+(VGMA9-VGMA11) × 3/8
3DH	1	1	1	1	0	1	V61	VGMA11+(VGMA9-VGMA11) × 2/8
3EH	1	1	1	1	1	0	V62	VGMA11+(VGMA9-VGMA11) × 1/8
3FH	1	1	1	1	1	1	V63	VGMA11

- RVGMA (γ-Corrected Resistance) RATIO.

(If the sum of RGMA1 and RGMA2 equals 1)

RGMA1	1.00	RGMA6	0.37
RGMA2		RGMA7	0.29
RGMA3	1.21	RGMA8	0.37
RGMA4	0.66	RGMA9	0.71
RGMA5	0.39	RGMA10	

RGMA1 + RGMA2 = 5.28kΩ