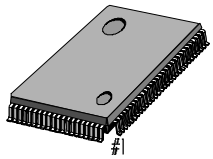
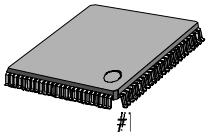
INTRODUCTION

The KS0086 is an LCD driver LSI which is fabricated by low power CMOS high voltage process technology.
In segment driver mode, it can be interfaced in 1-bit serial or 4-bit parallel method by the controller.
In common driver mode, dual type mode is applicable. And in segment mode application, the power down function reduces power consumption.

100 QFP-1420C



100 TQFP-1414



FEATURES

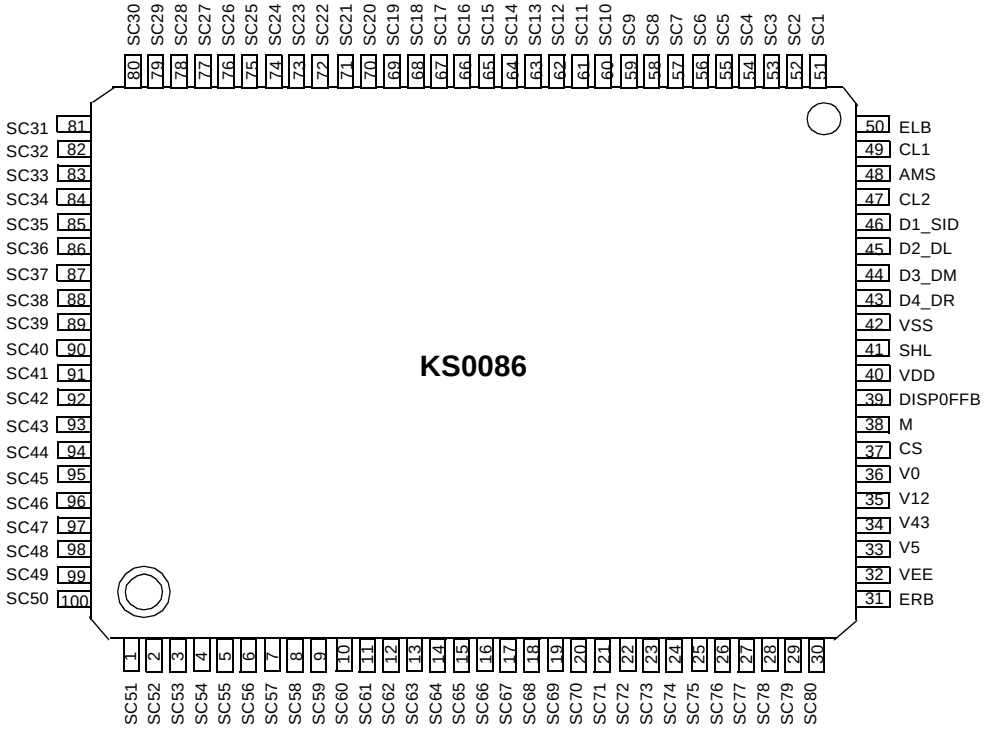
- Power supply voltage : +5 V ± 10 %, + 3 V ± 10 %
- Supply voltage for display : 6 to 28 V (VDD-VEE)
- 4-bit parallel/1-bit serial data processing (in segment mode).
- Single mode operation / dual mode operation (in common mode).
- Power down function (in segment mode).
- Applicable LCD duty : 1/64 ~ 1/256
- Interface

DRIVER	
COM (cascade)	SEG (cascade)
KS0086	KS0086

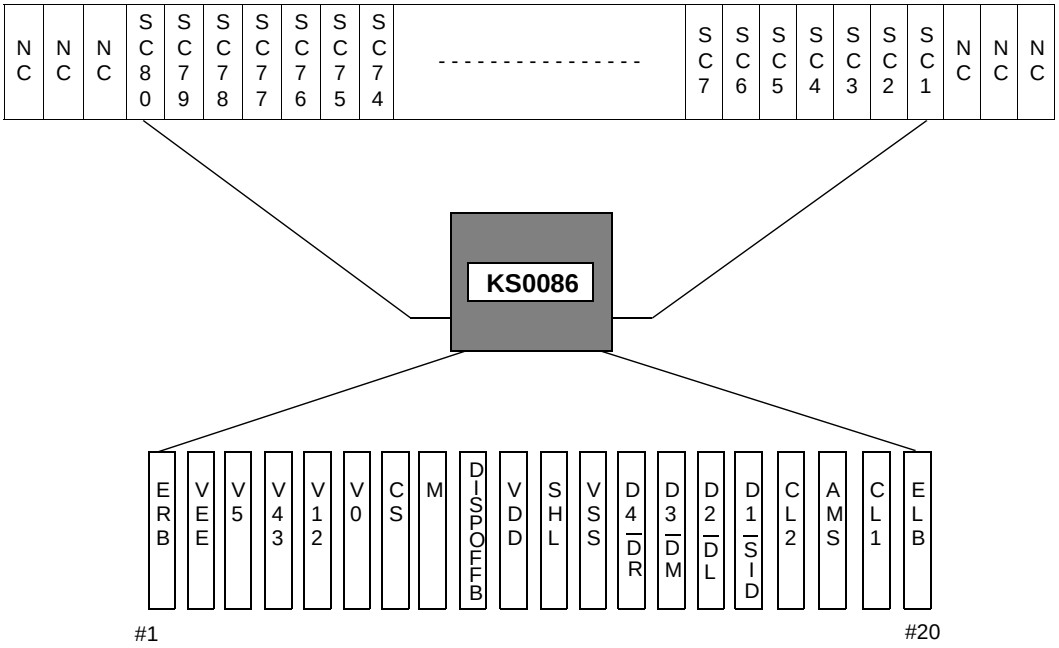
- High voltage CMOS process
- Available PKG type : bare chip, 100-QFP, 100-TQFP and 100-TAB.

PACKAGE INFORMATION

KS0086
PKG TYPE
100QFP PACKAGE



KS0086TB
PKG TYPE
100TCP PACKAGE

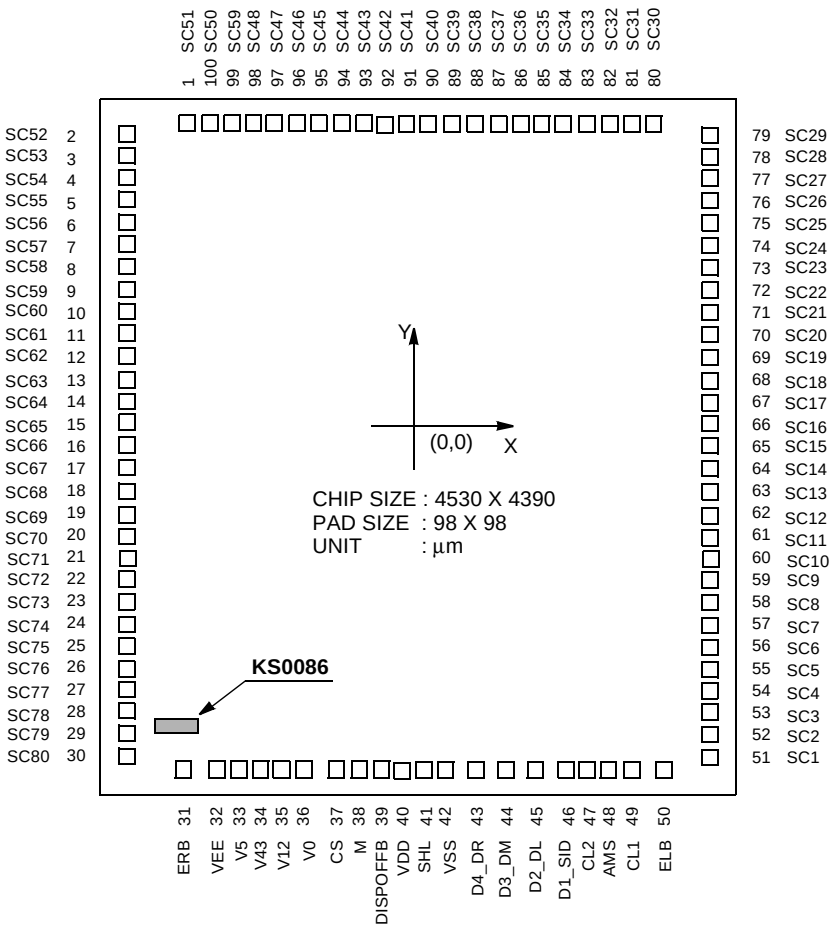


* PKG TYPE = 100 - TAB - 35 mm

* INPUT LEAD PITCH = 0.80 mm

* OUTPUT LEAD PITCH = 0.22 mm

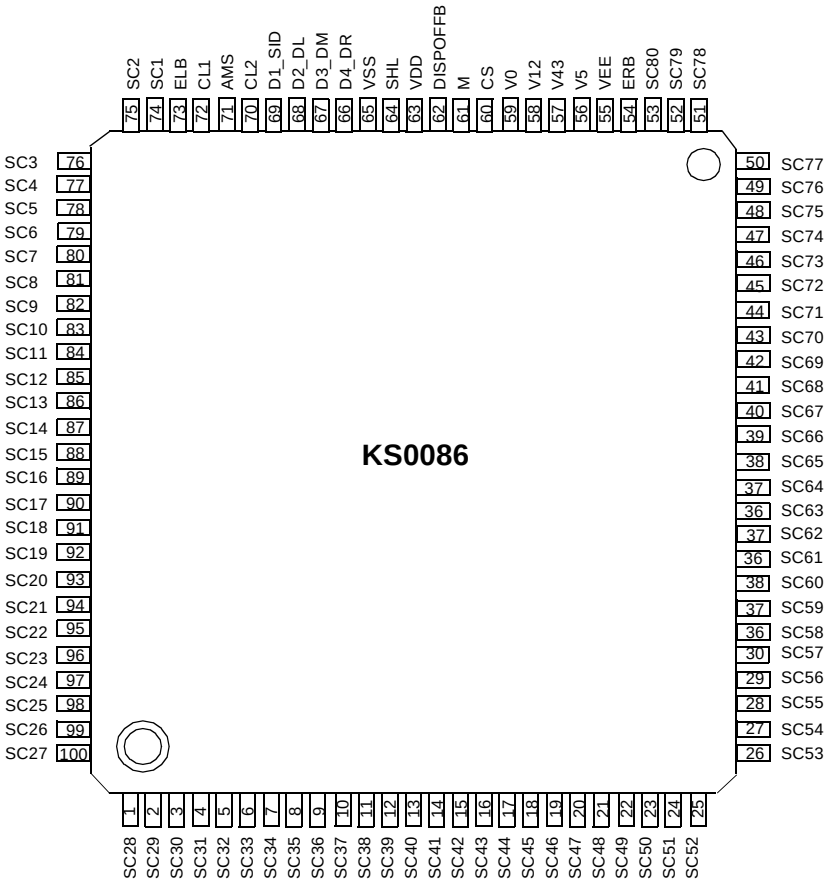
PAD DIAGRAM (KS0086/KS0086TB))



PAD LOCATION (KS0086/KS0086TB)

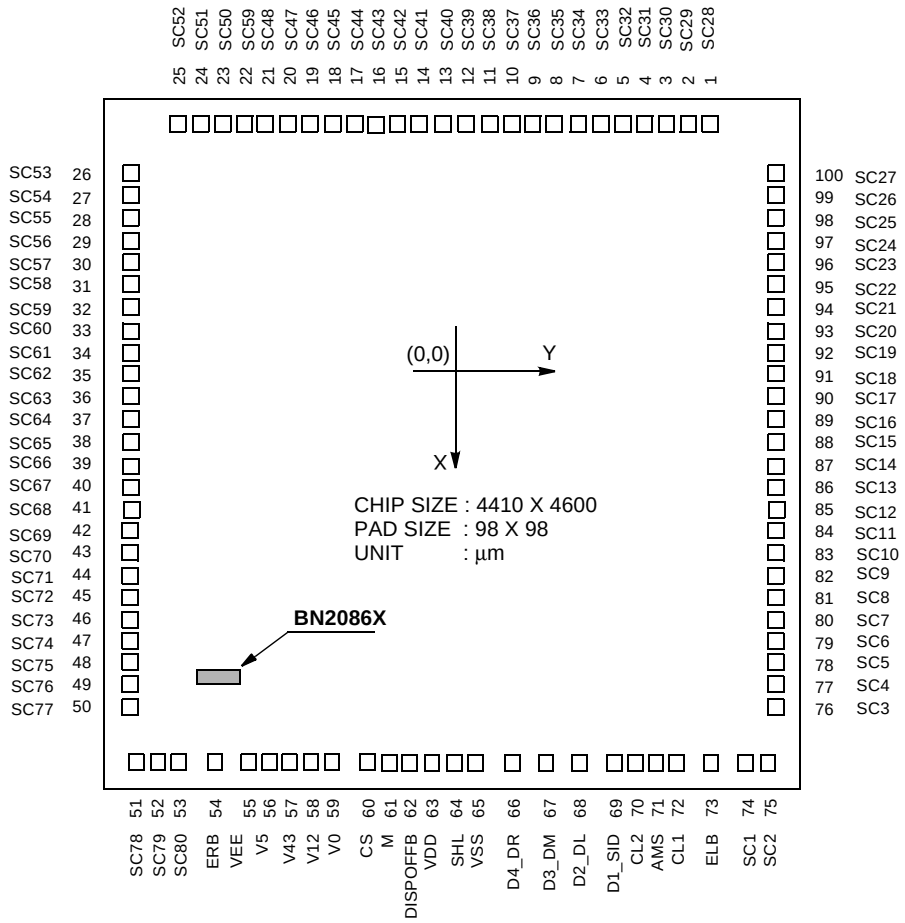
PAD NO.	PAD NAME	COORDINATES		PAD NO.	PAD NAME	COORDINATES		PAD NO.	PAD NAME	COORDINATES	
		X	Y			X	Y			X	Y
1	SC51	-1690	1959	35	V12	-900	-1959	69	SC19	2029	544
2	SC52	-2029	1884	36	V0	-775	-1959	70	SC20	2029	678
3	SC53	-2029	1750	37	CS	-600	-1959	71	SC21	2029	812
4	SC54	-2029	1616	38	M	-475	-1959	72	SC22	2029	946
5	SC55	-2029	1482	39	DISPOFFB	-350	-1959	73	SC23	2029	1080
6	SC56	-2029	1348	40	VDD	-225	-1959	74	SC24	2029	1214
7	SC57	-2029	1214	41	SHL	-100	-1959	75	SC25	2029	1348
8	SC58	-2029	1080	42	VSS	25	-1959	76	SC26	2029	1482
9	SC59	-2029	946	43	D4_DR	266	-1959	77	SC27	2029	1616
10	SC60	-2029	812	44	D3_DM	470	-1959	78	SC28	2029	1750
11	SC61	-2029	678	45	D2_DL	711	-1959	79	SC29	2029	1884
12	SC62	-2029	544	46	D1_SID	915	-1959	80	SC30	1690	1959
13	SC63	-2029	410	47	CL2	1040	-1959	81	SC31	1529	1959
14	SC64	-2029	276	48	ELB	1165	-1959	82	SC32	1368	1959
15	SC65	-2029	142	49	CL1	1290	-1959	83	SC33	1207	1959
16	SC66	-2029	8	50	ELB	1496	-1959	84	SC34	1046	1959
17	SC67	-2029	-126	51	SC1	2029	-1884	85	SC35	885	1959
18	SC68	-2029	-260	52	SC2	2029	-1735	86	SC36	724	1959
19	SC69	-2029	-394	53	SC3	2029	-1601	87	SC37	563	1959
20	SC70	-2029	-528	54	SC4	2029	-1467	88	SC38	402	1959
21	SC71	-2029	-662	55	SC5	2029	-1333	89	SC39	241	1959
22	SC72	-2029	-797	56	SC6	2029	-1199	90	SC40	80	1959
23	SC73	-2029	-931	57	SC7	2029	-1065	91	SC41	-80	1959
24	SC74	-2029	-1065	58	SC8	2029	-931	92	SC42	-241	1959
25	SC75	-2029	-1199	59	SC9	2029	-797	93	SC43	-402	1959
26	SC76	-2029	-1333	60	SC10	2029	-662	94	SC44	-563	1959
27	SC77	-2029	-1467	61	SC11	2029	-528	95	SC45	-724	1959
28	SC78	-2029	-1601	62	SC12	2029	-394	96	SC46	-885	1959
29	SC79	-2029	-1735	63	SC13	2029	-260	97	SC47	-1046	1959
30	SC80	-2029	-1884	64	SC14	2029	-126	98	SC48	-1207	1959
31	ERB	-1479	-1959	65	SC15	2029	8	99	SC49	-1368	1959
32	VEE	-1275	-1959	66	SC16	2029	142	100	SC50	-1529	1959
33	V5	-1150	-1959	67	SC17	2029	276				
34	V43	-1025	-1959	68	SC18	2029	410				

KS0086TQ
PKG TYPE
100TQFP PACKAGE



* PKG TYPE = 100 - TQFP - 1414
* PKG THICKNESS = 1.00 (± 0.05) mm
* PKG SIZE = 14.00 (± 0.10) X 14.00 (± 0.10) mm
* PAD PITCH = 0.5 mm
* PAD WIDTH = 0.20 (+ 0, 07, -0.03) mm
* PAD LENGTH = 1.00 (± 0.1) mm

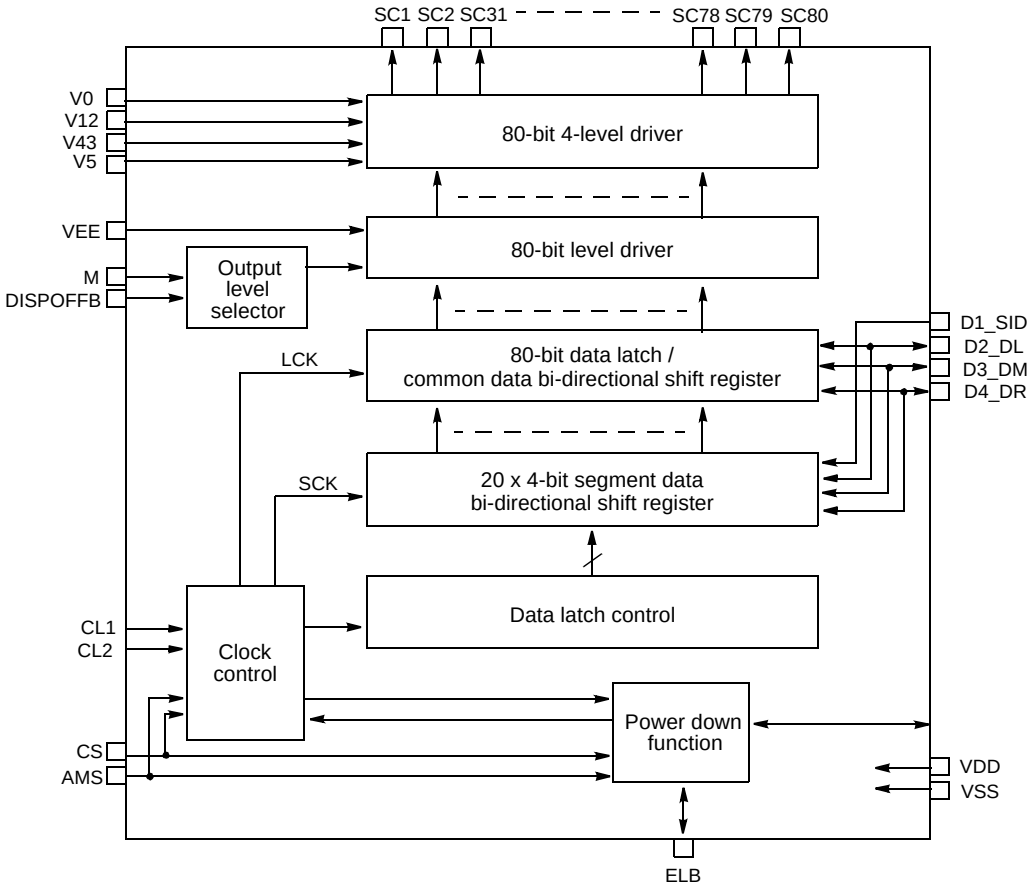
PAD DIAGRAM (KS0086TQ)



PAD LOCATION (KS0086TQ)

PAD NO.	PAD NAME	COORDINATES		PAD NO.	PAD NAME	COORDINATES		PAD NO.	PAD NAME	COORDINATES	
		X	Y			X	Y			X	Y
1	SC28	-1969	1691	35	SC62	-515	-2064	69	D1_SID	1969	924
2	SC29	-1969	1551	36	SC63	-390	-2064	70	CL2	1969	1049
3	SC30	-1969	1411	37	SC64	-265	-2064	71	AMS	1969	1174
4	SC31	-1969	1271	38	SC65	-140	-2064	72	CL1	1969	1299
5	SC32	-1969	1131	39	SC66	-15	-2064	73	ELB	1969	1504
6	SC33	-1969	991	40	SC67	110	-2064	74	SC1	1969	1904
7	SC34	-1969	851	41	SC68	235	-2064	75	SC2	1969	2029
8	SC35	-1969	711	42	SC69	360	-2064	76	SC3	1360	2064
9	SC36	-1969	571	43	SC70	485	-2064	77	SC4	1235	2064
10	SC37	-1969	431	44	SC71	610	-2064	78	SC5	1110	2064
11	SC38	-1969	291	45	SC72	735	-2064	79	SC6	985	2064
12	SC39	-1969	151	46	SC73	860	-2064	80	SC7	860	2064
13	SC40	-1969	11	47	SC74	985	-2064	81	SC8	735	2064
14	SC41	-1969	-151	48	SC75	1110	-2064	82	SC9	610	2064
15	SC42	-1969	-291	49	SC76	1235	-2064	83	SC10	485	2064
16	SC43	-1969	-431	50	SC77	1360	-2064	84	SC11	360	2064
17	SC44	-1969	-571	51	SC78	1969	-2029	85	SC12	235	2064
18	SC45	-1969	-711	52	SC79	1969	-1904	86	SC13	110	2064
19	SC46	-1969	-851	53	SC80	1969	-1779	87	SC14	-15	2064
20	SC47	-1969	-991	54	ERB	1969	-1475	88	SC15	-140	2064
21	SC48	-1969	-1131	55	VEE	1969	-1270	89	SC16	-265	2064
22	SC49	-1969	-1271	56	V5	1969	-1145	90	SC17	-390	2064
23	SC50	-1969	-1411	57	V43	1969	-1020	91	SC18	-515	2064
24	SC51	-1969	-1551	58	V12	1969	-895	92	SC19	-640	2064
25	SC52	-1969	-1691	59	V0	1969	-770	93	SC20	-765	2064
26	SC53	-1640	-2064	60	CS	1969	-595	94	SC21	-890	2064
27	SC54	-1515	-2064	61	M	1969	-470	95	SC22	-1015	2064
28	SC55	-1390	-2064	62	DISPOFFB	1969	-345	96	SC23	-1140	2064
29	SC56	-1265	-2064	63	VDD	1969	-220	97	SC24	-1265	2064
30	SC57	-1140	-2064	64	SHL	1969	-95	98	SC25	-1390	2064
31	SC58	-1015	-2064	65	VSS	1969	30	99	SC26	-1515	2064
32	SC59	-890	-2064	66	D4_DR	1969	272	100	SC27	-1640	2064
33	SC60	-765	-2064	67	D3_DM	1969	477				
34	SC61	-640	-2064	68	D2_DL	1969	719				

BLOCK DIAGRAM



BLOCK DESCRIPTION

Name	Function	COM/ SEG
Clock control	Generates latch clock (LCK), shift clock (SCK) and control clock timing according to the input of CL1, CL2 and control inputs (CS, AMS). In common driver application mode, this block generates the shift clock (LCK) for the common data I-directional shift register.	COM/ SEG
Data latch control	Determines the direction of segment data shift, and input data of each I-directional shift register. In 4-bit segment data parallel transfer mode, data is shifted by a 4-bit unit. In common driver application mode, data is transferred to the common data shift register directly, which disables this block.	SEG
Power down function	Controls the clock enable state of the current driver according to the input value of enable pin (ELB or ERB). If enable input value is “Low”, every clock of the current driver is enabled and the clock control block works. But if enable input is “High”, current driver is disabled and the input data value has no effect on the output level. So power consumption can be lowered.	SEG
Output level selector	Controls the output voltage level according to the input control pin (M and DISPOFFB) (refer to PIN DESCRIPTION).	COM/ SEG
20x4-bit segment data I-directional shift register	Stores output data value by shifting the input values. In 1-bit serial interface mode application, all 80 shift clocks (SCK) are needed to store all the display data. But in 4-bit parallel transfer mode application, only 20 clocks are needed. In common driver application mode, this block does not work.	SEG
80-bit data latch/common data I-directional shift register	In segment driver application mode, the data from the 20x4-bit segment data shift register are latched for segment driver output. In single-type common driver application,1-bit input data (from DL or DR pin) is shifted and latched by the direction according to the SHL signal input. In dual-type common application mode, 80-bit registers are divided by two blocks and controlled independently (refer to NOTE 3).	COM/ SEG
80-bit level shifter	Voltage level shifter block for high voltage part. The inputs of this block are of logical voltage level and the outputs of this block are at high voltage level value. These values are input in to the driver.	SEG
80-bit 4-level driver	Selects the output voltage level according to M and latched data value. If the data value is "High" the driver output is at selected voltage level (V0 or V5), and in the reverse case the driver output value is at the non-selected level (V12 or V43). In segment driver application mode, non-selected output value is V2 or V3. and when in common driver application, this value becomes V1 or V4.	SEG

PIN DESCRIPTION

<table>
<tr><th>Pin</th><th>Input
Output</th><th>Name</th><th>Function</th><th>Interface</th></tr>
<tr><td>VDD</td><td rowspan="3"></td><td rowspan="3">Power
supply</td><td>Logical "High" input port (+5 V ± 10%, +3 V ± 10%)</td><td rowspan="3">Power</td></tr>
<tr><td>VSS</td><td>0 V (GND)</td></tr>
<tr><td>VEE</td><td>Logical "Low" for high voltage part</td></tr>
<tr><td>V0, V12,
V43, V5</td><td>Input</td><td>LCD driver
output
voltage level</td><td>Bias supply voltage input to drive the LCD.
Bias voltage divided by the resistance is usually used as a supply voltage source (refer to NOTE 2).</td><td>Power</td></tr>
<tr><td>SC1
~
SC80</td><td>Output</td><td>LCD driver
output</td><td>Display data output pin which corresponds to the respective latch contents.
One of V0, V12, V34 and V5 is selected as a display driving voltage source according to the combination of the latched data level and M signal (refer to NOTE 1).</td><td>LCD</td></tr>
<tr><td>CL2</td><td>Input</td><td>Data shift
clock</td><td>Clock pulse input for the bi-directional shift register.
- In segment driver application mode, the data is shifted to 20 x 4-bit segment data shift register at the falling edge of this clock pulse. The clock pulse, which was input when the enable bit (ELB/ERB) is in not active condition, is invalid.
- In common driver application mode, the data is shifted to 80-bit common data bi-directional shift register by the
CL1 clock. Hence, this clock pin is not used (Open or connect this pin to VDD).</td><td>Controller</td></tr>
<tr><td>M</td><td>Input</td><td>AC signal
for LCD
driver output</td><td>Alternate signal input pin for LCD driving.
Normal frame inversion signal is input in to this pin.</td><td>Controller</td></tr>
<tr><td>CL1</td><td>Input</td><td>Data latch
clock</td><td>- In segment driver application mode, this signal is used for latching the shift register contents at the falling edge of this clock pulse. CL1 pulse "High" level initializes power-down function block.
- In common driver application mode, CL1 is used as a shifting clock of common output data.</td><td>Controller</td></tr>
<tr><td>DISPOFFB</td><td>Input</td><td>Display off
control</td><td>Control input pin to fix the driver output (SC1~SC80) to V0 level, during "Low" value input. LCD becomes non-selected by V0 level output from every output of segment drivers and every output of common drivers.</td><td>Controller</td></tr>
<tr><td>CS</td><td>Input</td><td>COM/SEG
mode
control</td><td>When CS = "Low", KS0086 is used as an 80-bit segment driver.
When CS = "High", KS0086 is set to an 80-bit common driver</td><td>VDD/VSS</td></tr>
<tr><td>AMS</td><td>Input</td><td>Application
mode select</td><td>According to the input value of the AMS and the CS pin, application mode of KS0086 is differs as shown below.
<table>
<tr><th>CS</th><th>AMS</th><th>Application mode</th><th>COM/SEG</th></tr>
<tr><td>0</td><td>0</td><td>4-bit parallel interface mode</td><td rowspan="2">SEG</td></tr>
<tr><td>0</td><td>1</td><td>1-bit serial interface mode</td></tr>
<tr><td>1</td><td>0</td><td>single-type application mode</td><td rowspan="2">COM</td></tr>
<tr><td>1</td><td>1</td><td>dual-type application mode</td></tr>
</table></td><td>VDD/VSS</td></tr>
</table>

PIN DESCRIPTION (continued)

<table>
<tr><th>Pin</th><th>Input
Output</th><th>Name</th><th>Function</th><th>Interface</th></tr>
<tr><td>D1_SID,
D2_DL,
D3_DM,
D4_DR</td><td>Input/
Output</td><td>Display data input / serial input data / left, right data input output</td><td>- In segment driver application mode, these pins are used as 4-bit data input pin (when 4-bit parallel interface mode : AMS = "Low"), or D1_SID is used as serial data input pin and other pins are not used (connect these to VDD) (when 1-bit serial interface mode : AMS = "High").
- In common driver application mode, the data is shifted from D2_DL(D4_DR) to D4_DR(D2_DL), when in single type interface mode (AMS = "Low"). In dual-type application case, the data are shifted from D2_DL and D3_DM (D4_DR and D3_DM) to D4_DR(D2_DL). In each case the direction of the data shift and the connection of data pins are determined by SHL input (refer to NOTE 3, NOTE 4).</td><td>Controller</td></tr>
<tr><td>SHL</td><td>Input</td><td>Shift direc-tion control</td><td>When SHL = "Low", data is shifted from left to right.
When SHL = "High", the direction is reversed. (refer to NOTE3)</td><td>VDD/VSS</td></tr>
<tr><td>ELB, ERB</td><td>Input/
Output</td><td>Enable data input/output</td><td>- In segment driver application mode, the internal operation is enabled only when enable input (ELB or ERB) is "Low" (power down function). When several drivers are serially connected, the enable state of each driver is shifted according to the SHL input. Connect these pins as below.
- In common driver application mode, power down function is not used.
Open these pins.
<table>
<tr><th rowspan="2">SHL</th><th colspan="2">SEGMENT DRIVER</th></tr>
<tr><th>ELB</th><th>ERB</th></tr>
<tr><td>L</td><td>Output
(open)</td><td>Input
(VSS)</td></tr>
<tr><td>H</td><td>Input
(VSS)</td><td>Output
(open)</td></tr>
</table></td><td>-</td></tr>
</table>

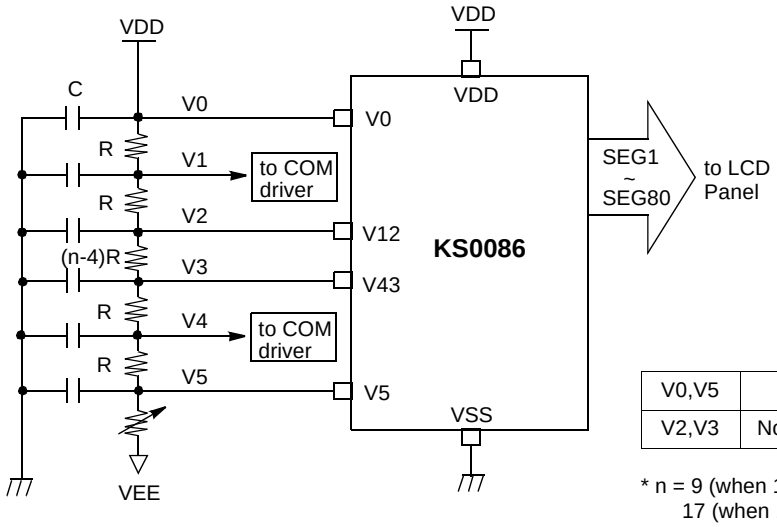
NOTE 1. Output level control

"X" : don't care

M	Latched data	DISPOFFB	Output level (SC1 ~ SC80)	
			SEG Mode	COM Mode
L	L	H	V12(V2)	V12(V1)
L	H	H	V0	V5
H	L	H	V43(V3)	V43(V4)
H	H	H	V5	V0
X	X	L	V0	V0

NOTE 2. LCD driving voltage application circuit

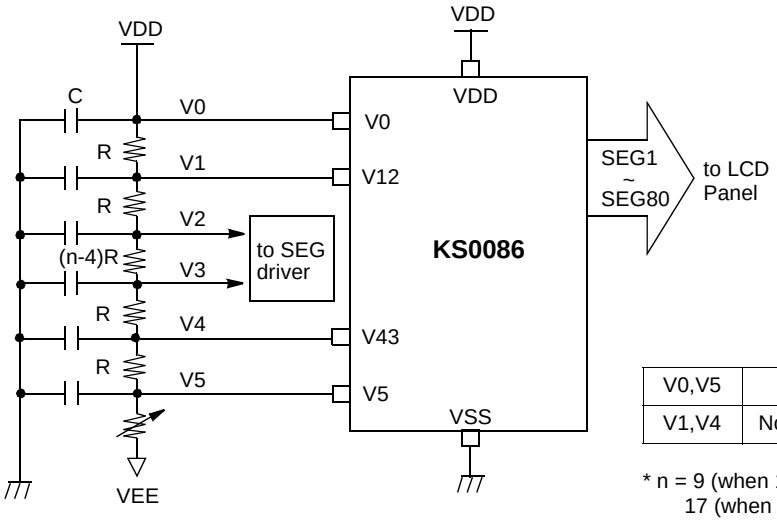
(1) Segment driver application (CS = “Low”)



V0,V5	Selection level
V2,V3	Non-selection level

* n = 9 (when 1/64 duty) to
17 (when 1/256 duty)

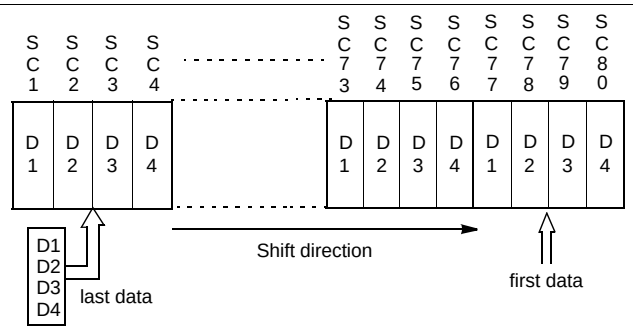
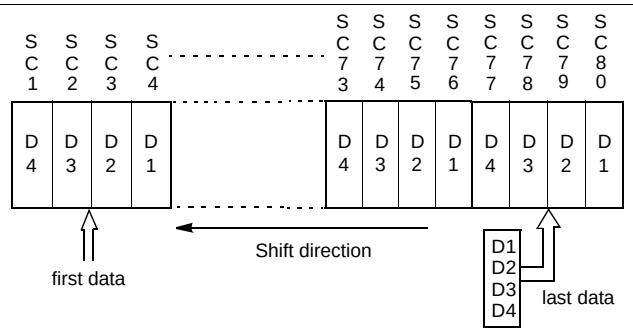
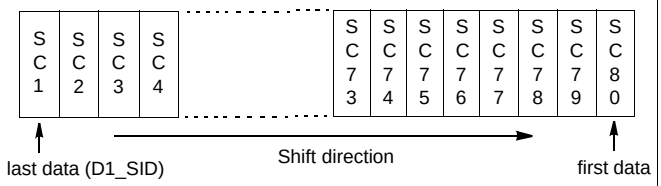
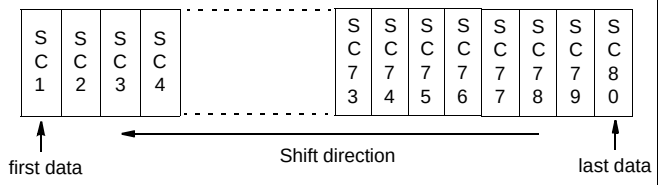
(2) Common driver application (CS = “High”)



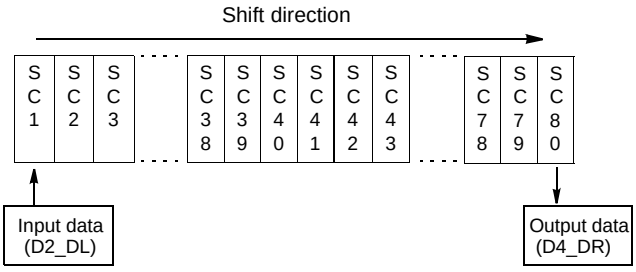
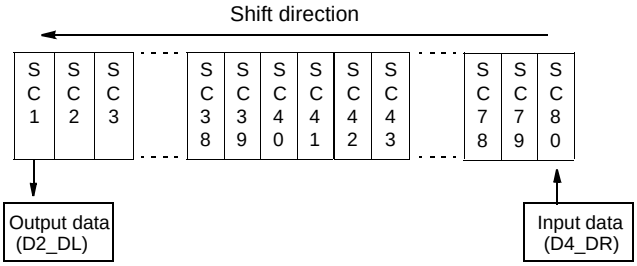
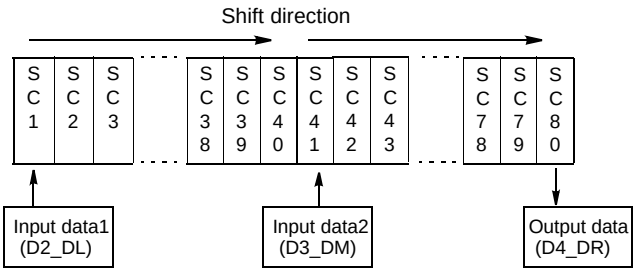
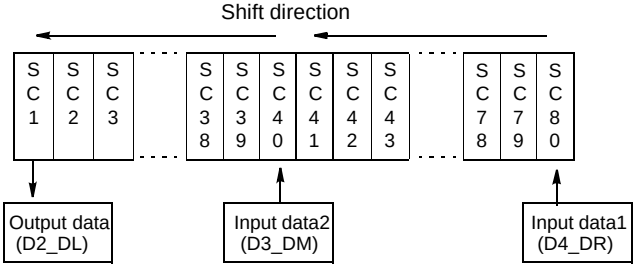
V0,V5	Selection level
V1,V4	Non-selection level

* n = 9 (when 1/64 duty) to
17 (when 1/256 duty)

NOTE 3. Data shift direction according to control signals
(1) When CS = “Low” (segment driver application)

AMS	SHL	Application mode	Data direction	Input pin
L	L	4-bit parallel data transfer mode (SEG)		D1_SID, D2_DL, D3_DM, D4_DR
	H			
H	L	1-bit serial data transfer mode (SEG)		D1 _SID
	H			

(2) When CS = “High” (common driver application)

AMS	SHL	Application mode	Data direction	Input pin
L	L	single-type application mode (COM)		D2_DL
	H			D4_DR
L	L	dual-type application mode (COM)		D2_DL, D3_DM
	H			D4_DR, D3_DM

NOTE 4. Usage of data pins

* X = don't care

COM/SEG (CS pin)	Application mode (AMS pin)	SHL	Data interface pin			
			D1_SID	D2_DL	D3_DM	D4_DR
SEG (CS = "Low")	4-bit parallel interface mode (AMS = "Low")	X	D1 (input)	D2 (input2)	D3 (input3)	D4 (input4)
	1-bit serial interface mode (AMS = "High")	X	SID (input)	Connect to VDD		
COM (CS = "High")	single-type application mode (AMS = "Low")	L	open	DL (input)	open	DR (output)
		H		DL (output)		DR (input)
	dual-type application mode (AMS = "High")	L	open	DL (input1)	DM (input2)	DR (output2)
		H		DL (output2)	DM (input2)	DR (input1)

MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit
Power supply voltage	V_{DD}	-0.3 ~ +7.0	V
Driver supply voltage	V_{LCD}	0 ~ +30	
Input voltage	V_{IN}	-0.3 ~ V_{DD} + 0.3	
Operating temperature	Topr	-30 ~ +85	^{o}C
Storage temperature	Tstg	-55 ~ +150	

* NOTE: Voltage greater than above may do damage to the circuit.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(1) SEGMENT DRIVER APPLICATION

(Vss = 0V, Ta = -30 ~ +85°C)

Characteristic	Symbol	Test Condition		MIN	TYP	MAX	Unit
Operating voltage1	V_{DD}	-		2.7	-	5.5	V
	V_{LCD}	V_{IN} = VDD - VEE		6	-	28	
Input voltage (*1)	V_{IH}	-		0.8VDD	-	VDD	
	V_{IL}	-		0	-	0.2VDD	
Output voltage (*2)	V_{OH}	I_{OH} = -0.4 mA		VDD-0.4	-	-	V
	V_{OL}	I_{OL} = 0.4 mA		-	-	0.4	
Input leakage current 1(*1)	I_{IL1}	V_{IN} = VDD to VSS		-10	-	10	µA
Input leakage current 2(*3)	I_{IL2}	V_{IN} = VDDto VEE		-25	-	25	
On resistance (*4)	R_{ON}	I_{ON} = 100 µA		-	2	4	KΩ
Supply current (*5)	I_{STBY}	f_{CL1}=32 kHz M=VSS	VSS pin	-	-	100	µA
	I_{DD}	f_{CL1}=32 kHz f_M=80 Hz	VDD=5 V	-	-	5	mA
			VDD=3 V	-	-	2	
	I_{EE}		VDD=5 V	-	-	500	µA

NOTES
(*1) Applied to CL1, CL2, ELB, ERB, D1_SID ~ D4_DR, SHL, DISPOFFB, M, CS, AMS pin
(*2) ELB, ERB pin
(*3) V0, V12, V43, V5 pin
(*4) VLCD=VDD-VEE, V0=VDD=5 V, V5=VEE=-23 V
V12=VDD-2/n(VLCD), V43=VEE+2/n(VLCD), n = 17 (1/256 duty, 1/17 bias)
(*5) V0=VDD, V12=1.71 V(VDD=5V) or -0.06 V(VDD=3 V),
V43=-19.71 V(VDD=5 V) or -19.94 V(VDD=3 V), V5=VEE=-23 V, no-load condition (1/256 duty, 1/17 bias)
4-bit parallel interface mode
I_{STBY} : VDD=5 V, fCL2=5.12 MHz, SHL=VSS, DISPOFFB=VDD, M=VSS, display data pattern = 0000
I_{DD} : VDD=3 V, f_{CL2}=4 MHz, display data pattern = 0101
VDD=5 V, f_{CL2}=5.12 MHz, display data pattern = 0101
I_{EE} : VDD=5 V, f_{CL2}=5.12 MHz, display data pattern = 0101, VEE pin

DC CHARACTERISTICS (continued)
(2) COMMON DRIVER APPLICATION

(Vss = 0 V, Ta = -30 ~ +85°C)

Characteristic	Symbol	Test Condition		MIN	TYP	MAX	Unit
Operating voltage	VDD	-		2.7	-	5.5	V
	V_{LCD}	V_{IN} = VDD - VEE		6	-	28	
Input voltage (*1)	V_{IH}	-		0.8VDD	-	VDD	
	V_{IL}	-		0	-	0.2VDD	
Output voltage (*3)	V_{OH}	I_{OH} = -0.4 mA		VDD-0.4	-	-	V
	V_{OL}	I_{OL} = 0.4 mA		-	-	0.4	
Input leakage current 1(*1)	I_{IL1}	V_{IN} = VDD to VSS		-10	-	10	μA
Input leakage current 2(*2)	I_{IL2}	V_{IN} = 0 V, VDD = 5 V (PULL UP)		-50	-125	-250	
Input leakage current 3(*4)	I_{IL3}	V_{IN} = VDD to VEE		-25	-	25	
On resistance (*5)	R_{ON}	I_{ON} = 100 μA		-	2	4	KΩ
Supply current (*6)	I_{STBY}	f_{CL1}=32kHz	VSS pin	-	-	100	μA
	I_{DD}	f_{CL1}=32 kHz, f_M=80 Hz	VDD=5 V	-	-	200	
			VDD=3 V	-	-	120	
	I_{EE}		VDD=5 V	-	-	150	

NOTES
(*1) Applied to CL1, D2_DL (SHL=LOW), D4_DR (SHL=HIGH), SHL, DISPOFFB, M, CS, AMS pin
(*2) Pull-up input pins : CL2, D1_SID, D3_DM (AMS=HIGH), ELB (SHL=LOW), ERB (SHL=HIGH)
(*3) D2_DL (SHL=HIGH) ,D4_DR (SHL=LOW) pin
(*4) V0, V12, V43, V5 pin
(*5) VLCD=VDD-VEE, V0=VDD=5 V, V5=VEE=-23 V
V12=VDD-1/n(VLCD), V43=VEE+1/n(VLCD), n = 17(1/256 duty, 1/17 bias)
(*6) V0=VDD, V12=3.35 V(VDD=5 V) or 1.47 V(VDD=3 V),
V43=-21.35 V(VDD=5 V) or -21.47 V(VDD=3 V), V5=VEE=-23 V, no-load condition (1/256 duty, 1/17 bias)
single-type mode operation : AMS=VSS, SHL=VSS, DISPOFFB=VDD
D1_SID=D3_DM=VDD, D4_DR=OPEN, ELB=ERB=OPEN,
I_{STBY} : VDD=5 V, M=VSS, D2_DL=VSS
I_{DD} : fM=80 Hz, D2_DL=VDD
VDD=3 V, display data pattern = 10000000..., 01000000..., 00100000..., 00010000..., ..
VDD=5 V, display data pattern = 10000000..., 01000000..., 00100000..., 00010000..., ..
I_{EE} : fM=80Hz, D2_DL=VDD
VDD=5 V, current through V_{EE} Pin, display data pattern = 10000000..., 01000000..., 00100000..., 00010000...

AC CHARACTERISTICS

(1) SEGMENT DRIVER APPLICATION

(Vss = 0 V, Ta = -30 ~ +85°C)

Characteristic	Symbol	Test Condition	(1) VDD=5 V ± 10%			(2) VDD=3 V ± 10%			Unit
			MIN	TYP	MAX	MIN	TYP	MAX	
Clock cycle time	t_{CY}	Duty=50%	125	-	-	250	-	-	ns
Clock pulse width	t_{WCK}	-	45	-	-	95	-	-	
Clock rise/fall time	$t_{R/tF}$	-	-	-	-	-	-	30	
Data set-up time	t_{DS}	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
Clock set-up time	t_{CS}	-	80	-	-	120	-	-	
Clock hold time	t_{CH}	-	80	-	-	120	-	-	
Propagation delay time	t_{PHL}	ELB Output	-	-	60	-	-	125	
		ERB Output			60			125	
ELB,ERB set-up time	t_{PSU}	ELB Input	30	-	-	65	-	-	
		ERB Input	30			65			
DISPOFFB low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	µs
DISPOFFB clear time	t_{CD}	-	100	-	-	100	-		ns
M - OUT propagation delay time	t_{PD1}	CL=15 pF	-	-	1.0	-	-	1.2	µs
CL1 - OUT propagation delay time	t_{PD2}		-	-	1.0	-	-	1.2	
DISPOFFB - OUT propagation delay time	t_{PD3}		-	-	1.0	-	-	-	

AC CHARACTERISTICS (continued)

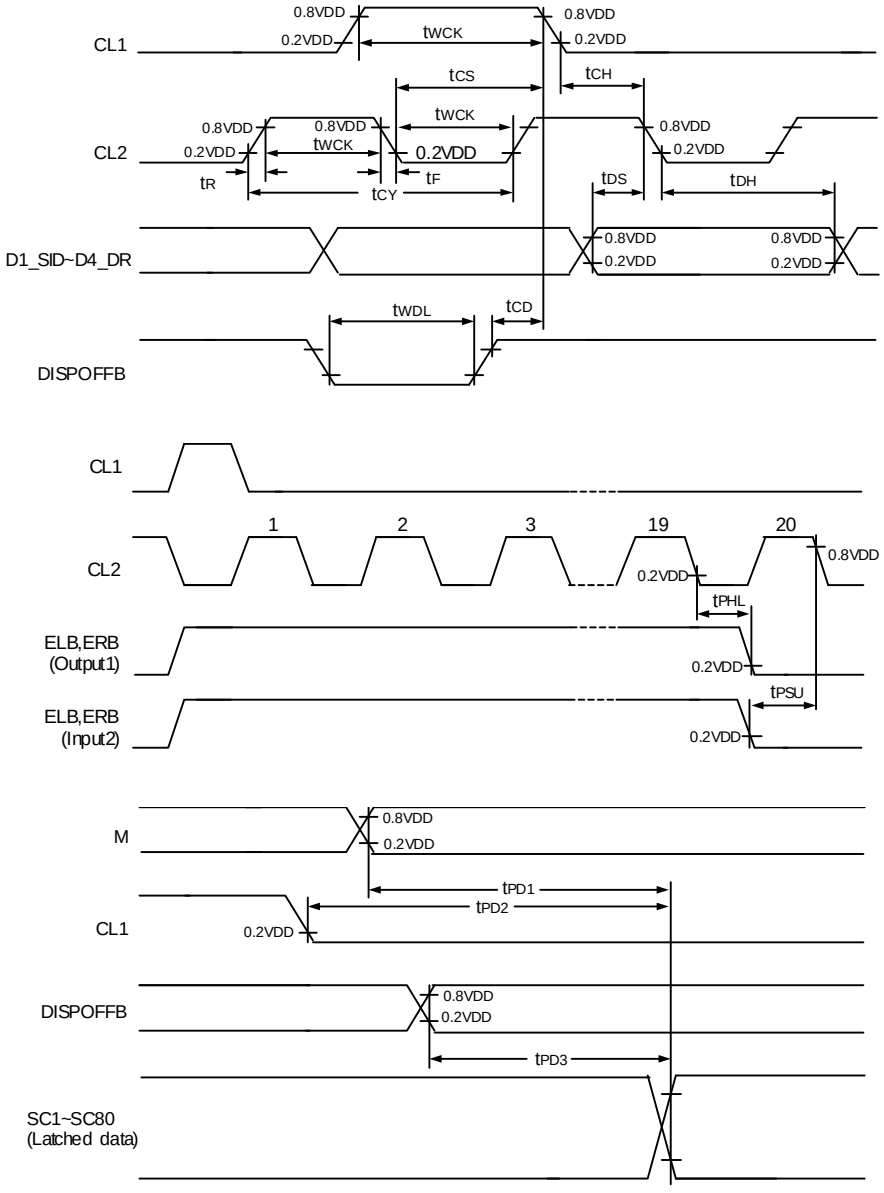
(2) COMMON DRIVER APPLICATION

(Vss = 0 V, Ta = -30 ~ +85°C)

Characteristic	Symbol	Test Condition	(1) VDD=5 V ± 10%			(2) VDD=3V±10%			Unit
			MIN	TYP	MAX	MIN	TYP	MAX	
Clock cycle time	t_{CY}	Duty=50%	250	-	-	500	-	-	ns
Clock pulse width	t_{WCK}	-	45	-	-	95	-	-	
Clock rise/fall time	$t_{R/tF}$	-	-	-	50	-	-	50	
Data set-up time	t_{DS}	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
DISPOFFB low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	µs
DISPOFFB clear time	t_{CD}	-	100	-	-	100	-	-	ns
Output delay time	t_{DL}	CL=15 pF	-	-	200	-	-	250	
M - OUT propagation delay time	t_{PD1}		-	-	1.0	-	-	1.2	µs
CL1 - OUT propagation delay time	t_{PD2}		-	-	1.0	-	-	1.2	
DISPOFFB - OUT propagation delay time	t_{PD3}		-	-	1.0	-	-	1.2	

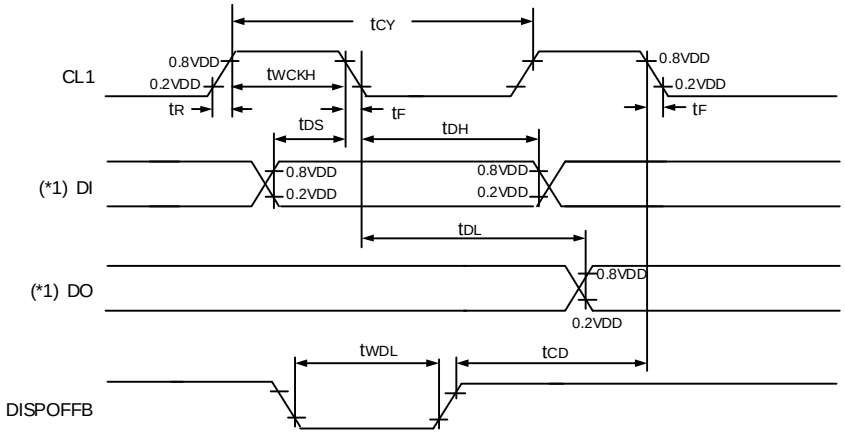
AC CHARACTERISTICS (continued)

(3) SEGMENT DRIVER APPLICATION TIMING

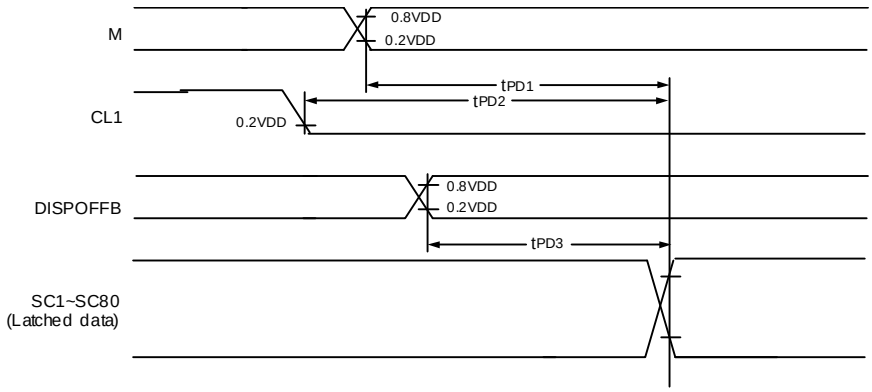


AC CHARACTERISTICS (continued)

(4) COMMON DRIVER APPLICATION TIMING



(*1) When in single-type interface mode
DI ⇒ D2_DL(SHL="L"), D4_DR(SHL="H")
DO ⇒ D4_DR(SHL="L"), D2_DL(SHL="H")
When in dual-type interface mode
DI ⇒ D2_DL and D3_DM(SHL="L"), D4_DR and D3_DM(SHL="H")
DO ⇒ D4_DR(SHL="L"), D2_DL(SHL="H")

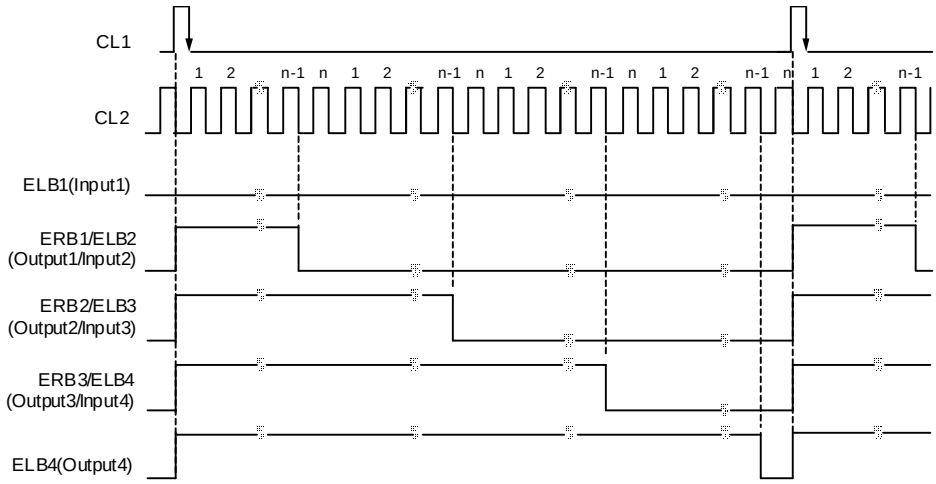


POWER DOWN FUNCTION

In the case of cascade connection of segment mode drivers, KS0086 has a "power down function" In order to reduce the power consumption.

SHL	Enable input	Enable out-put	Current driver status	The other drivers status
L	ERB	ELB	While ERB="Low", current driver is enabled.	Disabled
H	ELB	ERB	While ELB="Low", current driver is enabled.	Disabled

* In the case of common driver application, power down function does not work.



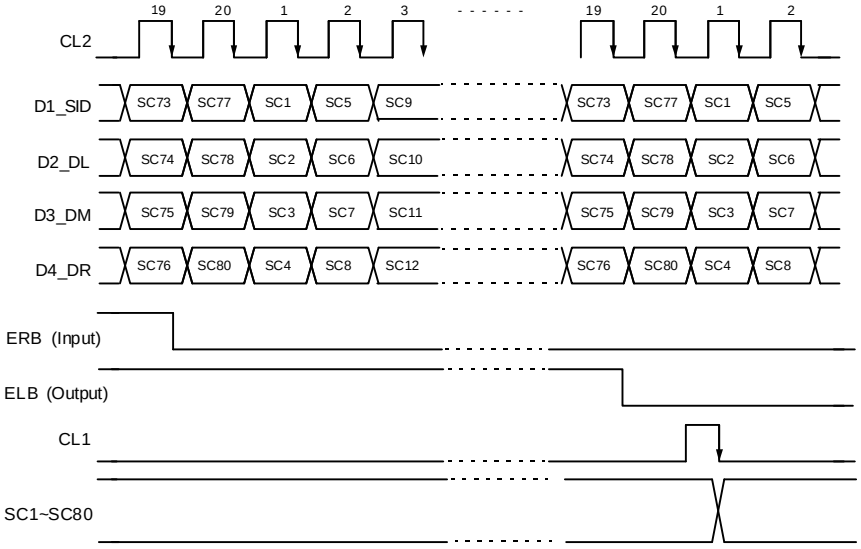
NOTE 1) SHL = "High" (ELB = Input, ERB = Output)
Current KS0086's ERB must be connected to the next KS0086's ELB.

2) When in 4-bit parallel interface mode : n = 20
When in 1-bit serial interface mode : n = 80

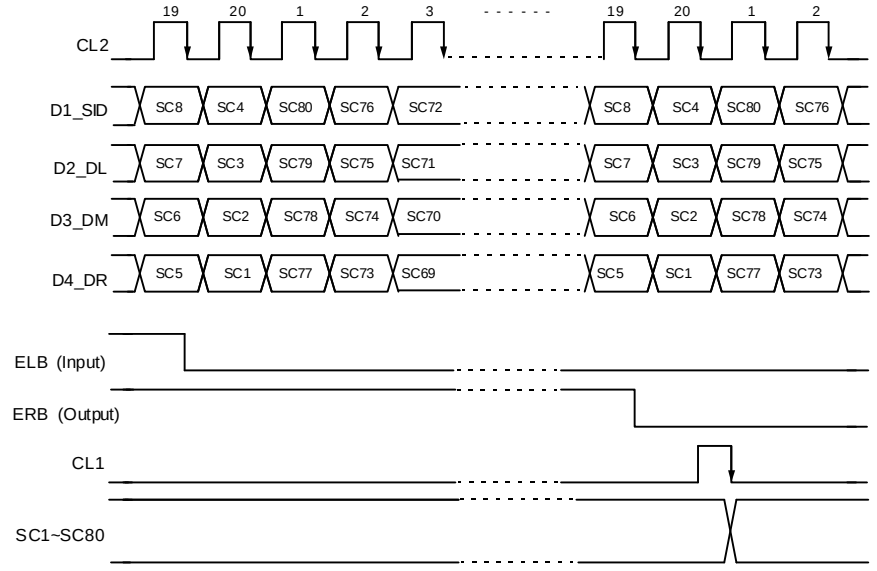
OPERATION TIMING DIAGRAM

4-BIT PARALLEL MODE INTERFACE SEGMENT DRIVER

When SHL = "Low"

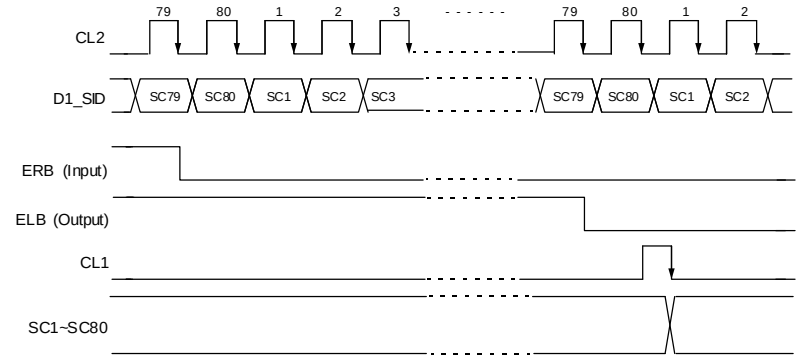


When SHL = "High"

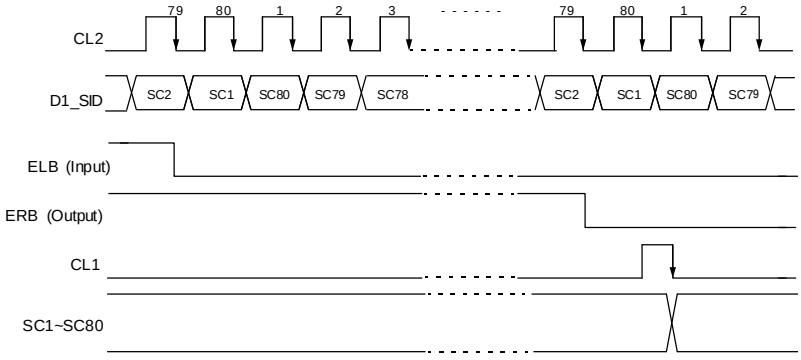


1-BIT SERIAL MODE INTERFACE SEGMENT DRIVER

When SHL = "Low"

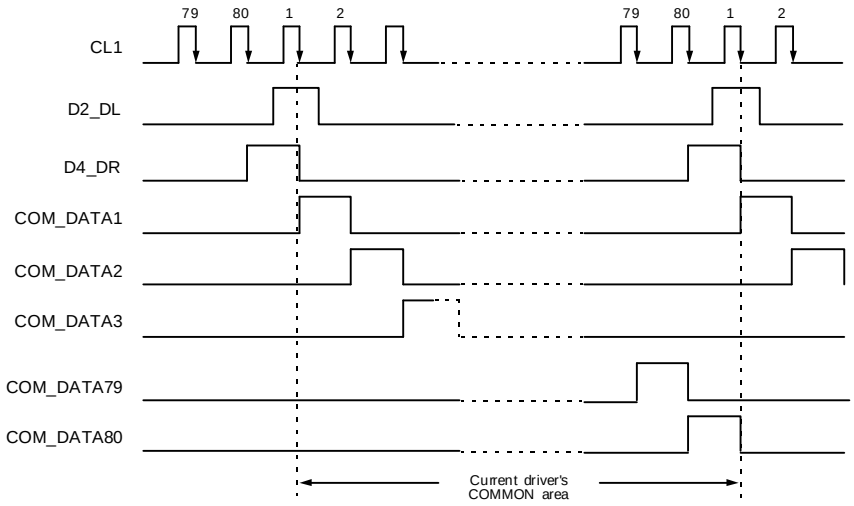


When SHL = "High"

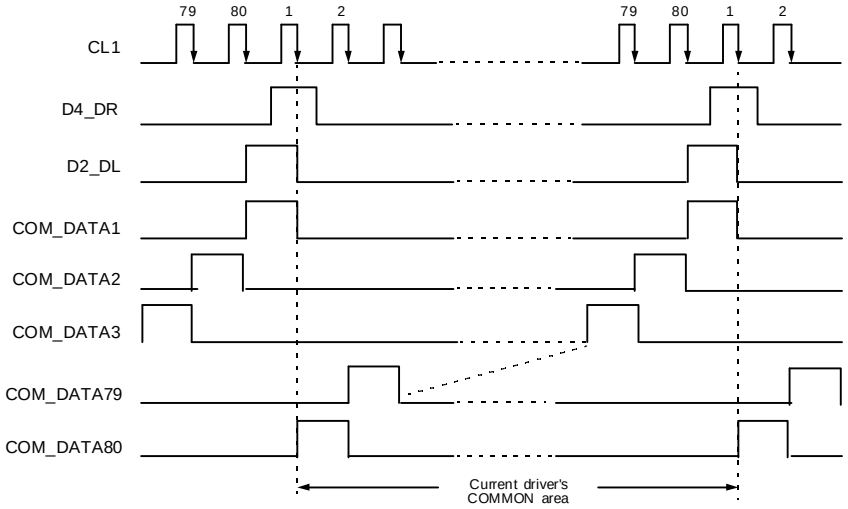


SINGLE-TYPE INTERFACE MODE COMMON DRIVER

When SHL = "Low"

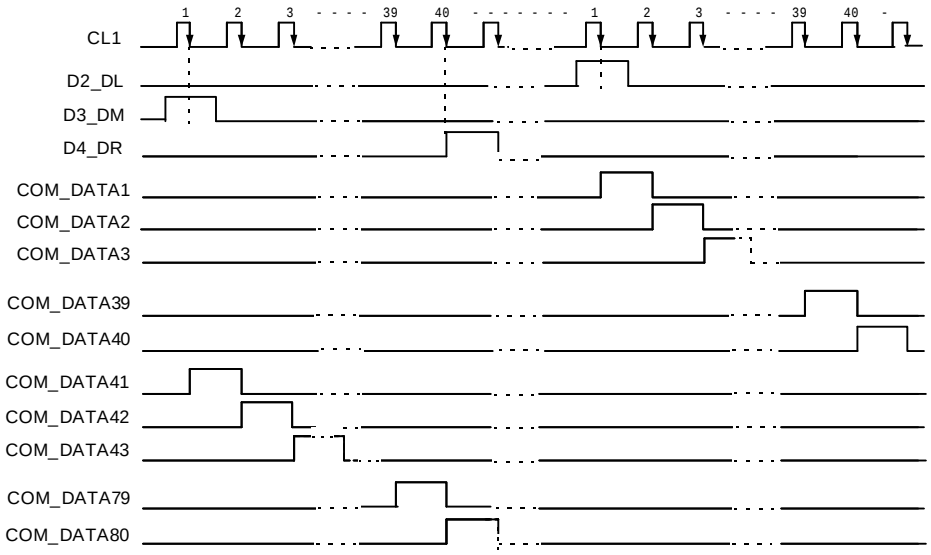


When SHL = "Low"

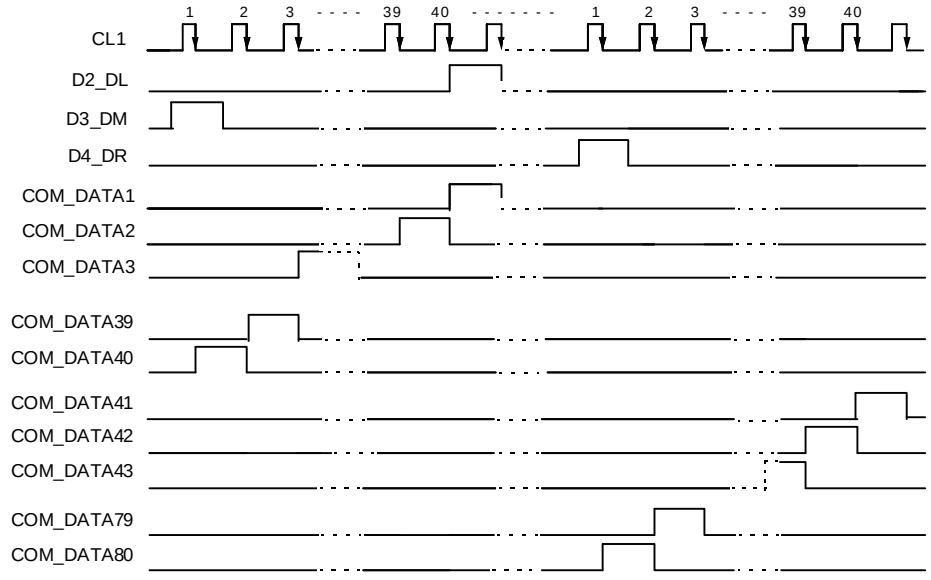


(4) DUAL-TYPE INTERFACE MODE COMMON DRIVER

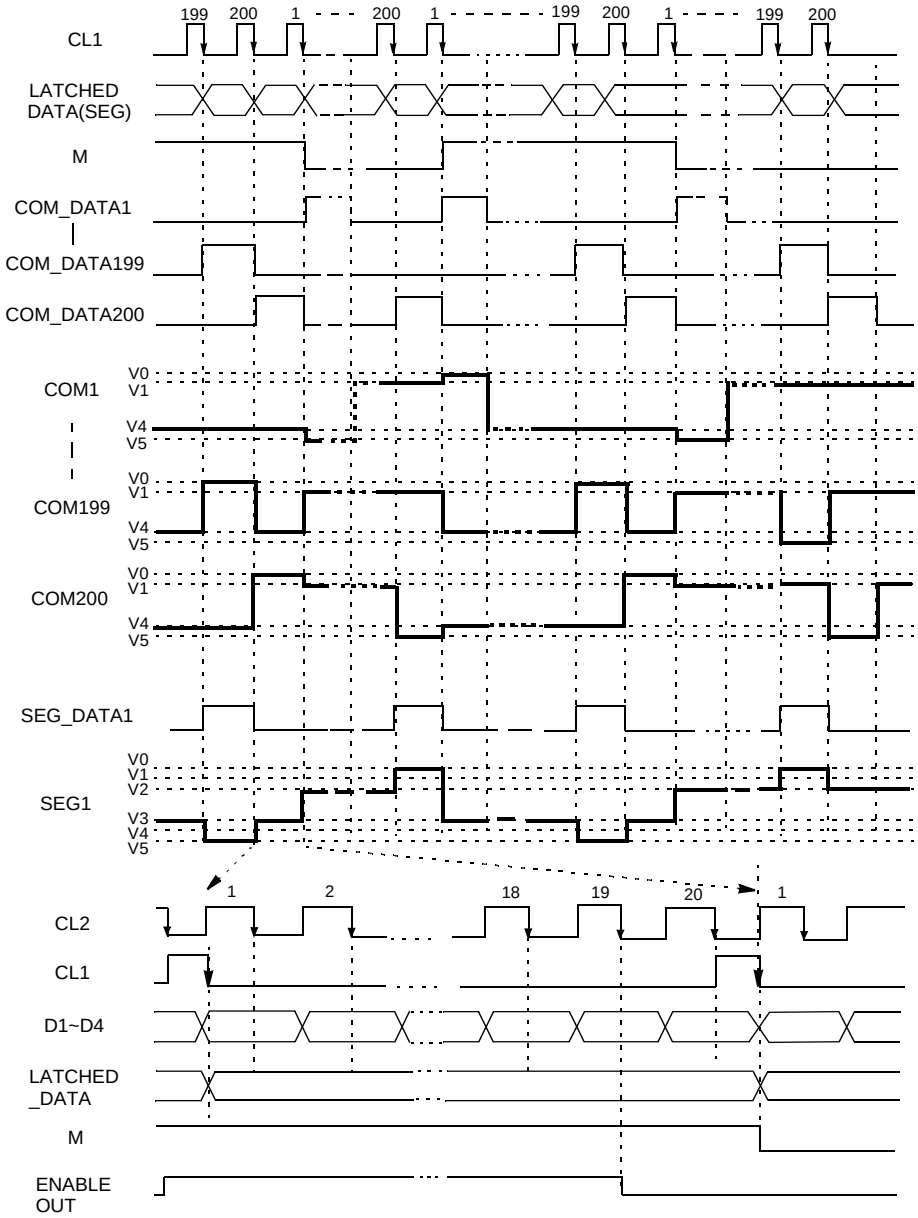
When SHL = "Low"



When SHL = "High"



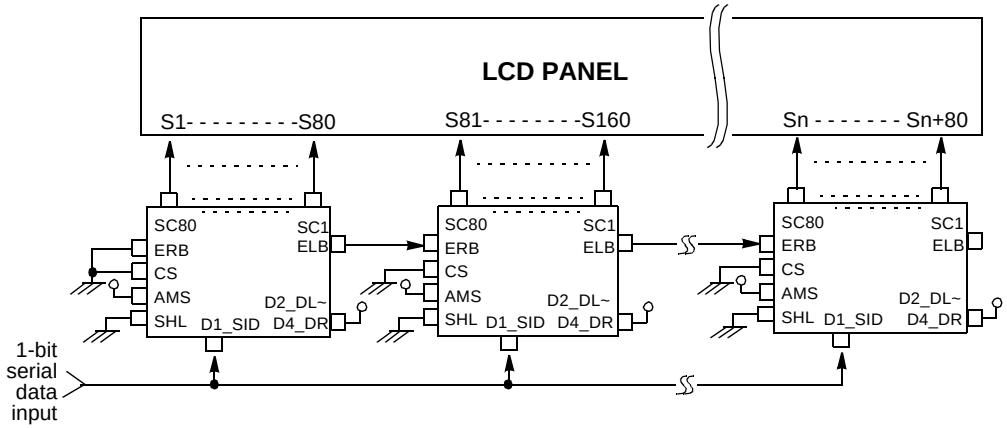
(5) COMMON / SEGMENT DRIVER TIMING (1/200 DUTY)



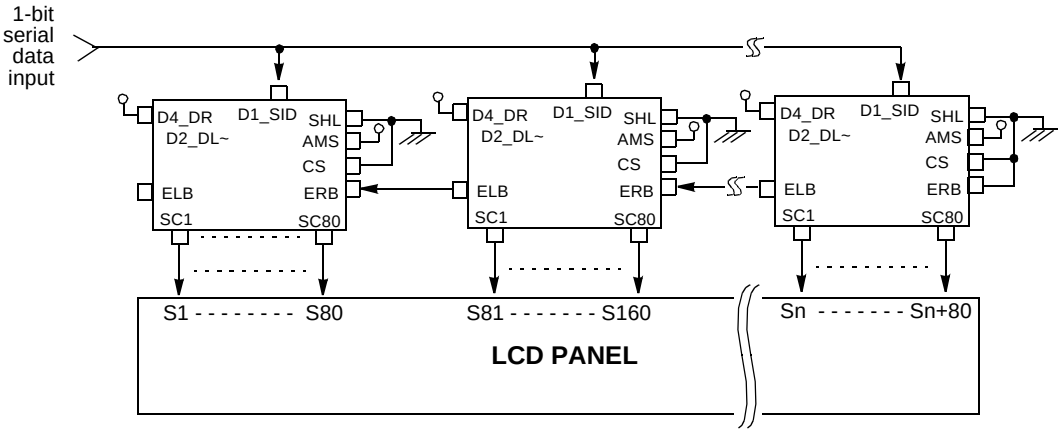
APPLICATION INFORMATION

(1) 1-BIT SERIAL INTERFACE MODE (80-CH SEGMENT DRIVER)

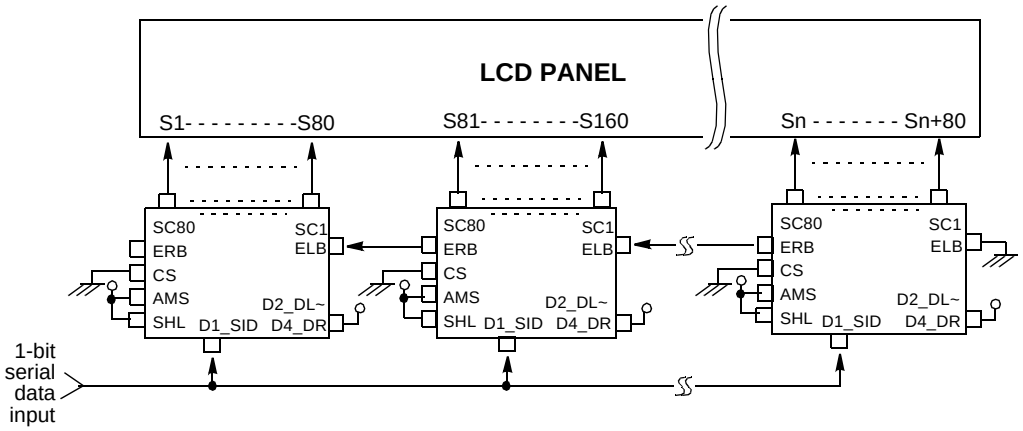
a) Lower View (SHL = L, AMS = H)



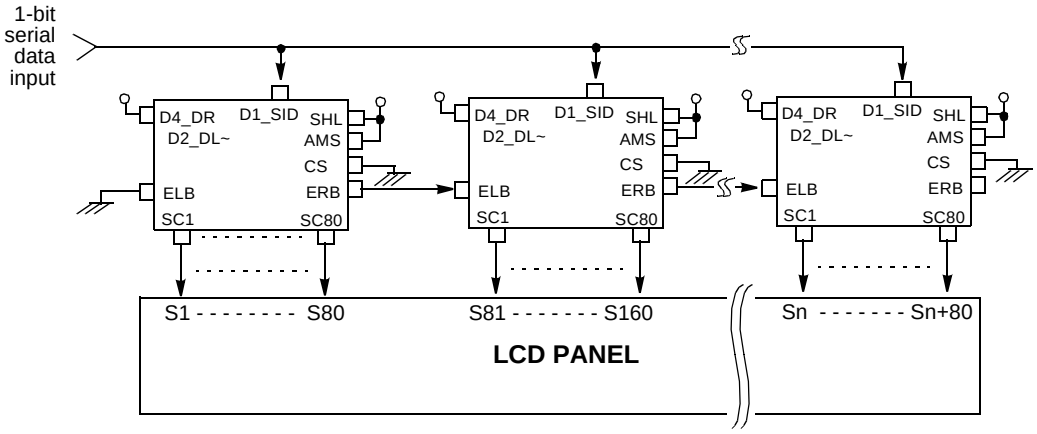
b) Upper View (SHL = L, AMS = H)



c) Lower View (SHL = H, AMS = H)

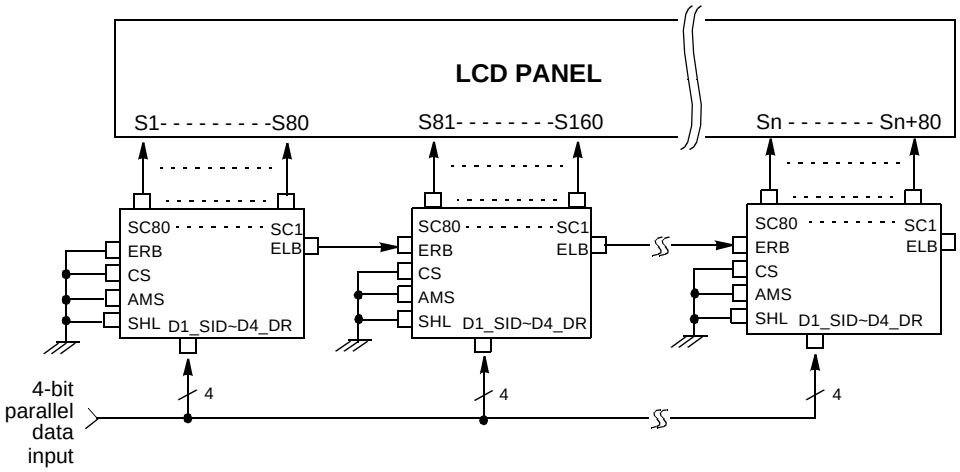


d) Upper View (SHL = H, AMS = H)

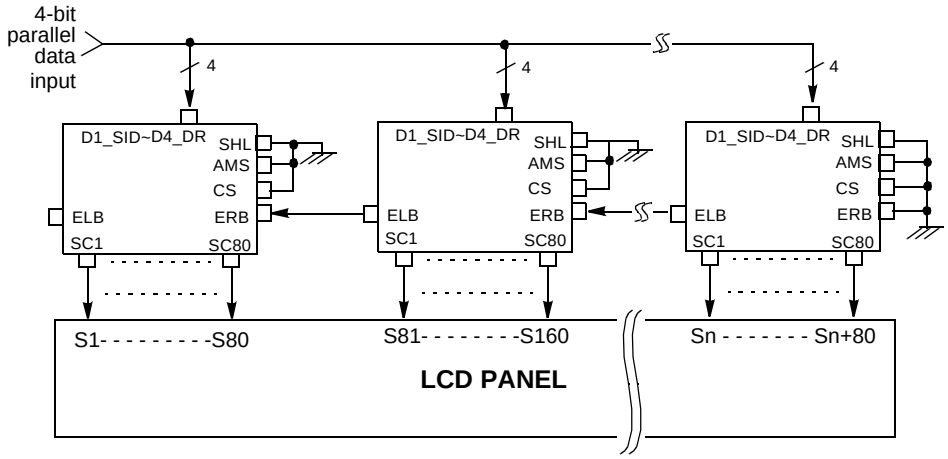


(2) 4-BIT PARALLEL INTERFACE MODE (80-CH SEGMENT DRIVER)

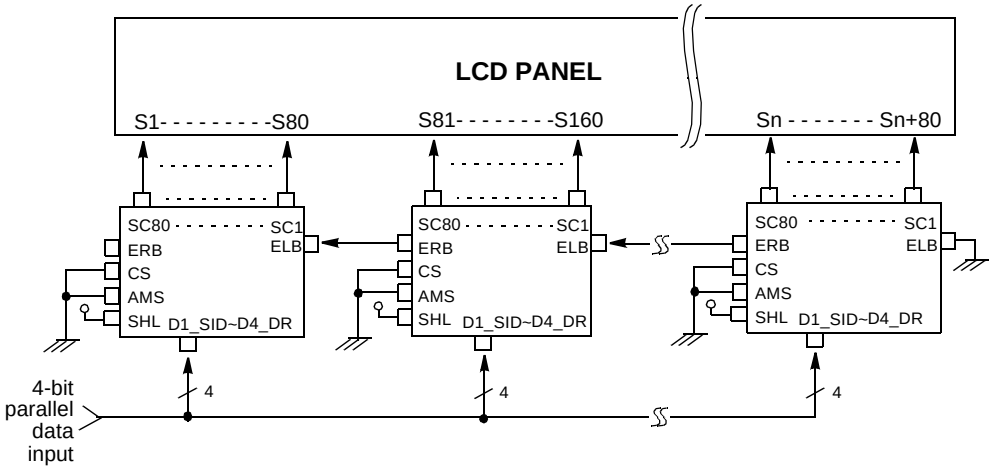
a) Lower View (SHL = L, AMS = L)



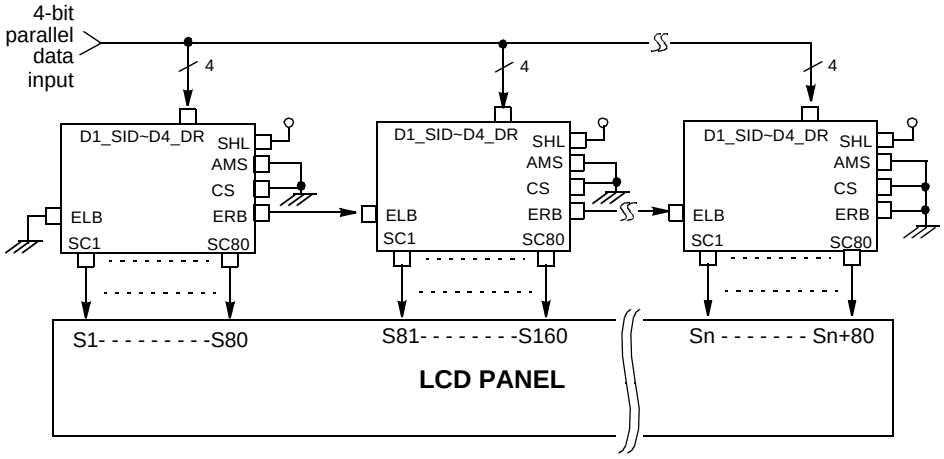
b) Upper View (SHL = L, AMS = L)



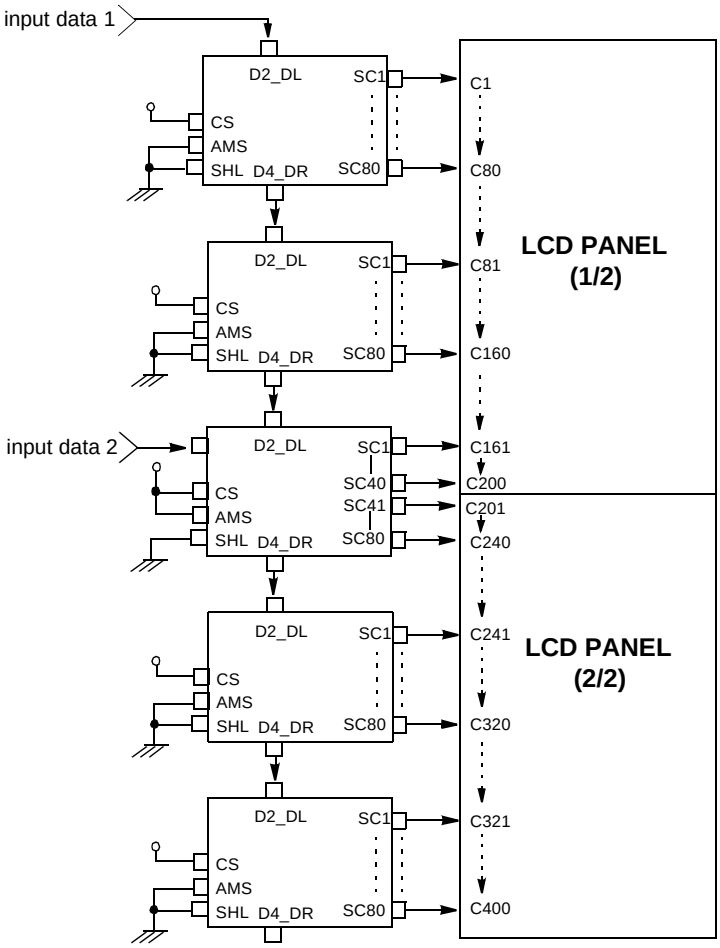
c) Lower View (SHL = H, AMS = L)



d) Upper View (SHL = H, AMS = L)

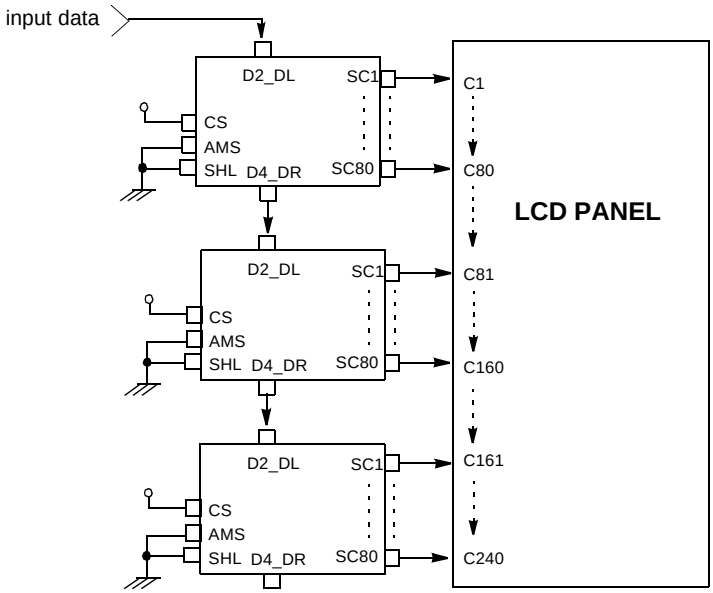


(3) DUAL-TYPE INTERFACE MODE (40CH + 40H COMMON DRIVER)



* NOTE:
Using this application mode (dual-type common mode), the duty ratio can be reduced to half. In the case abale, 1/200 duty can be used to drive the 400 common LCD panel.

(4) SINGLE-TYPE INTERFACE MODE (80-CH COMMON DRIVER)



APPLICATION CIRCUIT EXAMPLE