KM68257P/KM68257LP

CMOS SRAM

T-46-23-14

32K × 8 Bit Static RAM

FEATURES

- Fast Access Time 35,45,55ns(max.)
- Low Power Dissipation
  - Standby (TTL) : 3 mA (max.)
  - (CMOS): 100 μA (max.)
  - Operating : 120 mA (max.)
- Single 5V ± 10% Power Supply
- TTL compatible inputs and output
- Full Static Operation
  - No clock or refresh required
- Tri-state Output
- Low Data Retention Current: 50 μA (max.)
- Battery Back-up Operation
  - 2V (min.) Data Retention
- Standard 28-pin DIP (600mil)

GENERAL DESCRIPTION

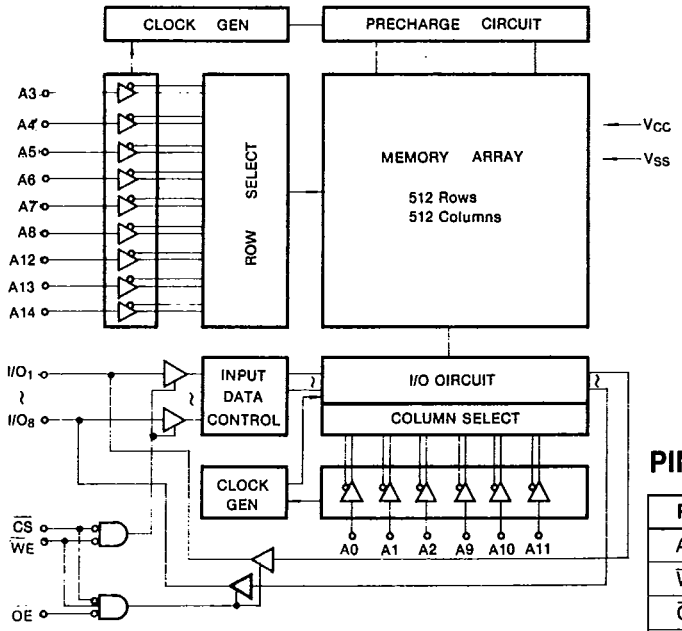
The KM68257 is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bit.

The device is fabricated using Samsung's advanced CMOS process.

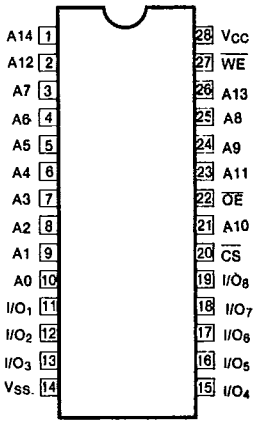
The KM68257 has an output enable input for precise control of the data outputs. It also has a chip enable input for the minimum current power down mode.

The KM68257 has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which battery back-up for nonvolatility is required.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Select
I/O_1-I/O_8	Data Input/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

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ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_d	1.0	W
Storage Temperature	T_{stg}	−55 to +125	°C
Operating Temperature	T_a	0 to 70	°C

*Note: Stresses grater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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RECOMMENDED OPERATING CONDITIONS (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2		$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}*	−0.5		0.8	V

* V_{IL}(min) = −3.0V for <20ns pulse

DC AND OPERATING CHARACTERISTICS

(Ta = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Condition	Ver	Min	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}		−2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{I/O} = V_{SS}$ to V_{CC}		−2	2	μA
Operating Power Supply Current	I_{CC1}	$\overline{CS} = V_{IL}$, $V_{IN} = V_{IL}/V_{IH}$ I_{OUT} = 0mA			30	mA
Average Operating Current	I_{CC2}	Min Cycle, 100% Duty $\overline{CS} = V_{IL}$, I_{OUT} = 0mA			120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$			3	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$	P		1	mA
			LP		100	μA
Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
Output High Voltage	V_{OH}	I_{OL} = −4mA		2.4		V

CAPACITANCE (f = 1MHz, Ta = 25°C)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	8	pF

*Note: Capacitance is sampled and not 100% tested.

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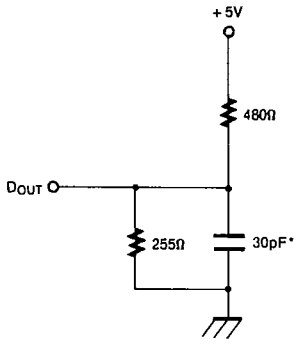
AC CHARACTERISTICS

(Ta = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

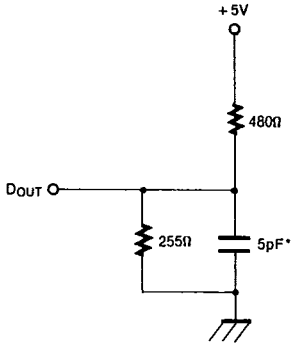
TEST CONDITIONS (Ta = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load(a)



Output Load(b)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



*Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68257P-35 KM68257LP-35		KM68257P-45 KM68257LP-45		KM68257P-55 KM68257LP-55		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		55		ns
Address Access Time	t_{AA}		35		45		55	ns
Chip Select to Output	t_{ACS}		35		45		55	ns
Output Enable to Output	t_{OE}		15		20		25	ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Enable to Low-Z Output	t_{LZ}	5		10		10		ns
Output Disable to High-Z Output	t_{OHZ}	0	15	0	15	0	20	ns
Chip Disable to High-Z Output	t_{HZ}	0	15	0	15	0	20	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		ns
Chip Deselection to Power Down Time	t_{PD}		30		35		40	ns

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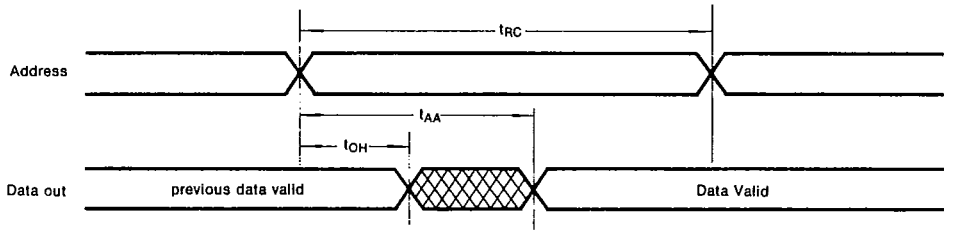
WRITE CYCLE

Parameter	Symbol	KM68257P-25 KM68257LP-25		KM68257P-35 KM68257LP-35		KM68257P-45 KM68257LP-45		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	35		45		55		ns
Chip Select to End of Write	t_{CW}	35		40		45		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	30		35		40		ns
Write Pulse Width	t_{WP}	30		35		40		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	15	0	15	0	20	ns
Data to Write Time Overlap	t_{DW}	20		25		30		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		5		5		ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE NO: 1



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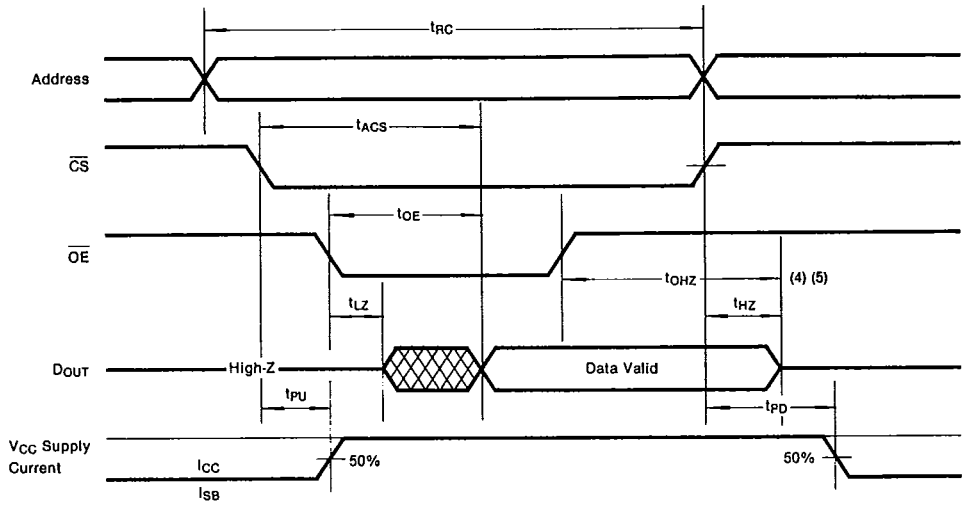
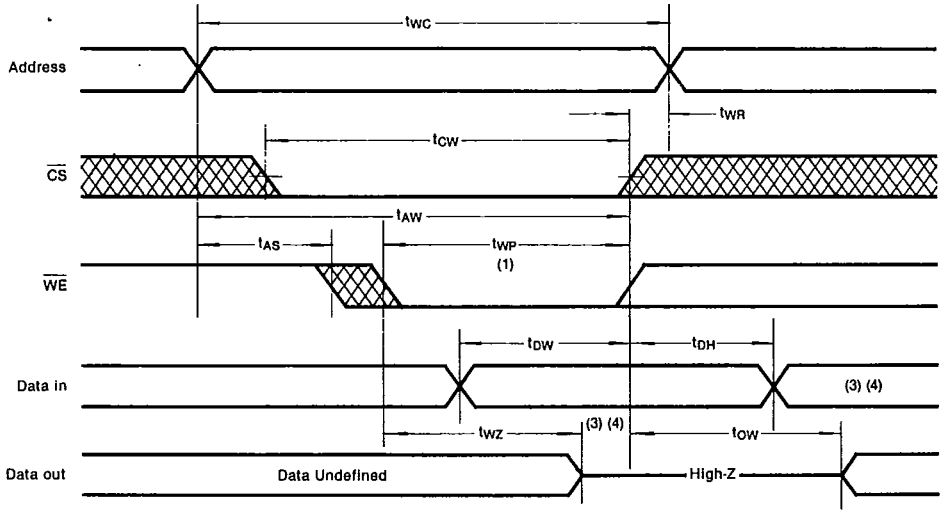
TIMING WAVEFORM OF READ CYCLE NO: 2



Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load(b).
5. This parameter is sampled and not 100% tested.
6. Device is continuosly selected with $\overline{CS} = V_{IL}$
7. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



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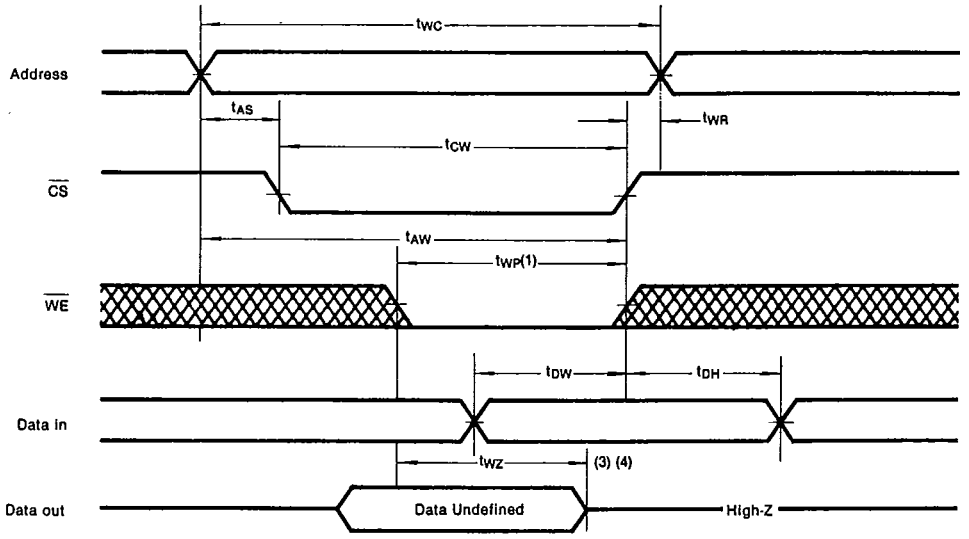
TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



Note (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±500mV from steady state voltage with Load(b).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
6. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

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FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O PIN	Supply Current	Mode
H	X	X	High-Z	I_{SB}, I_{SB1}	Standby Mode
L	H	H	High-Z	I_{CC1}, I_{CC2}	Output Disable
L	H	L	D_{OUT}	I_{CC1}, I_{CC2}	Read
L	L	L	D_{IN}	I_{CC1}, I_{CC2}	Write

*Note: X means Don't Care

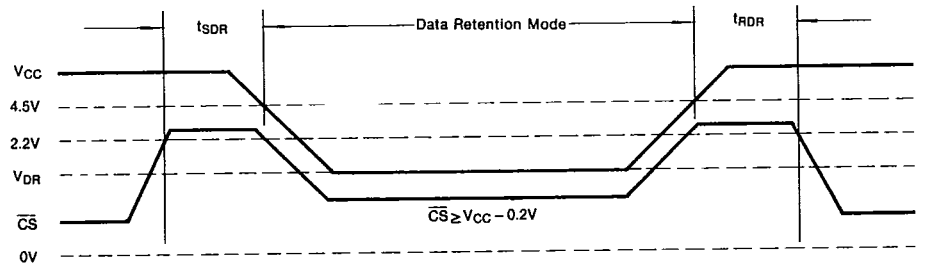
DATA RETENTION CHARACTERISTICS (Ta=0 to 70°C)

(This characteristics is guaranteed only for L-version)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	I_{DR}	$V_{CC}=3V$ $\overline{CS} \geq V_{CC} - 0.2V$		1	50	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)	0			nS
Recovery Time	t_{RDR}		t_{RC}*			nS

*t_{RC} = Read Cycle Time

DATA RETENTION WAVEFORM



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PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)