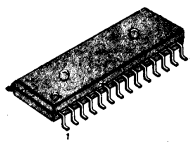
KDA0340D

1 BIT D/A CONVERTER

INTRODUCTION

The KDA0340D is a CMOS low-power two-channel digital-to-analog converter for digital audio systems. It is a delta-sigma D/A converter which includes an 8x digital interpolation filter followed by 64x oversampled Delta-sigma Modulator and PWM blocks.
The delta-sigma technology makes it possible for digital audio systems to process high quality audio signals by combining the oversampling and the noise shaping technologise. The PWM block output signal is the PCM signal generated by the internal control signal. Each channel of the D/A converter has positive- and negative-phase output. The external differential circuit makes it possible to achieve a high S/N ratio and low THD.
The master clock rate is 384 times the input word rate.
The KDA0340D has an interface switching control pin (MCOM) which makes it possible to select MICOM control and deemphasis control which can respond to three types of sampling rates (32,44.1.48Khz). In the double speed mode, by using the double speed mode pin (DN) the KDA0340D can operate normally with no change of the external master clock rate.

28 -SOP - 375



ORDERING INFORMATION

Device	Supply Voltage	Package	Temperature Range
KDA0340D	5V	28SOP	0 ~ + 70℃

FEATURES

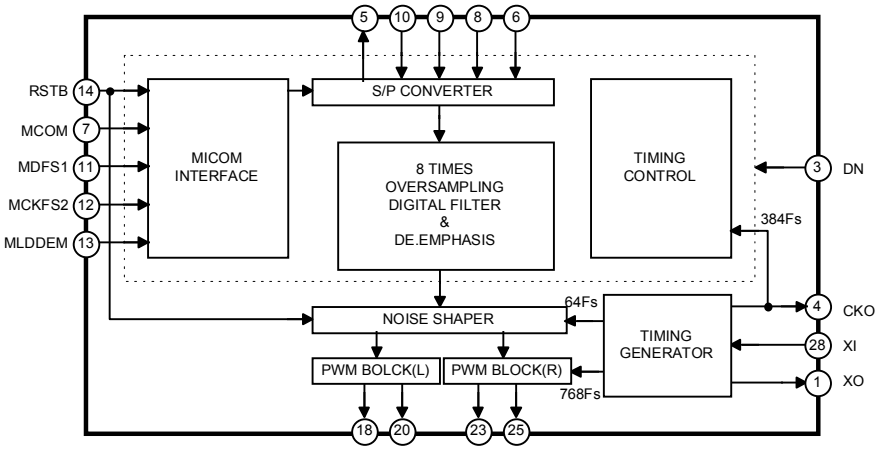
- 16-bit 2s complement serial data input
  (corresponds to LSI format and 1^2s format)
- On-chip 8 times digital filter
  (Passband ripple : ± 0.0072dB, Stopband attenuation :>62.7dB)
- 3 times △-Σ method (1bit D/A converter)
- On-chip timing generator (with exteranl X-tal)
- Zero input detection function
- Digital attenuation control
- Master clock rate : 384 times (in both normal and double speed mode)
- Adjustable system sampling rate including 32KHz, 44.1KHz, and 48KHz
- Power supply : 5V single (double speed mode operation possible)
- Package type : 28SOP

TYPICAL APPLICATIONS

CDP, LDP, DCC, MD, and high quality digital audio systems

KDA0340D 1 BIT D/A CONVERTER

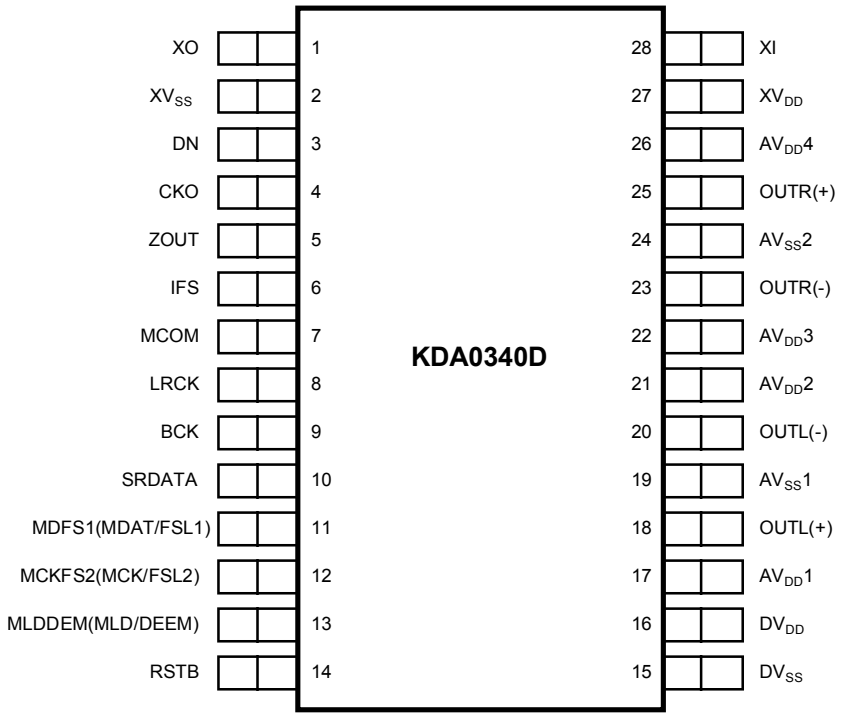
BLOCK DIAGRAM



PIN CONFIGURATION

KDA0340D **1 BIT D/A CONVERTER**

Small Outline Package



(Top View)

PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	XO	O	X-tal output
2	XV_{SS}	-	Digital ground (X-tal oscillator part)
3	DN	I	Double speed mode select (when H : double, L: normal)
4	CKO	O	$384f_s$ output
5	ZOUT	O	Zero input detection output (when zero detection, low output)
6	IFS	I	Input format select (when L: SONY, H: PHILIPS 1^2S format).
7	MCOM	I	Interface switching control input (when H : MDAT, MCK, MLD pin control) when L : FSL1, FSL2, DEEM pin control
8	LRCK	I	LR clock input
9	BCK	I	Bit clock input
10	SRDATA	I	Serial digital data input
11	MDFS1 (MDAT/FSL1)	I	Micom command data input : MDAT (when MCOM is H) Format selection pin 1 : FSL1 (when MCOM is L)
12	MCKFS2 (MCK/FSL2)	I	Micom command clock input : MCK (when MCOM is H) Format selection pin 2 : FSL2 (when MCOM is L)
13	MLDDEM (MLD/DEEM)	I	Micom command load input : MLD (when MCOM is H) De - emphasis control input : DEEM (when MOCM is L) when DEEM is H : de - emphasis on, when L : de - emphasis off.
14	RSTB	I	Reset (when low : reset)
15	DV_{SS}	-	Digital ground
16	DV_{DD}	-	Digital supply voltage
17	$AV_{DD}1$	-	Analog supply voltage 1
18	OUTL(+)	O	L-channel positive output
19	$AV_{SS}1$	-	Analog ground 1
20	OUTL(-)	O	L-channel negative output
21	$AV_{DD}2$	-	Analog supply voltage 2
22	$AV_{DD}3$	-	Analog supply voltage 3
23	OUTR(-)	O	R-channel negative output
24	$AV_{SS}2$	-	Analog ground 2
25	OUTR (+)	O	R-channel positive output
26	$AV_{DD}4$	-	Analog supply voltage 4
27	XV_{DD}	-	Digital supply voltage (X-tal oscillator part)
28	XI	I	X-tal input

ABSOLUTE MAXIMUM RATINGS (Notes 1&2)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to 7.0	V
Input Voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Output Voltage	V_{OUT}	-0.3 to V_{DD} +0.3	V
Power Dissipation	P_D	264	mW
Storage Temperature Range	T_{STG}	-40 to +125	℃
ESD Susceptibility (Note 3)	V_{ESD}	> ± 1,500	V

(Test Conditions : V_{SS} = OV, V_{SS} = XV_{SS}, AV_{SS}, DV_{SS}, V_{DD} = AV_{DD}, DV_{DD}, XV_{DD})

Note 1 : ABSOLUTE MAXIMUM RATINGS are those values beyond which the device may be damaged permanenty.
Normal operation is not guaranteed at or above these estremes.
Note 2 : All voltages are measured with respect to the voltage level unless otherwise specified.
Note 3 : 100pF discharged through a 1.5kΩ resistor (Human body model).

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
X-tal Oscillation Frequency	$f_{x\text{-}tal}$		16.9344		MHz
Digital Input H Voltage 1 (Note 4)	$V_{IH}1$	3.5			V
Digital Input L Voltage 1 (Note 4)	$V_{IL}1$			0.5	V
Digital Input H Voltage 2 (Note 5)	$V_{IH}2$	$0.7XV_{DD}$			V
Digital Input L Voltage 2 (Note 5)	$V_{IL}2$			$0.3XV_{DD}$	V
Clock High Time	t_{PWH}	23.6			ns
Clock LowTime	t_{PWL}	23.6			ns
Operating Temperature Range (Note 6)	T_{OPR}	0		70	℃

(Test Conditons : V_{SS} = OV, V_{SS}= = XV_{SS}, AV_{SS}, DV_{SS}, V_{DD} = AV_{DD}, DV_{DD}, XV_{DD})

Note 4 : DN, IFS, MCOM, LRCK, BCK, SRDATA, MDFS1, MCKFS2, MLDDEM, RSTB
Note 5 : XI
Note 6 : Test Condition : V_{DD} =AV_{DD}, DV_{DD}, XV_{DD} = 5V

DC ELECTRICAL CHARACTERISTICS

(Converter Specifications V_{DD}= AV_{DD} = DV_{DD} = XV_{DD} =4.5 ~ 5.5V, V_{SS} = XV_{SS} = AV_{SS} = DV_{SS} = 0V,
Ta = 25℃, Clock rate = 384 times, Input word rate = 44.1KHz, Input Data = 16 bits unless otherwise specified.)

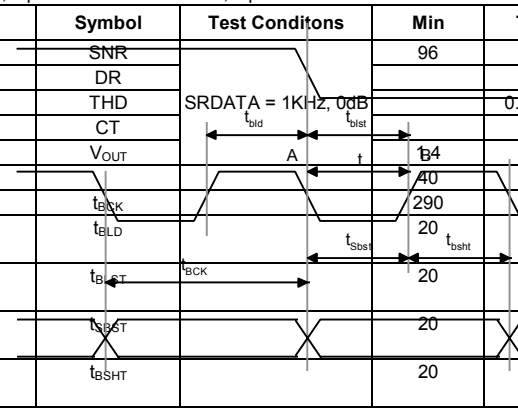
Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Digital Supply Current	DI_{DD}	No Load		30	45	mA
Analog Supply Current	AI_{DD}	V_{DD} = 5V		2	3	mA
Power Dissipation	P_D			160	264	mW
Input Leakage Current	I_{LEAK}		-10		10	㎂
Digital Output H Voltage	V_{OH}	I_{OH} = -1mA	AV_{DD} -0.5			V
Digital Output L Voltage	V_{OL}	I_{OL} = 1mA			0.5	V

Note 7 : V_{OH}, V_{OL} items are for OUTL(+), OURL (-), OUTR (+), OUTR (-), CKO, ZOUT pins.

AC ELECTRICAL CHARACTERISTICS

(Converter specifications : V_{DD} = AV_{DD} = DV_{DD} = XV_{DD} = 5V, V_{SS} = XV_{SS} = AV_{SS} = DV_{SS} = 0V,
Ta = 25℃, Clock rate = 384times, Input word rate = 44.1Khz, Input Data = 16 bits unless otherwise specified)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Signal-to-Noise Ratio	SNR	SRDATA = 1KHz, 0dB	96	100		dB
Dynamic Range	DR			96		dB
Total Harmonic Distortion	THD			0.0035	0.006	%
Crosstalk	CT			100		dB
Analog Output Voltage	V_{OUT}		1.4	1.7		Vrms
Master Clock Duty Cycle			40		60	%
BCK Period	t_{BCK}		290			ns
BCK Rising and LRCK Edge Delay	t_{BLD}		20			ns
BCK Rising and LRCK Edge Setup Time	t_{BLST}		20			ns
SRDATA and BCK Rising Setup time	t_{SBST}		20			ns
BCK Ring and SRDATA Hold Time	t_{BSHT}		20			ns



* The LRCK edge should be between BCK falling (A) and BCK rising (B).

Fig 1. Timing Diagram

FUNCTION DESCRIPTION

1. Digital Filter
(1) 8x oversampling
(2) FIR digital filter
(3) Filter characteristics (when de - emphasis is off)

Characteristics	Value	Unit
Passband	0 ~ 20	KHz
Stopband	24.1	KHz
Passband Ripple	± 0.0072	dB
Stopband Attenuation	-62.7	dB

(Table 1)

Composite DAC Response
composite(8X) DAC Response

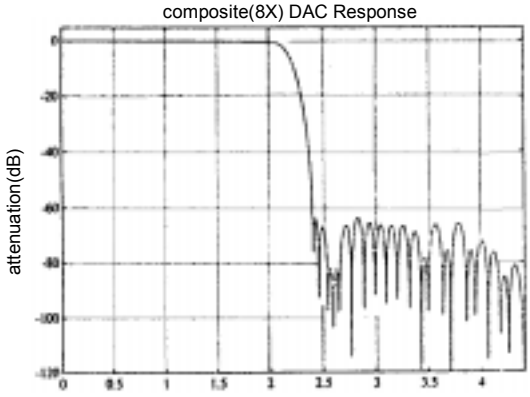


Fig2, Filter Full-frequency Characteristics

Composite DAC Response
composite(8X) D\C Response

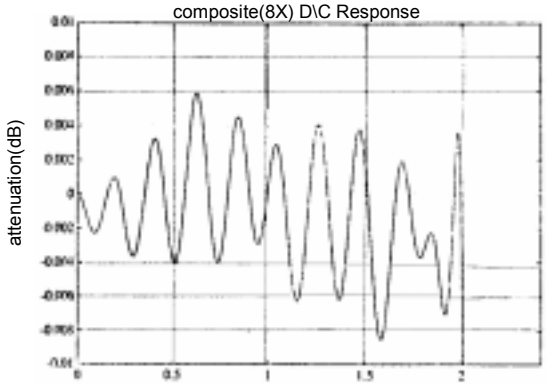


Fig3. Filter Ripple Characteristics

2. Serial Data Interface

(1) Data Input Format

Digital audio 2s complement data can be carried in MSB first sequence.

Mode	IFS	Input Format
0	L	16 - bit SONY LSI mode
1	H	16 - bit PHILIPS I^2S mode

According to the mode, timing diagram of LRCK, SRDATA, and BCK is as follows :

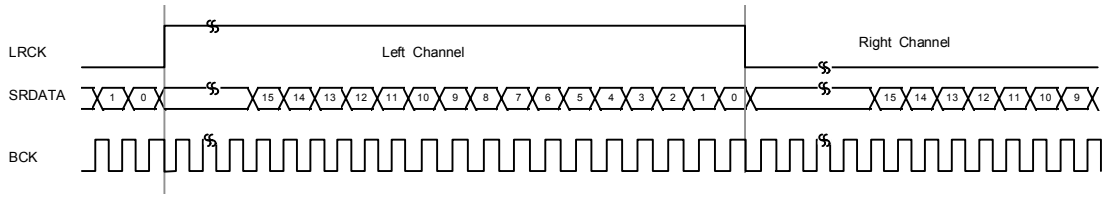


Fig 4. SONY LSI Input Format

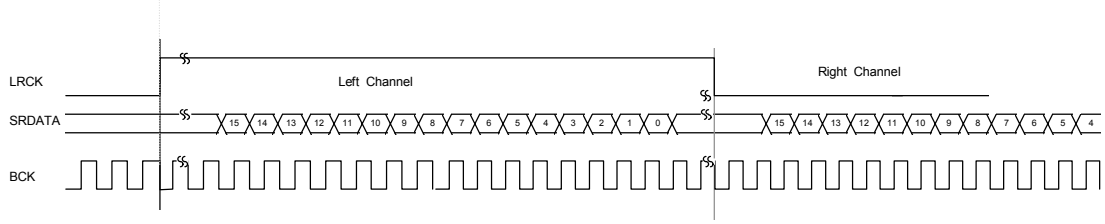


Fig 5. PHILIPS I^2S Input Format

The upper and lower limits of BIT clock are $64f_s$ and $32f_s$.

3. Synchronization Circuit

(1) Reset

When RSTB is in low state, both the LRCK phase and the timing generation counter phase of the digital filter become reset to the initial state.

(2) Detection of Asynchronization

After releasing reset, if the phase interval of LRCK and the timing generation counter are over $+1/32f_s$ and $-1/16f_s$, the timing generation counter in the digital filter becomes reset and then the phase of LRCK (fs) counter returns to initial state.

(3) Output Signal form of Asynchronization

After asynchronization of the digital filter, 46 samples of data arrive to correct the asynchronization and before all the RAM data are changed, any normal data is not output.

Accordingly, during the 1.04ms interval after asynchronization, the data outputs irregularly.

But, because the jitter of LR signal in the current CDP is several tens ns including the temperature characteristics, if there is no external noise source, asynchronization cannot occur.

4. Description of DN, CKO, ZOUT, MCOM, RSTB

(1) DN (Double Speed)

Either double speed or normal speed mode can be selected by the state of DN.
When DN is in low, normal speed operation is available, and when DN is in high, double speed mode can be possible.
In double speed mode, no change of the external X - tal or master clock rate is needed.

	Normal Speed	Double Speed
f_s	44.1KHz	88.2KHz
Master Clock (XI)	16.9344MHz	16.9344MHz

Table 3.

(2) CKO (Clock Output)

The CKO outputs $384f_s$ which is the master clock.

(3) ZOUT (Zero Input Detection Output)

When the L/R data applied from the SRDATA pin are zero state consecutively during the interval of 185.8ms (8192 times /CH), ZOUT becomes high level, and the PWM output pins of OUTL (+)/(-) and OUTR (+)/(-) turn low at the same time, otherwise to the non - zero input data, the state of ZOUT turns low immediately.
ZOUT logic can be utilized as a muting control signal of a micro - controller in audio systems.

(4) MCOM (Interface Switching Control Input)

Either digital attenuation or de - emphasis function can be decided by the state of MCOM. When MCOM is high state, the digital attenuation can be possible in which MDFS1/MCKFS2/MLDDEM pins are switched to MDAT/MCK/MLD functions, otherwise when MCOM is low state, the de - emphasis can be chosen in which MDFS1/MCKFS2/MLDDEM pins are switched FSL1/FSL2/ DEEM functions.

(5) RSTB (Reset)

When the RSTB is active low, all the blocks are reset to initial state, and the PWM output pins of OUTL (+)/(-) and OUTR (+)/(-) turn low. For 5.8ms interval after releasing instance, the PWM output pins get the square wave form of 50% duty ; after that the normal data can be outputed through outputs.

5. De - emphasis Mode Interface

Either de - emphasis or digital attenuation can be selected by the state of MCOM.
When MCOM is in low state, de - emphasis possible and MDFS1 / MCKFS2 / MLDDEM pins take the role of FSL1/FSL2/DEEM functions. The de - emphasis filter consists of IIR filter, in which the filter coefficient is decided by the choice of FSL1 and FSL2, and three kinds of sampling rate (fs = 32KHz, 44.1KHz, 48 KHz) can be chosen. (See Table 4.)
When the input data with emphasis is applied, the normal signal can be obtained through the de - emphasis block. When DEEM is set to high, the de - emphasis block operates; otherwise it does not operate.

When MCOM = L		FSL2	
		L	H
FSL1	L	44.1KHz	48KHz
	H	44.1KHz	32KHz

Table 4.

When DEEM = H, the frequency response of the filter is shown in Fig6.

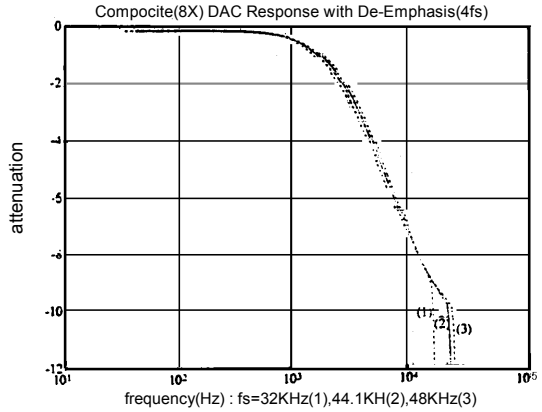


Fig 6. Frequency Response of the Filter When DEEM = H

6. Micom Interface (Micom Digital Attenuation)

When MCOM is in high state, digital attenuation can be possible and MDFS1/MCKFS2/MLDDEM pins are switched to MDAT/MCK/MLD functions.

(1) Digital Attenuation

When the 8 - bit serial data is applied to the MDAT, MCK, MLD in the form of Fig.7, digital attenuation is accomplished according to the data. The upper two MSBs should be 1.0 and the attenuation level can be adjusted according to the lower six bits. (See Table 5.) 32 steps of attenuation level is possible. When RSTB is in low state the latch circuitry for setting the attenuation level becomes reset and the attenuation level is 0dB. At this instance, because the digital filter circuit stops operation, the act of attenu - ation is impossible. In addition, whenever MDAT is not carried, MCK must be in High state.

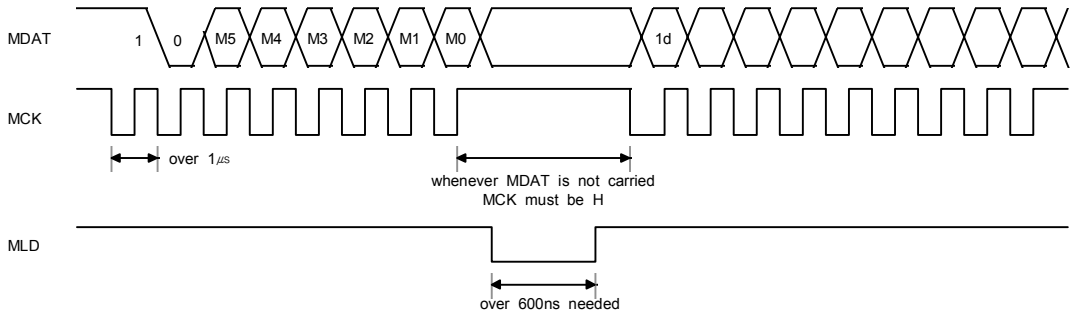


Fig 7. MICOM Interface Timing Chart

MDAT								Attenuation Level (dB)	MDAT								Attenuation Level (dB)
MSB							LSB		MSB							LSB	
	M5	M4	M3	M2	M1	M0				M5	M4	M3	M2	M1	M0	
1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	-6.30
1	0	0	0	0	0	0	1	-0.28	1	0	0	0	0	0	0	1	-6.58
1	0	0	0	0	0	1	0	-0.42	1	0	0	0	0	0	1	0	-6.88
1	0	0	0	0	0	1	1	-0.56	1	0	0	0	0	0	1	1	-7.18
1	0	0	0	0	1	0	0	-0.71	1	0	0	0	0	1	0	0	-7.50
1	0	0	0	0	1	0	1	-0.86	1	0	0	0	0	1	0	1	-7.82
1	0	0	0	0	1	1	0	-1.01	1	0	0	0	0	1	1	0	-8.16
1	0	0	0	0	1	1	1	-1.16	1	0	0	0	0	1	1	1	-8.52
1	0	0	0	1	0	0	0	-1.32	1	0	0	0	1	0	0	0	-8.89
1	0	0	0	1	0	0	1	-1.48	1	0	0	0	1	0	0	1	-9.28
1	0	0	0	1	0	1	0	-1.64	1	0	0	0	1	0	1	0	-9.68
1	0	0	0	1	0	1	1	-1.80	1	0	0	0	1	0	1	1	-10.10
1	0	0	0	1	1	0	0	-1.97	1	0	0	0	1	1	0	0	-10.55
1	0	0	0	1	1	0	1	-2.14	1	0	0	0	1	1	0	1	-11.02
1	0	0	0	1	1	1	0	-2.32	1	0	0	0	1	1	1	0	-11.51
1	0	0	0	1	1	1	1	-2.50	1	0	0	0	1	1	1	1	-12.04
1	0	0	1	0	0	0	0	-2.68	1	0	0	1	0	0	0	0	-12.60
1	0	0	1	0	0	0	1	-2.87	1	0	0	1	0	0	0	1	-13.20
1	0	0	1	0	0	1	0	-3.06	1	0	0	1	0	0	1	0	-13.84
1	0	0	1	0	0	1	1	-3.25	1	0	0	1	0	0	1	1	-14.54
1	0	0	1	0	1	0	0	-3.45	1	0	0	1	0	1	0	0	-15.30
1	0	0	1	0	1	0	1	-3.66	1	0	0	1	0	1	0	1	-16.12
1	0	0	1	0	1	1	0	-3.87	1	0	0	1	0	1	1	0	-17.04
1	0	0	1	0	1	1	1	-4.08	1	0	0	1	0	1	1	1	-18.06
1	0	0	1	1	0	0	0	-4.30	1	0	0	1	1	0	0	0	-19.22
1	0	0	1	1	0	0	1	-4.53	1	0	0	1	1	0	0	1	-20.56
1	0	0	1	1	0	1	0	-4.76	1	0	0	1	1	0	1	0	-22.14
1	0	0	1	1	0	1	1	-5.00	1	0	0	1	1	0	1	1	-24.08
1	0	0	1	1	1	0	0	-5.24	1	0	0	1	1	1	0	0	-26.58
1	0	0	1	1	1	0	1	-5.49	1	0	0	1	1	1	0	1	-30.10
1	0	0	1	1	1	1	0	-5.75	1	0	0	1	1	1	1	0	-36.12
1	0	0	1	1	1	1	1	-6.02	1	0	0	1	1	1	1	1	$-\infty$

Table 5. KDA0340D Digital Attenuation Level

7. Power Supply Circuitry Structure

(1) The analog, digital, and X - tal supplies are separated.

(2) The digital supply is only one combination :

DV_{DD} / DV_{SS} applied to all the blocks except the analog, X - tal and system clock generation blocks

(3) The analog supply consists of two parts :

$AV_{DD}1$ / $AV_{SS}1$ / $AV_{DD}2$ applied to the output stage : OUTL (+), OUTL(-) circuits.

$AV_{DD}3$ / $AV_{SS}2$ / $AV_{DD}4$ applied to the outut stage : OUTR (+), OUTR (-), circuits.

(4) The X - tal supply is only one combination.

XV_{DD} / XV_{SS} applied to the x - tal and system clock generation blocks.

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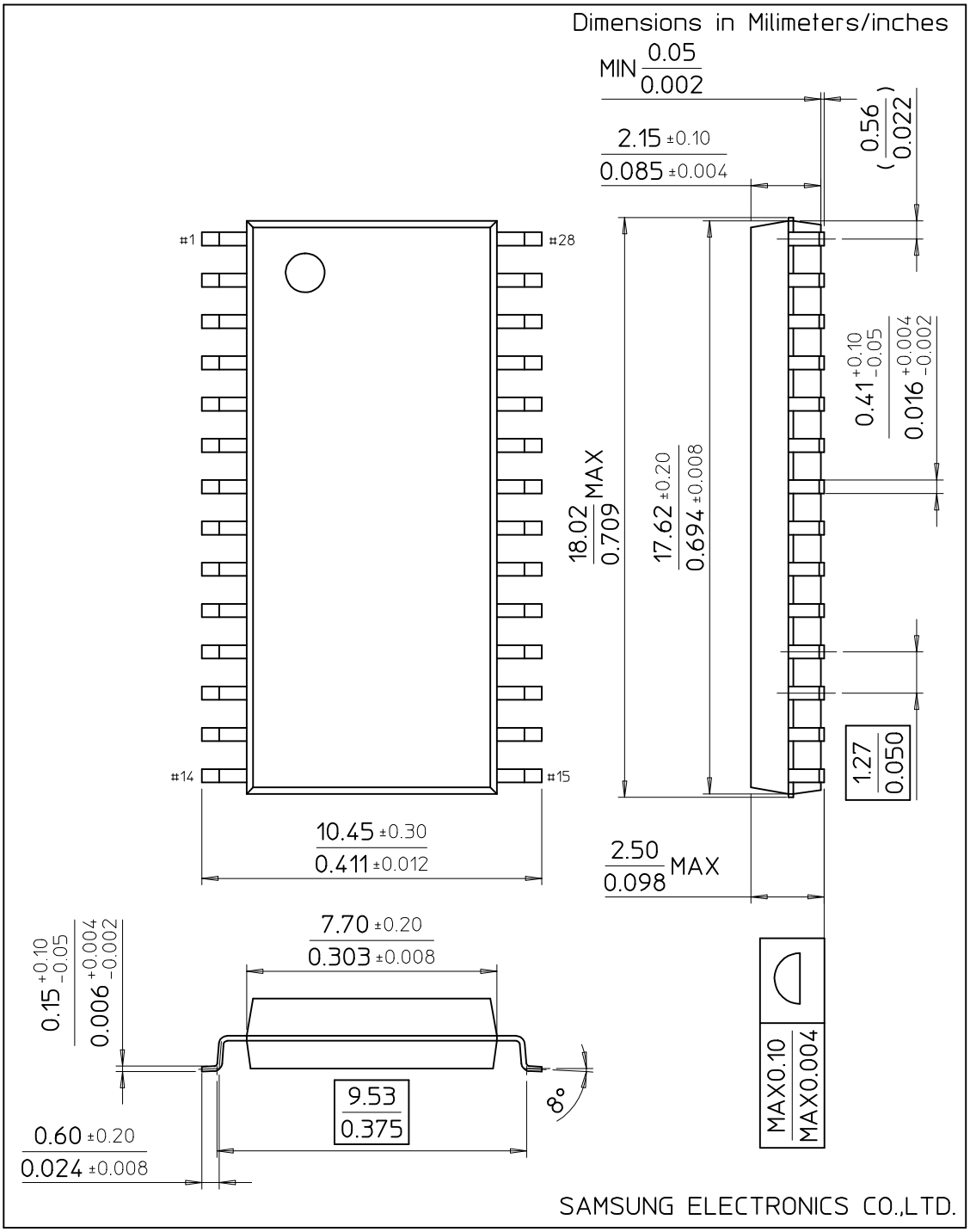
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2.15 ±0.10 / 0.085 ±0.004
(0.56 / 0.022)
#1
#28
#14
#15
18.02 / 0.709 MAX
17.62 ±0.20 / 0.694 ±0.008
0.41 +0.10 −0.05 / 0.016 +0.004 −0.002
1.27 / 0.050
10.45 ±0.30 / 0.411 ±0.012
2.50 / 0.098 MAX
7.70 ±0.20 / 0.303 ±0.008
0.15 +0.10 −0.05 / 0.006 +0.004 −0.002
9.53 / 0.375
8°
0.60 ±0.20 / 0.024 ±0.008
MAX0.10 / MAX0.004
SAMSUNG ELECTRONICS CO.,LTD.