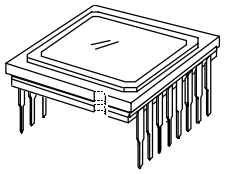
INTRODUCTION

The KC73125UC is an interline transfer CCD area image sensor developed for NTSC 1/3inch optical format video cameras, surveillance cameras, object detectors and image pattern recognizers. High sensitivity is achieved through the adoption of Ye, Cy, Mg and G complementary color mosaic filters, and on-chip micro lenses.
This chip features a field integration read-out system and an electronic shutter with variable charge storage time.

16 Pin Cer DIP



FEATURES

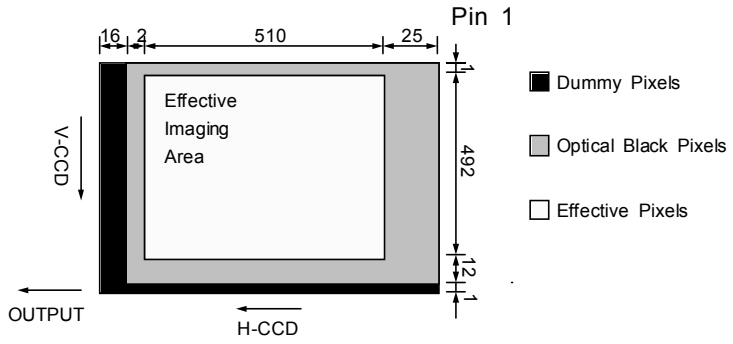
- High Sensitivity
- Optical Size 1/3inch Format
- Ye, Cy, Mg, G On-chip Complementary Color
- Mosaic Filter
- Variable Speed Electronic Shutter
- Low Dark Current
- Horizontal Register 5V Drive
- 16pin Ceramic DIP Package
- Field Integration Read-Out System

ORDERING INFORMATION

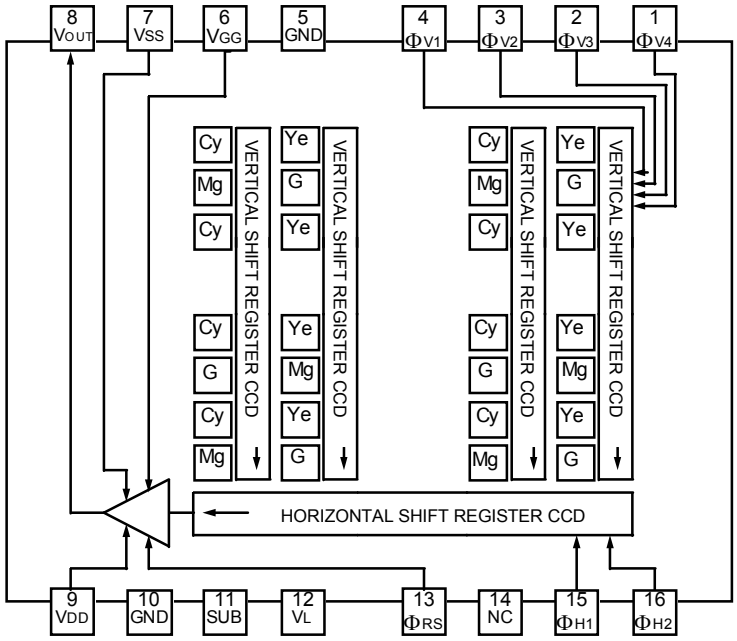
Device	Package	Operating Temperature
KC73125UC	16 pin Cer DIP	-10°C ~ +50°C

STRUCTURE

· Number of total pixels : 537 (H) × 505 (V)
· Number of effective pixels : 510 (H) × 492 (V)
· Chip size : 6.00mm(H) × 4.95mm(V)
· Unit pixel size : 9.60μm(H) × 7.50μm(V)
· Optical blacks & dummies : Refer to figure below



BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Symbol	Description	Pin	Symbol	Description
1	ϕ_{V4}	Vertical CCD Transfer Clock 4	9	V_{DD}	Output Stage Drain Bias
2	ϕ_{V3}	Vertical CCD Transfer Clock 3	10	GND	Ground
3	ϕ_{V2}	Vertical CCD Transfer Clock 2	11	SUB	Substate Bias
4	ϕ_{V1}	Vertical CCD Transfer Clock 1	12	V_L	Protection Bias
5	GND	Ground	13	ϕ_{RS}	Charge Reset Clock
6	V_{GG}	Output Stage Gate Bias	14	NC	No Connection
7	V_{SS}	Output Stage Gate Bias	15	ϕ_{H1}	Horizontal CCD Transfer Clock 1
8	V_{OUT}	Signal Output	16	ϕ_{H2}	Horizontal CCD Transfer Clock 2

ABSOLUTE MAXIMUM RATINGS* (1)

Characteristics	Symbol	Min.	Max.	Unit.
Substrate Voltage	SUB-GND	-0.3	55	V
Supply Voltage	V_{DD},V_{OUT},V_{SS}-GND	-0.3	17	V
Vertical Clock Input Voltage	ϕ_{V1},ϕ_{V2},ϕ_{V3},ϕ_{V4}-GND	-15	30	V
	ϕ_{V1},ϕ_{V2},ϕ_{V3},ϕ_{V4}-V_L	-0.3	30	V
Horizontal Clock Input Voltage	ϕ_{H1},ϕ_{H2} - GND	-0.3	20	V
Voltage Difference between Vertical and Horizontal Clock Input Pins	ϕ_{V1},ϕ_{V2},ϕ_{V3},ϕ_{V4}	-30	30	V
	ϕ_{H1},ϕ_{H2}	-20	20	V
	ϕ_{H1},ϕ_{H2} - ϕ_{V4}	-30	30	V
Output Clock	ϕ_{RG},V_{GG} - GND	-0.3	20	V
Protection Circuit Bias Voltage	V_L - SUB	-55	0.3	V
Operating Temperature	T_{OPR}	-10	50	°C
Storage Temperature	T_{STG}	-30	80	°C

*(1) The device can be destroyed, if the applied voltage or temperature is higher than the absolute maximum rating voltage or temperature.

DC CONDITIONS

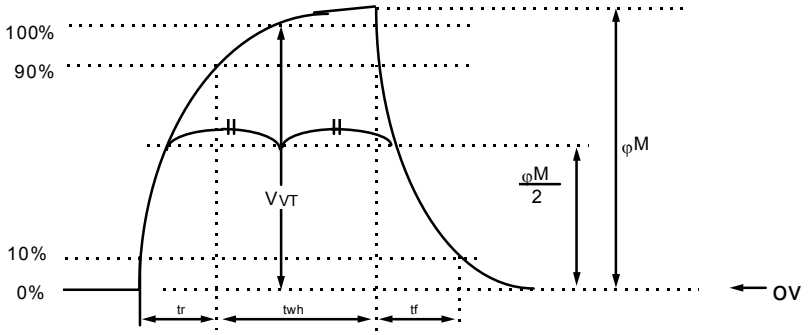
Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Output Stage Drain Bias	V_{DD}	14.55	15.0	15.45	V	
Protection Circuit Bias Voltage	V_L	The lowest vertical clock level				
Output Stage Drain Current	I_{DD}		2.5mA	3.0mA	mA	

CLOCK VOLTAGE CONDITIONS

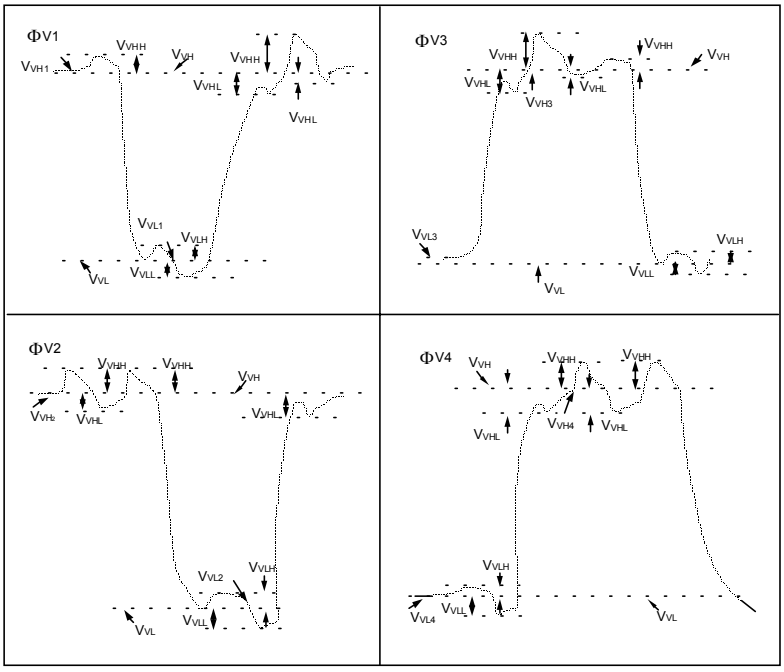
Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Read-out Clock Voltage	V_{VH1}, V_{VH3}	14.55	15.0	15.45	V	High level
Vertical Transfer Clock Voltage	V_{VM1} ~ V_{VM4}	-0.05	0.0	0.05	V	Middle level
	V_{VL1} ~ V_{VL4}	-9.5	-9.0	-8.5	V	Low level
Horizontal Transfer Clock Voltage	$V_{\phi H}$	4.75	5.0	5.25	V	High
	V_{HL}	-0.05	0.0	0.05	V	Low
Charge Reset Clock Voltage	V_{RSH}	4.75	5.0	5.25	V	High
	V_{RSL}	-0.05	0.0	0.05	V	Low
Clock Voltage	V_{RGLH} -V_{RGLL}			0.8	V	Low
Substrate Clock Voltage	$V_{\phi SUB}$	20.0	23.0	25.0	V	Shutter

DRIVE CLOCK WAVEFORM CONDITIONS

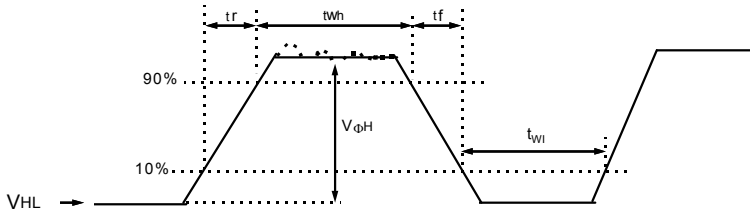
(1) Read out clock waveform



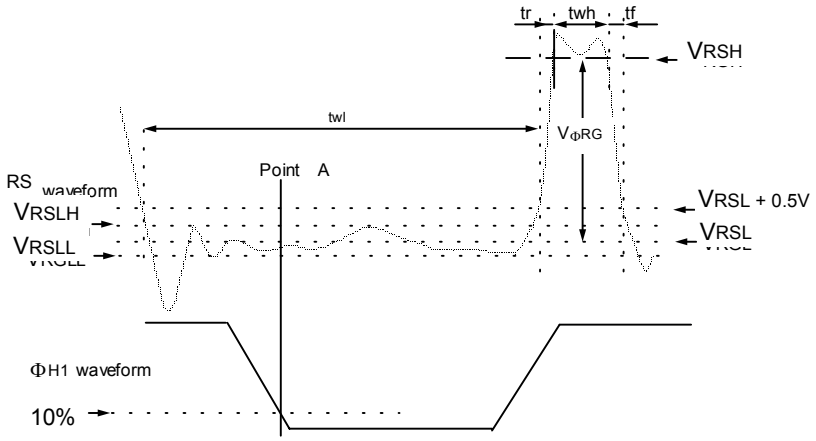
(2) Vertical transfer clock waveform



(3) Horizontal transfer clock waveform diagram



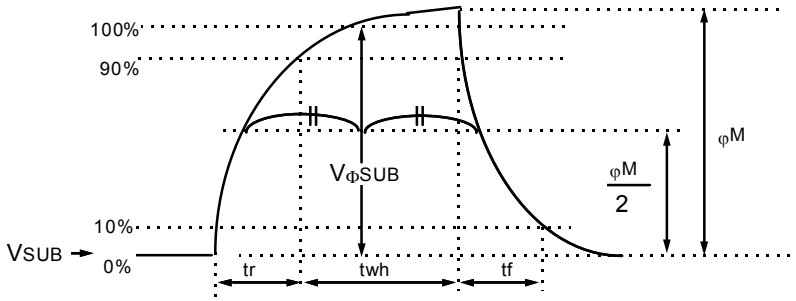
(4) Reset gate clock waveform diagram



V_{RGLH} is the maximum value and V_{RGLL} the minimum value of the coupling waveform in the period from Point A in the diagram about to RG rise

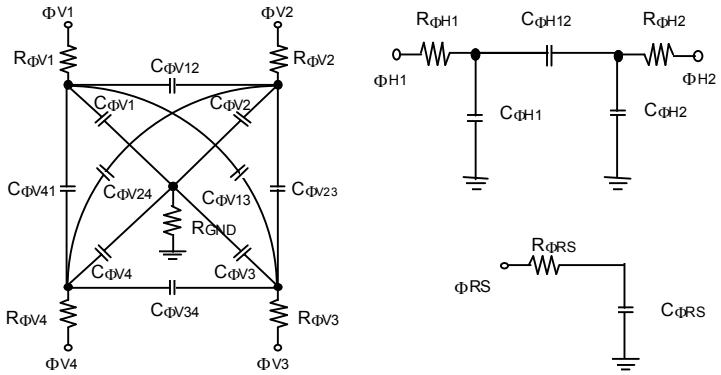
$V_{RGL}=(V_{RGLH}+V_{RGLL})/2$, $V_{\varphi RG}=V_{RGH}-V_{RGL}$

(5) Substrate clock waveform



CLOCK EQUIVALENT CIRCUIT CONSTANT

Item	Symbol	Typ.	Unit	Remark
Capacitance between Vertical Transfer Clock and GND	$C_{\phi V1}$, $C_{\phi V3}$	1,300	pF	
	$C_{\phi V2}$, $C_{\phi V4}$	1,300	pF	
Capacitance between Vertical Transfer Clocks	$C_{\phi V12}$, $C_{\phi V34}$	600	pF	
	$C_{\phi V23}$, $C_{\phi V41}$	230	pF	
	$C_{\phi V13}$	120	pF	
	$C_{\phi V24}$	90	pF	
Capacitance between Horizontal Transfer Clock and GND	$C_{\phi H1}$, $C_{\phi H2}$	38	pF	
Capacitance between Horizontal Transfer Clocks	$C_{\phi H12}$	38	pF	
Capacitance between Reset Gate Clock and GND	$C_{\phi RS}$	10	pF	
Capacitance between Substrate Clock and GND	$C_{\phi SUB}$	1120	pF	
Vertical Transfer Clock Serial Resistor	$R_{\phi V1}$ ~ $R_{\phi V4}$	40	Ω	
Vertical Transfer Clock Ground Resistor	R_{GND}	15	Ω	
Horizontal Transfer Clock Serial Resistor	$R_{\phi H1}$, $R_{\phi H2}$	10	Ω	
Reset Gate Clock Serial Resistor	$R_{\phi RS}$	100	Ω	

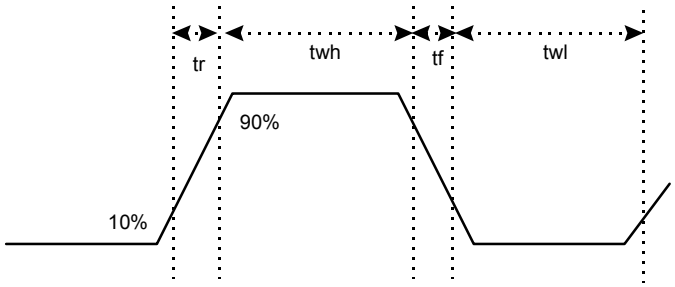


SAMSUNG ELECTRONICS

CLOCK SWITCHING CHARACTERISTICS

Item	Symbol	twh			twl			tr			tf			unit
		min	typ	max	min	typ	max	min	typ	max	min	typ	max	
Read-out Clock	Φ_{VH}		2.5						0.5			0.5		μs
Vertical Clock	Φ_{V1}, Φ_{V2} Φ_{V3}, Φ_{V4}										15		250	ns
Horizontal Clock	Φ_{H1}	37	41		38	42			12	15		10	15	ns
	Φ_{H2}	37	41		38	42			12	15		10	15	ns
Reset Clock	Φ_{RS}	11	15		75	79			6.5			4.5		ns
Substrate Clock	Φ_{SUB}	1.5	2.0							0.5			0.5	μs

* The twh, twl, tr, tf are as plotted in the figure below.



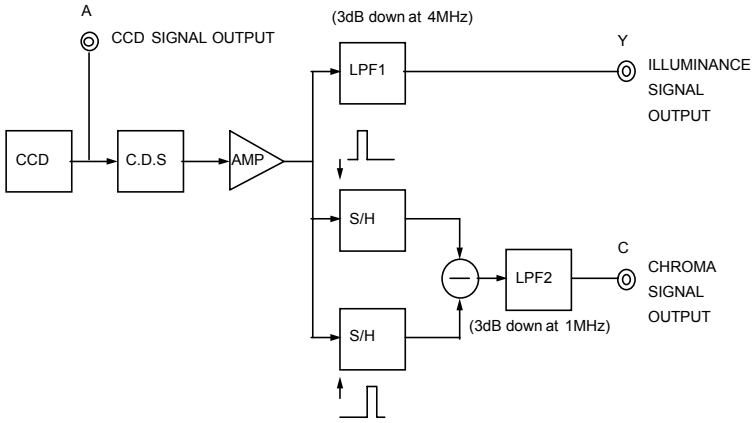
Clock Voltage Diagram

IMAGE SENSOR CHARACTERISTICS

(Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remark
Sensitivity	S	35	45		mV/lux	1	
Saturation Signal	Y_{SAT}	600			mV	2	
Smear	SM			0.015	%	3	
Blooming Margin	BM	1,000			times	4	
Uniformity	U			20	%	5	
Dark Signal	D			2	mV	6	Ta=50°C
Flicker Y	F_Y			2	%	7	
Flicker Red, Blue	F_{CR},F_{CB}			5	%	8	
Color Uniformity	D_{SR},D_{SB}			10	%	9	
Line Stripe W,R,G,B	L_{CW},L_{CR}, L_{CG},L_{CB}			2	%	10	

TESTING SYSTEM



NOTE) Adjust AMP gain so that total gains between A and Y and between A and C equal 1

TEST CONDITIONS

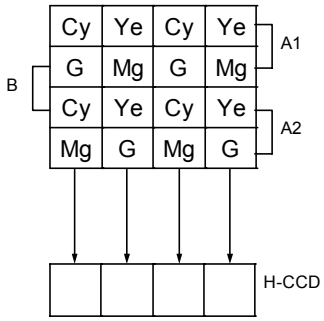
1) Use a light source with the color temperature of 3,200 K, and CM-500S as IR cut filter. The light source is adjusted in accordance with the average value of Y signals indicated in each item.

2) Through the following tests, the substrate voltage and reset gate clock are set to the value of the bias condition, while the device conditions are at the typical value of the bias and clock conditions.

3) Through the following tests, defects are excluded and unless otherwise specified the optical black level (henceforth referred as OB) is set for the reference of the output signal which is taken as the Y signal output or chroma signal output for the test system.

COLOR FILTER ARRAY

The color filter array of this image sensor is shown in the figure to the right. This complementary mosaic CFA is used with the operation of field integration mode, where all of the photosensors are read out during each video field. The signals from two vertically-adjacent photosensor lines, such as line couple A1 or A2 for field A are summed when the signal charges are transferred into the vertical transfer CCD column. The read-out line pairing is shifted down by one line for field B. The sensor output signals through the horizontal register (H-CCD) at line A1 are [G+Cy], [MG+Ye], [G+CY], and [Mg+Ye]. These signals are processed in order to compose Y and C signals. By adding the two adjacent signals at line A1, Y signal is formed as follows.



$$= \tfrac{1}{2}[(G + Cy) + (Mg + Ye)]$$
$$= \tfrac{1}{2}(2B + 3G + 2R)$$

C signal is composed by substracting the two adjacent signals at line A1.

$$R - Y = [(Mg + Ye) - (G + Cy)]$$
$$= (2R - G)$$

Next, the signals through H-CCD at line A2 are [Mg+Cy], [G+Ye], [Mg+Cy], and [G+Ye]. Similarly, Y and C signals are composed at line A2 as follows.

$$= \tfrac{1}{2}[(G + Ye) + (Mg + Cy)]$$
$$= \tfrac{1}{2}(2B + 3G + 2R)$$

$$-(B - Y) = [(G + Ye) - (Mg + Cy)]$$
$$= -(2B - G)$$

Accordingly, Y signal is balanced in relation to scanning lines, and C signal takes the form of R-Y and -(B-Y) on alternate lines. It is same for B field.

TEST METHODS

1. Measure the light intensities(L) when the averaged illuminance output value(Y) is the standard illuminance output value, 150mV(Y_A) and when half of 150mV(1/2 Y_A).

$$S = \frac{Y_A - \frac{1}{2}Y_A}{L_{Y_A} - L_{\frac{1}{2}Y_A}}$$

2. Adjust the light intensity to 10 times that of the Y signal output average value (Y_A = 150mV) , then test the Y signal minimum value ($Y=Y_{SAT}$).

3. Adjust the light intensity to 500 times that of the Y signal output average value (Y_A=150mV), then remove the read-out clock and drain the signal in photosensors by the electronic shutter operation in all the respective horizontal blanking times with the other clocks unchanged. Measure the maximum illuminance output value (Y_{SM}).

$$SM = \frac{Y_{SM}}{Y_A} \times \frac{1}{500} \times \frac{1}{10} \times 100(\%)$$

4. Adjust the light intensity to 1000 times that of the Y signal output average value (Y_A=150mV), then confirm that blooming does not appear.

5. Measure the maximum and minimum illuminance output value (YMAX, YMIN) when the light intensity is adjusted to make Y to be Y_A.

   U = (YMAX - YMIN) /YA X 100. (%)

6. Measure the Y signal output average value Y_D[mV] with the horizontal idling time transfer level as reference, when the device ambient temperature is 50°C, and all of the light sources are shielded.

7. Adjust the light intensity to make $Y=Y_A$. Measure the difference value (ΔY_F) between the averaged illuminance signal values of the even and odd fields.

$$F_Y = \frac{\Delta Y_F}{Y_A} \text{ x100 (\%)}$$

8. Adjust the light intensity to make Y=YA.Then insert red (R) and blue (B) optical filters respectively, measure the differences (ΔC_R, ΔC_B) between the chroma signal values in even and odd fields, and the C signal output average value (C_R, C_B).

$$F_{C_i} = \frac{\Delta C_i}{C_i} \times 100(\%) \quad , \quad \text{where i = R, B}$$

9. Adjust the light intensity to make $Y=Y_A$. Then test maximum ($C_{R,MAX}$and $C_{B,MAX}$) and minimum ($C_{R,MIN}$ and $C_{B,MIN}$) values of chroma signals from R-Y and B-Y channels.

$$DS_i = \frac{C_{i,MAX} - C_{i,MIN}}{Y_i} \times 100(\%) \text{ , where i = R, B}$$

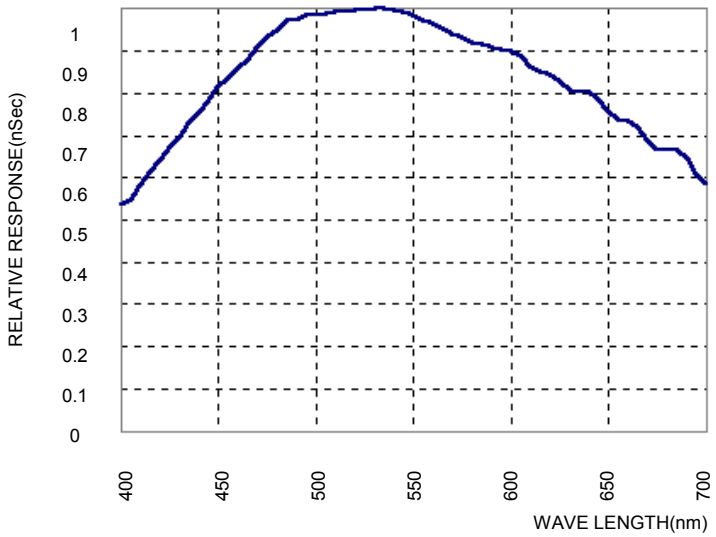
10. Adjust the light intensity to make Y=150mV(Y_L).Then insert white (no filter, W), red(R), green(G) and blue(B) optical filters respectively, and measure the illuminance signal difference values (ΔY_{LW}, ΔY_{LR}, ΔY_LG, ΔY_{LB}) between illuminance signal lines of the same field.

$$L_{C_i} = \frac{\Delta Y_{L_i}}{Y_L} \times 100(\%) \quad \text{, where i = W, R, G, B}$$

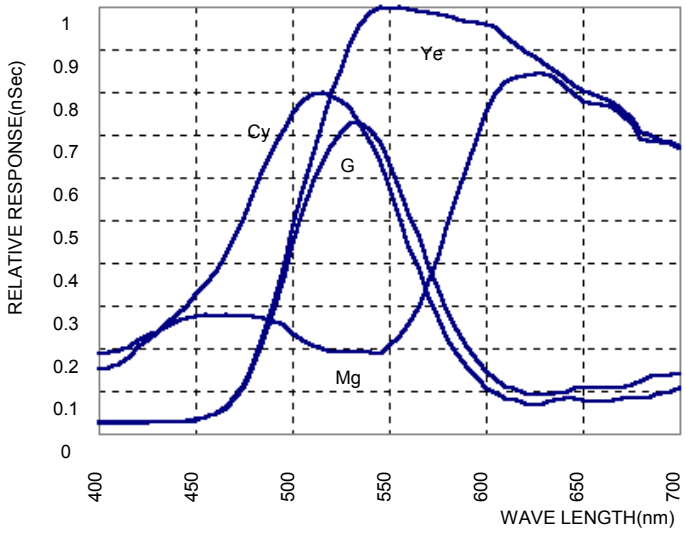
SPECTRAL SENSITIVITY CHARACTERISTICS

(Excluding light source characteristics)

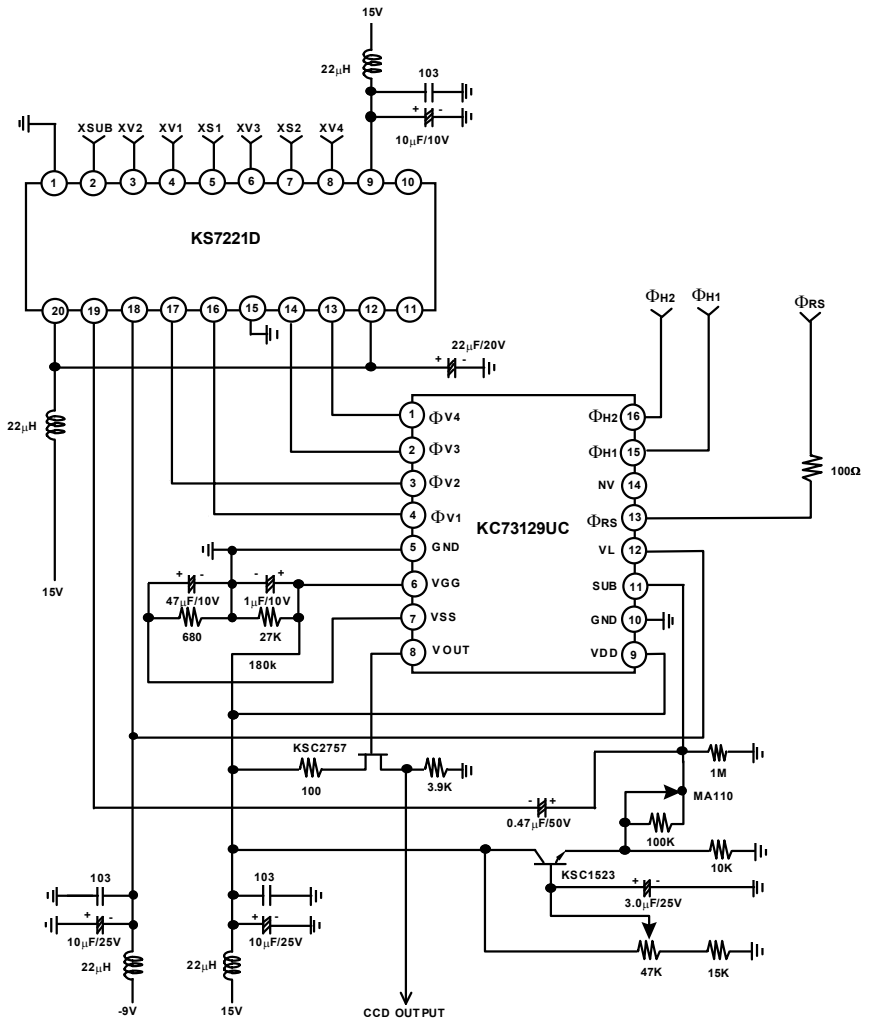
WITHOUT COLOR FILTER



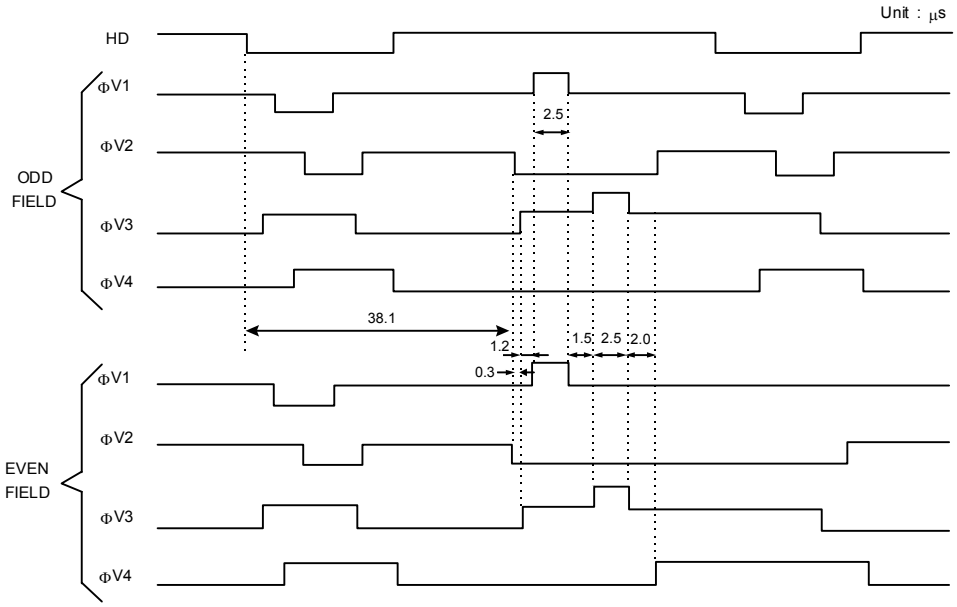
COLOR SPECTRAL CHARACTERISTICS



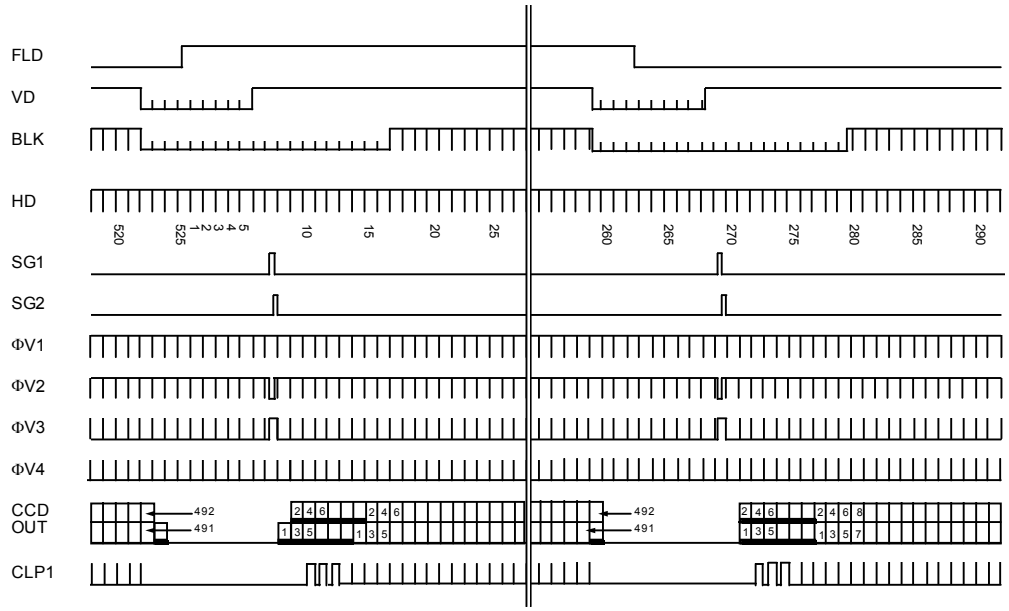
APPLICATION CIRCUITS



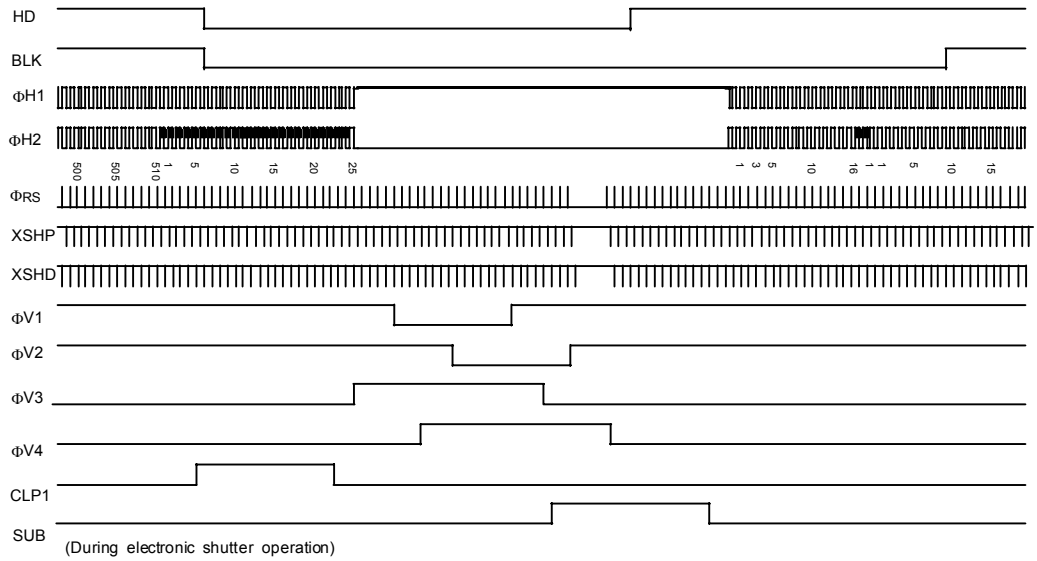
READ-OUT CLOCK TIMING CHART



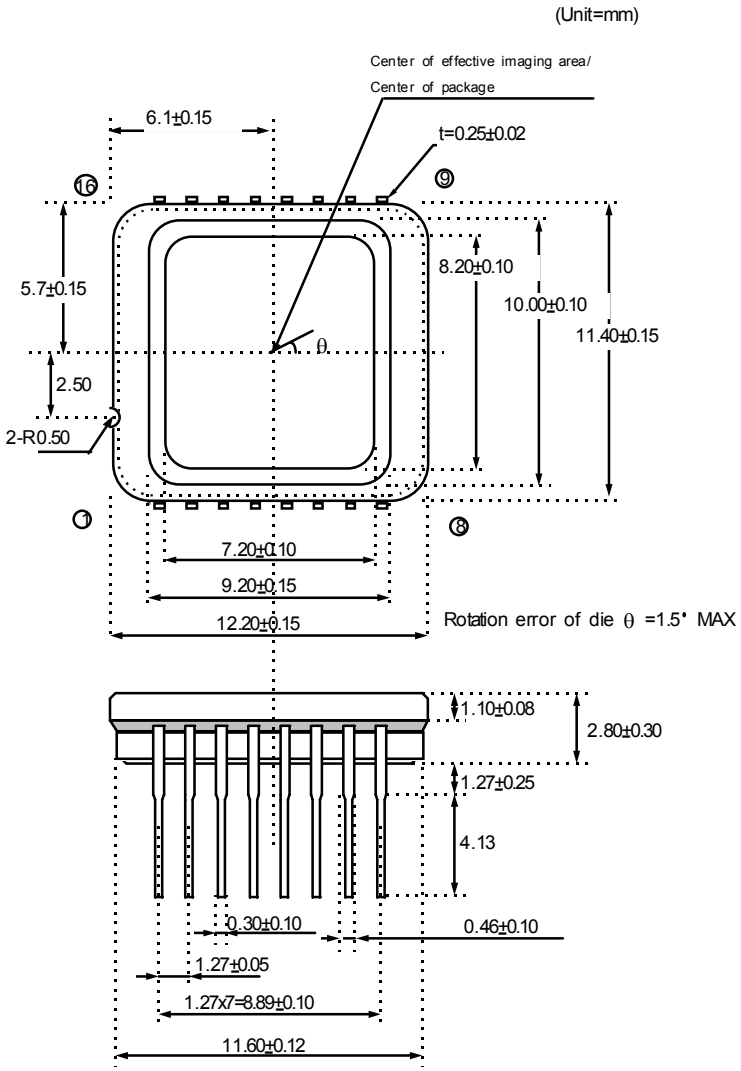
CLOCK TIMING CHART (VERTICAL SYNC.)



CLOCK TIMING CHART (HORIZONTAL SYNC.)



PACKAGE DIMENSIONS



1. Optical center deviation from mechanical center = ± 0.15mm for X and Y direction.
2. Optical surface height from glass lid surface = 1.1 ±0.15mm
3. Optical surface height from package backside bottom = 1.7±0.10mm

HANDLING INSTRUCTIONS

1. Static charge prevention

CCD image sensors can be easily damaged by static discharge. Before handling be sure to take the following protective measures.

1) Either handle bare-handed or use non-chargeable gloves, clothes or material. Also, use conductive shoes.
2) When handling directly, use an earth band.
3) Install a conductive mat on the floor or working table to prevent generation of static electricity.
4) Ionized air is recommended for discharging when handling CCD image sensor.
5) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2. Soldering

1) Make sure the package temperature does not exceed 80°C.
2) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
3) To dismount an imaging device, do not use solder suction equipment. When using an electronic disoldering tool, use a thermal controler of the zero cross On/Off type and connect to ground.

3. Dust and Dirt protection

1) Operate in clean environment (about class 1000 will be appropriate).
2) Do not touch glass plates by hand or have an object be in contact with the glass surface. Should dirt stick to a glass surface, blow it off with an air blow (for dirt stuck through static electricity, ionized air is recommended).
3) Clean with a cotton bud and ethyl alcohol if the glass surface is stained with grease. Be carful not to scratch the glass.
4) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room whith great temperature differences.
5) When a protective tape is applied before shipping, just before use, remove the tape applied for electrostatic protection. Do not reuse the tape.

4. Do not expose to strong light (sun light) for a long period. The Color filter will be discolored.

5. Exposure to high temperatures or humidity will affect the characteristics. Accordingly, avoid storage or usage in such conditions.

6. CCD image sensor is precise optical device, and should not be subjected to mechanical shocks.