FAIRCHILD SEMICONDUCTOR®

December 2012

KA431 / KA431A / KA431L
Programmable Shunt Regulator

Features

- Programmable Output Voltage to 36 V
- Low Dynamic Output Impedance: 0.2 Ω Typical
- Sink Current Capability: 1.0 to 100 mA
- Equivalent Full-Range Temperature Coefficient of 50 ppm/°C (Typical)
- Temperature Compensated for Operation Over Full Rated Operating Temperature Range
- Low-Output Noise Voltage
- Fast Turn-on Response

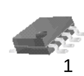
Description

The KA431 / KA431A / KA431L are three-terminal adjustable regulators with a guaranteed thermal stability over applicable temperature ranges. The output voltage may be set to any value between V_{REF} (approximately 2.5 V) and 36 V with two external resistors. These devices have a typical dynamic output impedance of 0.2 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for Zener diodes in many applications.

TO-92

1. Ref 2. Anode 3. Cathode

8-SOIC



1.Cathode 2.3.6.7.Anode
4.5.NC 8.Ref

Ordering Information

Part Number	Operating Temperature Range	Output Voltage Tolerance	Top Mark	Package	Packing Method
KA431DTF	-25 ~ +85°C	2%	431	8-SOIC	Tape and Reel
KA431ADTF		1%	431A	8-SOIC	Tape and Reel
KA431AZBU			KA431AZ	TO-92	Bulk
KA431AZTA			KA431AZ	TO-92	Ammo
KA431LZTA		0.5%	KA431LZ	TO-92	Ammo

Block Diagram

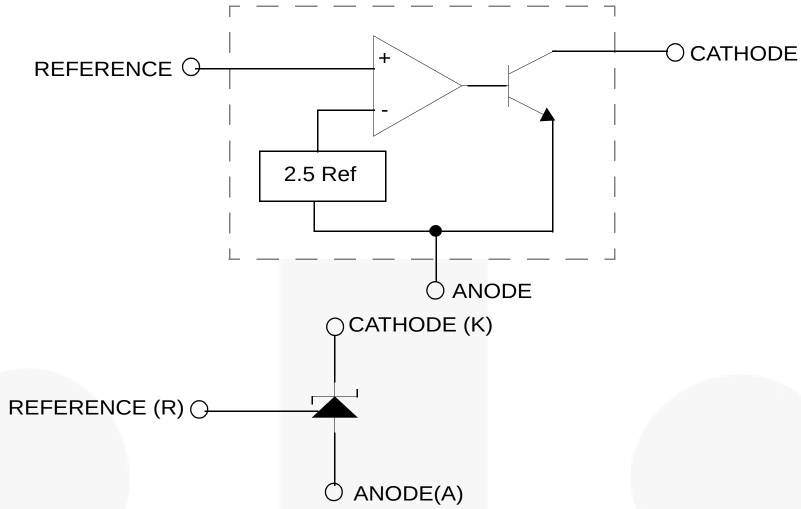


Figure 1. Block Diagram

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{KA}	Cathode Voltage	37	V
I_{KA}	Cathode Current Range (Continuous)	-100 ~ +150	mA
I_{REF}	Reference Input Current Range	-0.05 ~ +10	mA
P_D	Power Dissipation D, Z Suffix Package	770	mW
T_{OPR}	Operating Temperature Range	-25 ~ +85	°C
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 ~ +150	°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{KA}	Cathode Voltage	V_{REF}	36	V
I_{KA}	Cathode Current	1.0	100	mA

Electrical Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions		KA431			KA431A			KA431L			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{REF}	Reference Input Voltage	$V_{KA} = V_{REF}$, I_{KA} = 10 mA		2.450	2.500	2.550	2.470	2.495	2.520	2.482	2.495	2.508	V
$\Delta V_{REF}/\Delta T$	Deviation of Reference Input Voltage Over-Temperature	$V_{KA} = V_{REF}$, I_{KA} =10 mA $T_{MIN} \le T_A \le T_{MAX}$ (1)			4.5	17.0		4.5	17.0		4.5	17.0	mV
$\Delta V_{REF}/\Delta V_{KA}$	Ratio of Change in Reference Input Voltage to the Change in Cathode Voltage	I_{KA} = 10 mA	ΔV_{KA} = 10V-V_{REF}		-1.0	- 2.7		-1.0	- 2.7		-1.0	-2.7	mV / V
			ΔV_{KA} = 36 V-10 V		-0.5	-2.0		-0.5	-2.0		-0.5	-2.0	
I_{REF}	Reference Input Current	I_{KA} = 10 mA, R1 =10 kΩ, R2 = ∞			1.5	4		1.5	4		1.5	4	µA
$\Delta I_{REF}/\Delta T$	Deviation of Reference Input Current Over Full Temperature Range	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞ T_A = Full Range			0.4	1.2		0.4	1.2		0.4	1.2	µA
$I_{KA(MIN)}$	Minimum Cathode Current for Regulation	$V_{KA} = V_{REF}$			0.45	1.0		0.45	1.0		0.45	1.0	mA
$I_{KA(OFF)}$	Off - Stage Cathode Current	V_{KA} = 36 V, V_{REF} = 0			0.05	1.0		0.05	1.0		0.05	1.0	µA
Z_{KA}	Dynamic Impedance	$V_{KA} = V_{REF}$, I_{KA} =1 to 100 mA f ≥ 1.0 kHz			0.15	0.5		0.15	0.5		0.15	0.5	Ω

Note:

1. T_{MIN} = -25°C, T_{MAX} = +85°C.

Test Circuits

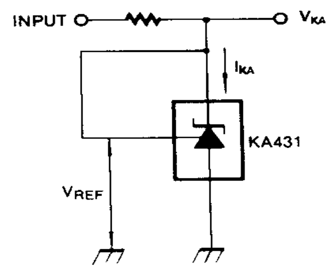


Figure 2. Test Circuit for $V_{KA} = V_{REF}$

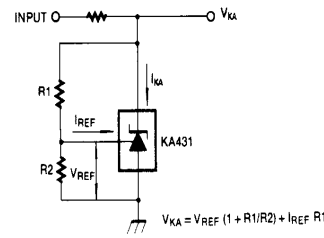


Figure 3. Test Circuit for $V_{KA} \geq V_{REF}$

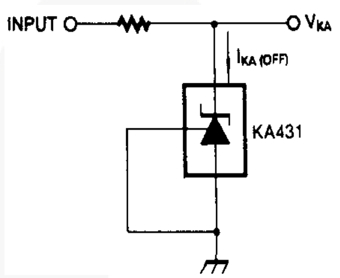


Figure 4. Test Circuit for $I_{KA(OFF)}$

Typical Performance Characteristics

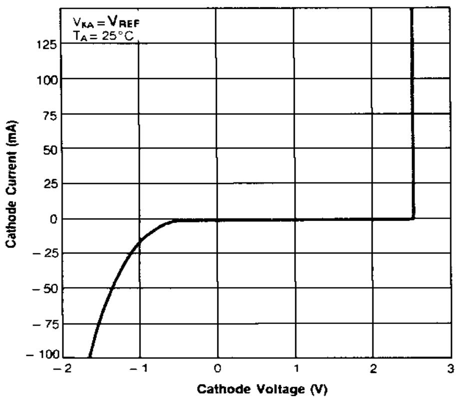


Figure 5. Cathode Current vs. Cathode Voltage

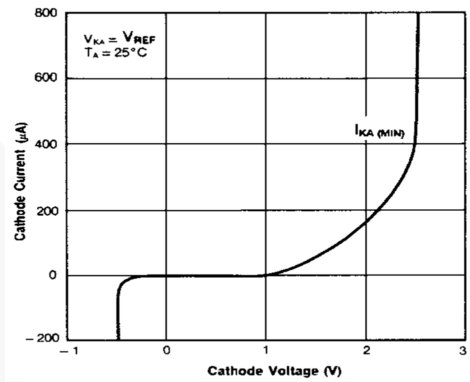


Figure 6. Cathode Current vs. Cathode Voltage

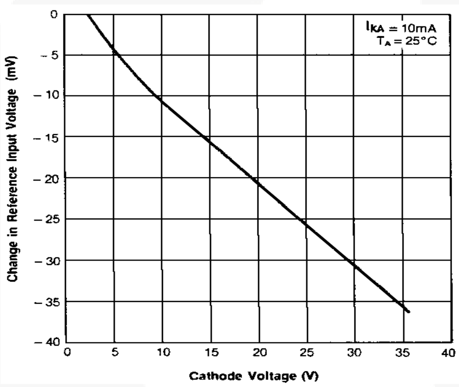


Figure 7. Change In Reference Input Voltage vs. Cathode Voltage

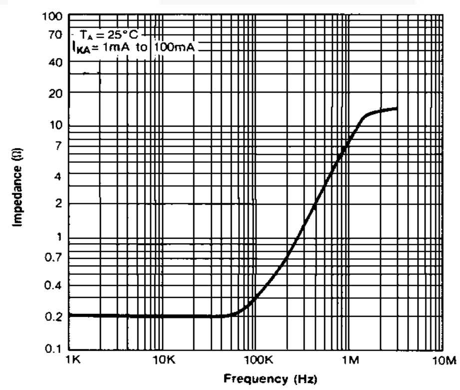


Figure 8. Dynamic Impedance Frequency

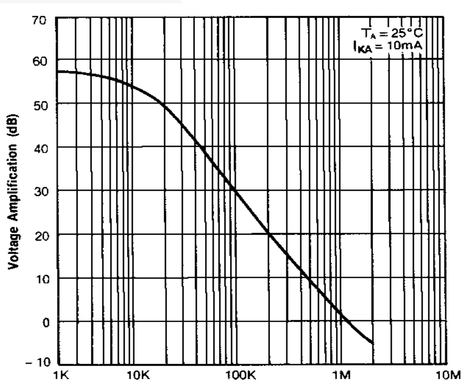


Figure 9. Small Signal Voltage Amplification vs. Frequency

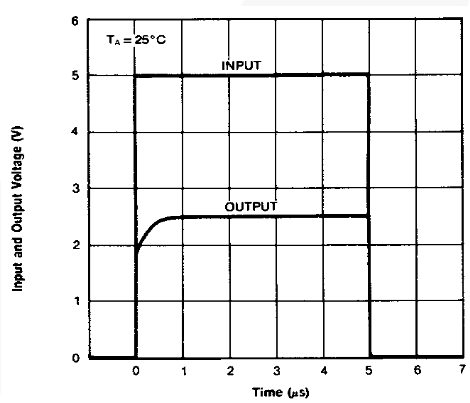


Figure 10. Pulse Response

Typical Performance Characteristics (Continued)

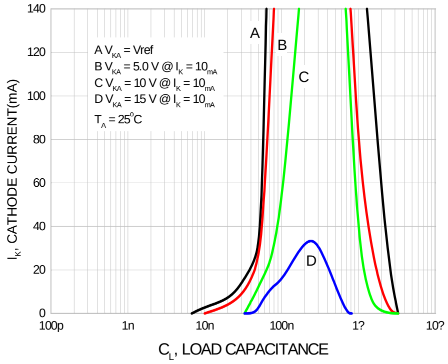


Figure11. Stability Boundary Conditions

Typical Application

$$V_O = \left(1 + \frac{R_1}{R_2}\right)V_{ref}$$

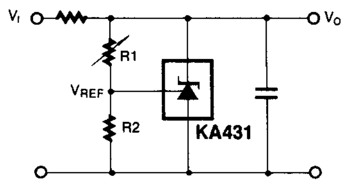


Figure 12. Shunt Regulator

$$V_O = V_{ref}\left(1 + \frac{R_1}{R_2}\right)$$

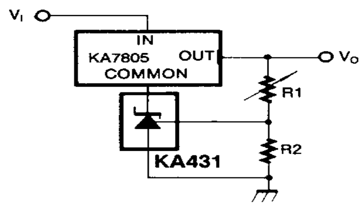


Figure 13. Output Control for Three-Terminal Fixed Regulator

$$V_O = \left(1 + \frac{R_1}{R_2}\right)V_{ref}$$

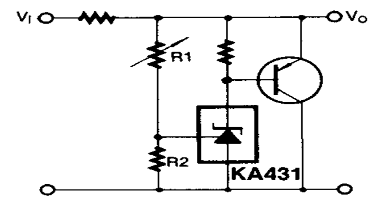


Figure 14. High-Current Shunt Regulator

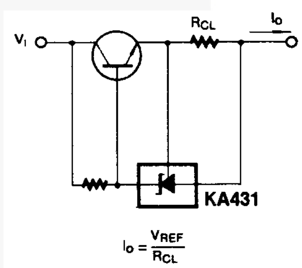


Figure 15. Current Limit or Current Source

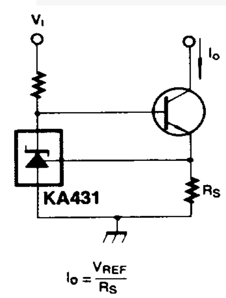
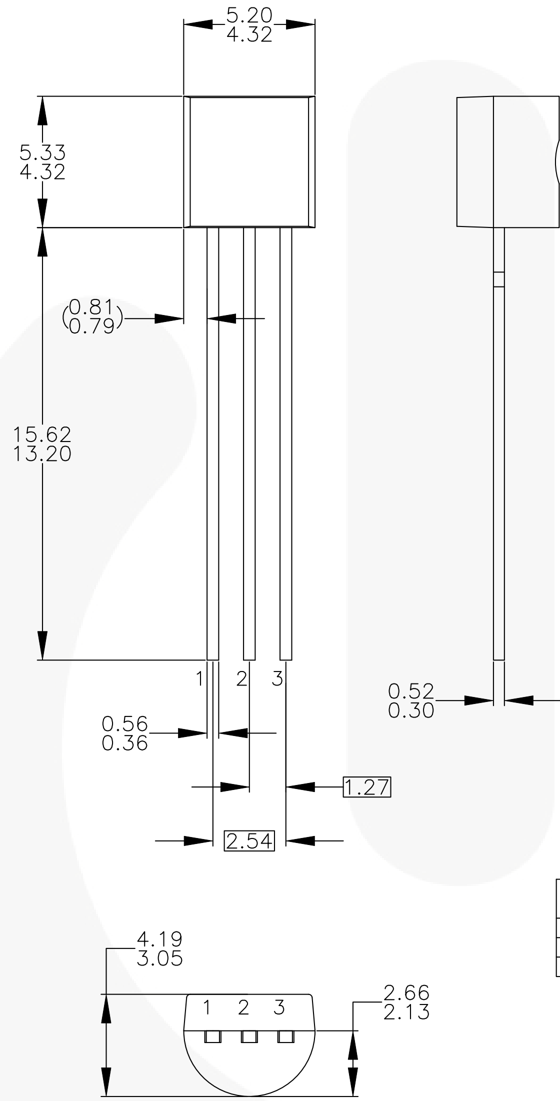


Figure 16. Constant-Current Sink

Physical Dimensions

TO-92 Bulk Type



NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO−92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M−1994.
D) TO−92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P − BIPOLAR   E − EMITTER   D − DRAIN
F − JFET   B − BASE   S − SOURCE
M − DMOS   C − COLLECTOR   G − GATE

E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT−ZA03DREV3.

Figure 17. 3-Lead, TO-92, Molded, Standard Straight Lead

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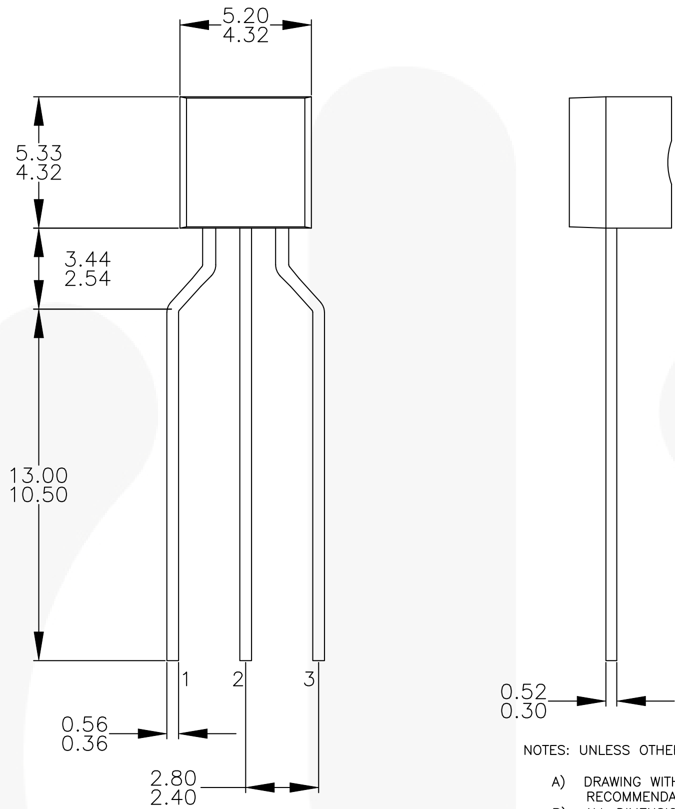
Physical Dimensions (Continued)

TO-92 Ammo Type



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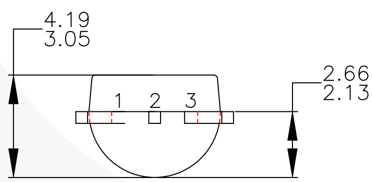
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M-1994.
D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P – BIPOLAR
F – JFET
M – DMOS
E – EMITTER
B – BASE
C – COLLECTOR
D – DRAIN
S – SOURCE
G – GATE



E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT-ZA03FREV2.

Figure 18. 3-Lead, TO-92, Molded, 0.200 in Line Spacing Lead Form

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Physical Dimensions (Continued)

8-SOIC

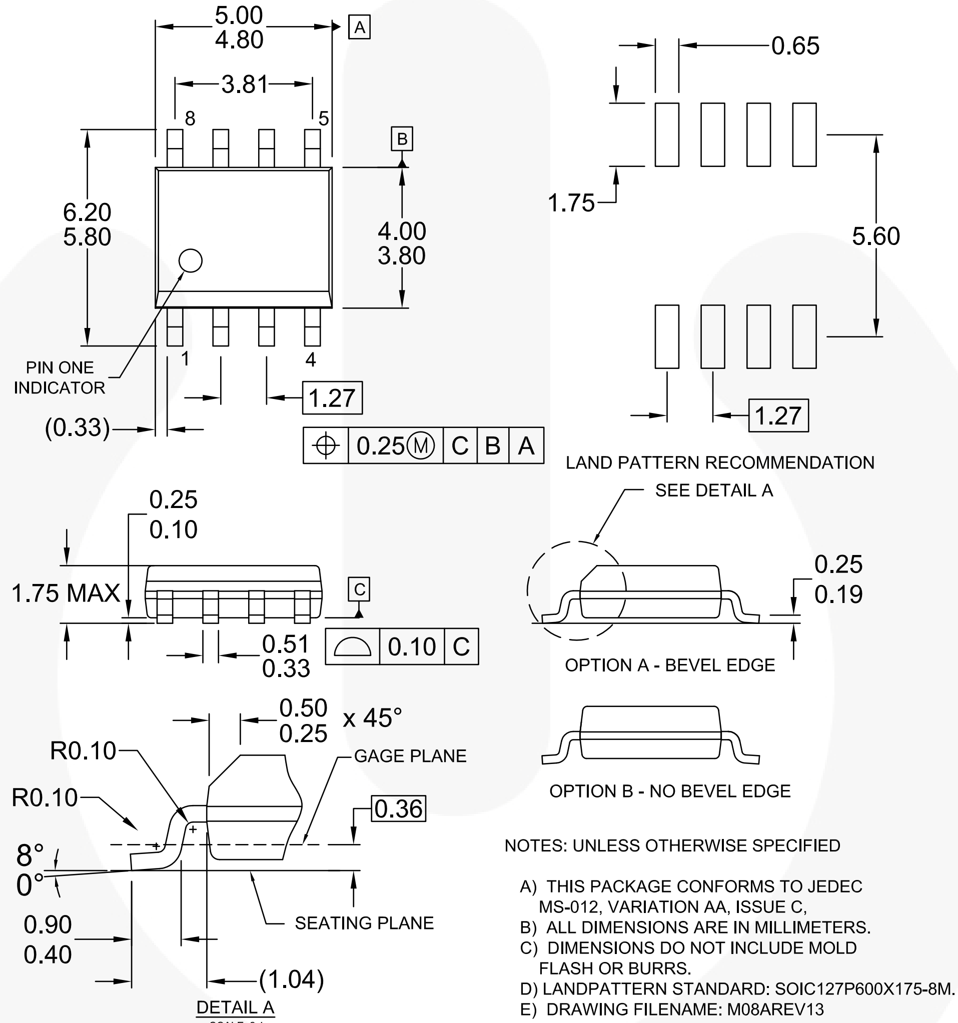

Figure 19. 8-Lead, SOIC, JEDEC MS 0-12, 0.150 inch Narrow Body

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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