TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

JT6J14-AS

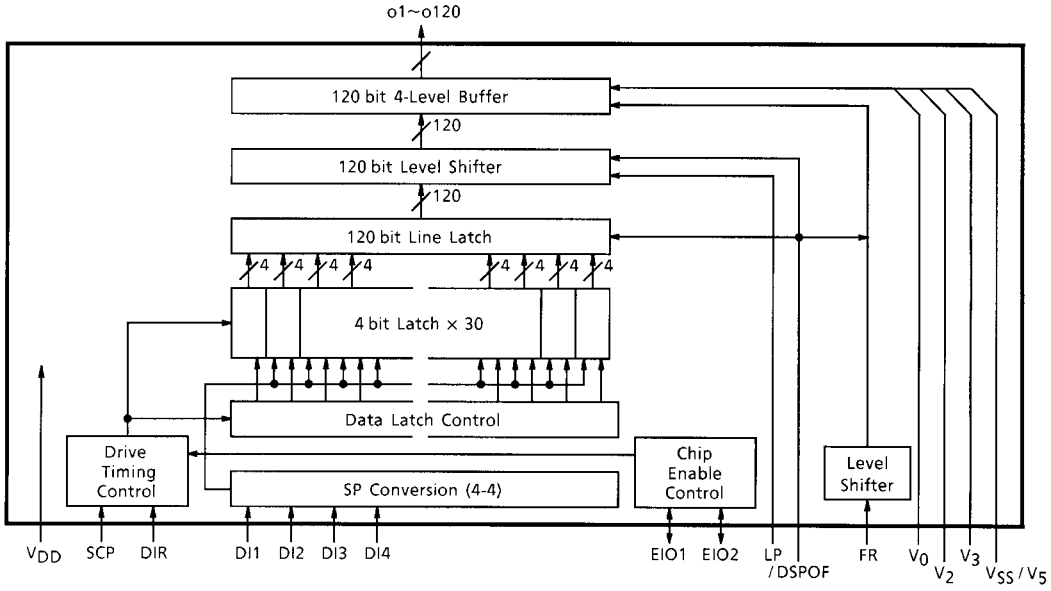
COLUMN DRIVER FOR A DOT MATRIX LCD

The JT6J14-AS is a 120-channel-output column driver for a STN dot matrix LCD. The JT6J14-AS features a 28-V LCD drive voltage and a 10 MHz maximum operating frequency. The JT6J14-AS is able to drive LCD panels with a duty ratio of up to 1/160.
The JT6J14-AS is recommended for use with the JT6J15A-AS row driver.

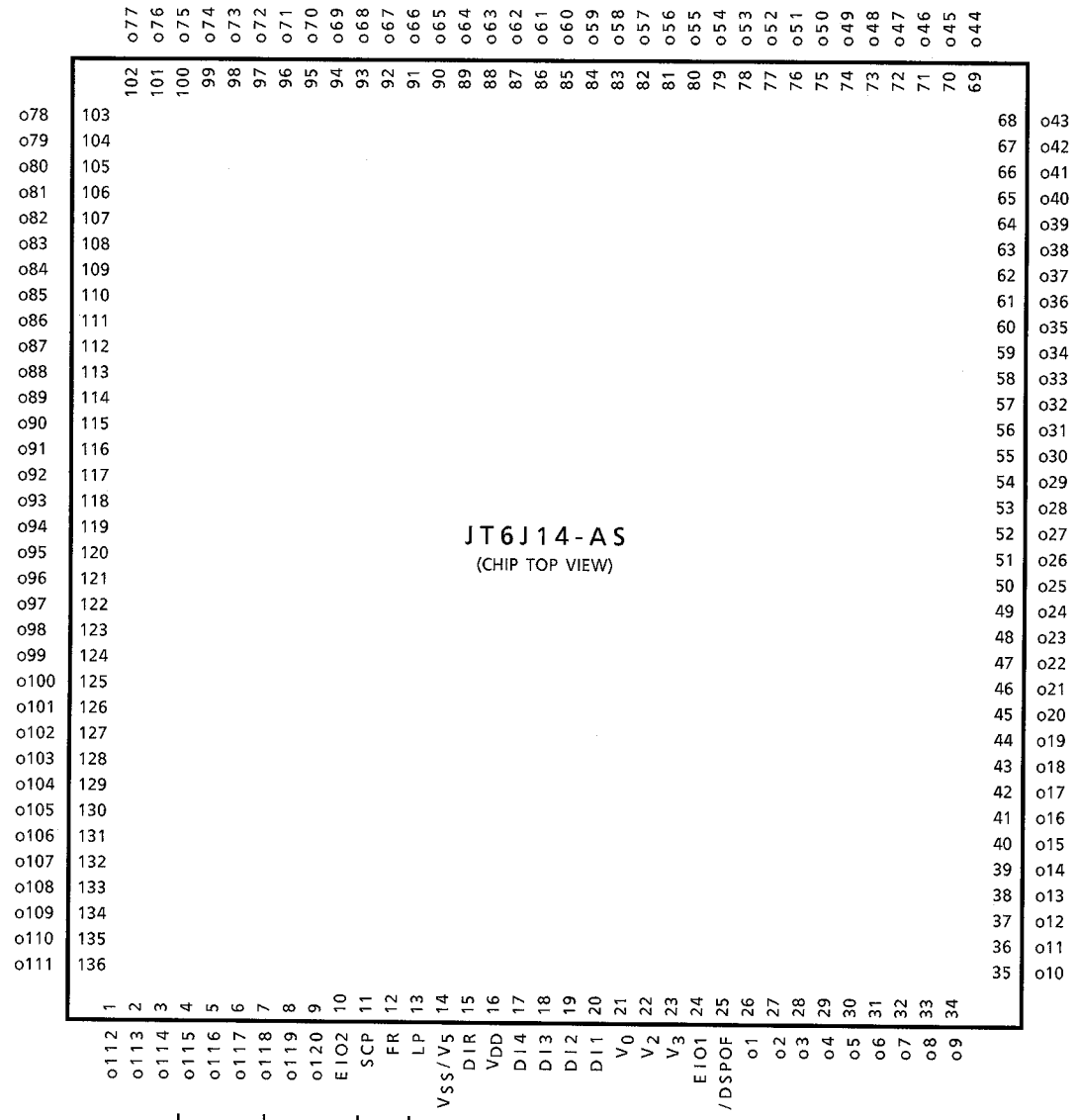
Features

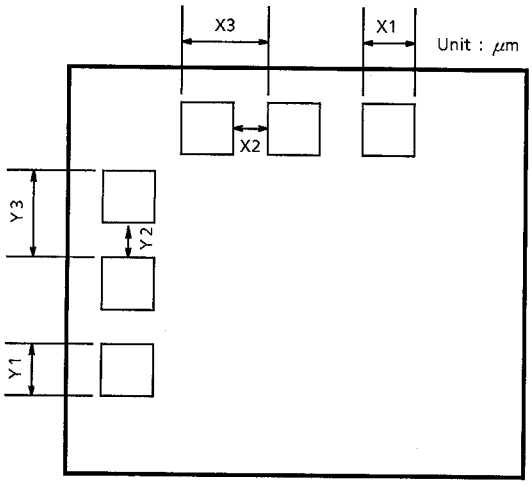
- Display duty application : to 1/160
- LCD drive signal : 120
- Data transfer : 4-bit bidirectional
- Maximum operating frequency: 10 MHz (V_{DD} = 4.5 V), 6.5 MHz (V_{DD} = 2.7 V)
- LCD drive Voltage : 11 to 28 V (max = 30 V)
- Power supply voltage : 2.7 to 5.5 V
- Operating temperature : −20 to 75°C
- LCD drive output resistance : 2.2 kΩ Max (V_0 = 12.8 V, 1/7 to 1/14 bias)
- Display−off function : When / DSPOF is L, all LCD drive outputs (o1 to o120) remain at the V_{SS}/V_5 level.
- Low Power Consumption : Cascade connections and auto enable transfer functions are available.

Block Diagram



Pin Assignment





	X1	X2	X3
Dimensions (μm)	100	30	130

	Y1	Y2	Y3
Dimensions (μm)	100	30	130

Pad Coordinates

Scribe width : 80 × 140 μm
Chip size : 5180 × 5240 μm (Including scribe width)
Number of PAD : 136 pcs
PAD size : 100 μm□
Palette edge coordinates 1: −2550, −2550
2: −2550, 2550
3: 2550, 2550
4: 2550, −2550
Chip edge coordinates 1: −2590, −2620
2: −2590, 2620
3: 2590, 2620
4: 2590, −2620

[Unit: μm]

No	Pad Name	X Point	Y Point
1	o112	−2145	−2334
2	o113	−2015	−2334
3	o114	−1885	−2334
4	o115	−1755	−2334
5	o116	−1625	−2334
6	o117	−1495	−2334
7	o118	−1365	−2334
8	o119	−1235	−2334
9	o120	−1105	−2334
10	EI02	−975	−2334
11	SCP	−845	−2334
12	FR	−715	−2334
13	LP	−585	−2334
14	V_{SS} / V5	−455	−2334
15	DIR	−325	−2334
16	V_{DD}	−195	−2334
17	DI4	−65	−2334
18	DI3	65	−2334
19	DI2	195	−2334
20	DI1	325	−2334
21	V0	455	−2334
22	V2	585	−2334
23	V3	715	−2334
24	EIO1	845	−2334
25	/ DSPOF	975	−2334
26	o1	1105	−2334
27	o2	1235	−2334
28	o3	1365	−2334
29	o4	1495	−2334
30	o5	1625	−2334
31	o6	1755	−2334
32	o7	1885	−2334
33	o8	2015	−2334

No	Pad Name	X Point	Y Point
34	o9	2145	−2334
35	o10	2334	−2145
36	o11	2334	−2015
37	o12	2334	−1885
38	o13	2334	−1755
39	o14	2334	−1625
40	o15	2334	−1495
41	o16	2334	−1365
42	o17	2334	−1235
43	o18	2334	−1105
44	o19	2334	−975
45	o20	2334	−845
46	o21	2334	−715
47	o22	2334	−585
48	o23	2334	−455
49	o24	2334	−325
50	o25	2334	−195
51	o26	2334	−65
52	o27	2334	65
53	o28	2334	195
54	o29	2334	325
55	o30	2334	455
56	o31	2334	585
57	o32	2334	715
58	o33	2334	845
59	o34	2334	975
60	o35	2334	1105
61	o36	2334	1235
62	o37	2334	1365
63	o38	2334	1495
64	o39	2334	1625
65	o40	2334	1755
66	o41	2334	1885

No	Pad Name	X Point	Y Point
67	o42	2334	2015
68	o43	2334	2145
69	o44	2145	2334
70	o45	2015	2334
71	o46	1885	2334
72	o47	1755	2334
73	o48	1625	2334
74	o49	1495	2334
75	o50	1365	2334
76	o51	1235	2334
77	o52	1105	2334
78	o53	975	2334
79	o54	845	2334
80	o55	715	2334
81	o56	585	2334
82	o57	455	2334
83	o58	325	2334
84	o59	195	2334
85	o60	65	2334
86	o61	−65	2334
87	o62	−195	2334
88	o63	−325	2334
89	o64	−455	2334
90	o65	−585	2334
91	o66	−715	2334
92	o67	−845	2334
93	o68	−975	2334
94	o69	−1105	2334
95	o70	−1235	2334
96	o71	−1365	2334
97	o72	−1495	2334
98	o73	−1625	2334
99	o74	−1755	2334
100	o75	−1885	2334
101	o76	−2015	2334

No	Pad Name	X Point	Y Point
102	o77	−2145	2334
103	o78	−2334	2145
104	o79	−2334	2015
105	o80	−2334	1885
106	o81	−2334	1755
107	o82	−2334	1625
108	o83	−2334	1495
109	o84	−2334	1365
110	o85	−2334	1235
111	o86	−2334	1105
112	o87	−2334	975
113	o88	−2334	845
114	o89	−2334	715
115	o90	−2334	585
116	o91	−2334	455
117	o92	−2334	325
118	o93	−2334	195
119	o94	−2334	65
120	o95	−2334	−65
121	o96	−2334	−195
122	o97	−2334	−325
123	o98	−2334	−455
124	o99	−2334	−585
125	o100	−2334	−715
126	o101	−2334	−845
127	o102	−2334	−975
128	o103	−2334	−1105
129	o104	−2334	−1235
130	o105	−2334	−1365
131	o106	−2334	−1495
132	o107	−2334	−1625
133	o108	−2334	−1755
134	o109	−2334	−1885
135	o110	−2334	−2015
136	o111	−2334	−2145

Pin Functions

Pin Name	I / O	Functions	Signal Voltage
o1 to o120	Output	Output for LCD drive signal	V_0 to V_{SS} / V_5
DI1 to DI4	Input	Input for shift data	V_{DD} to V_{SS} / V_5
SCP	Input	(Shift Clock Pulse) Input of shift clock pulse It is latched in the shift data synchronously with the falling edge of SCP.	
FR	Input	(Frame) Input for frame signal	
LP	Input	(Latch Pulse) Input for shift clock pulse The display data is latched on the falling edge of LP. When EIO1 (input) = L, setting $\overline{SCP}$ ·LP = H enables the 1st LSI.	
DIR	Input	(Direction) Input for data flow direction select	
EIO1, EIO2	I / O	Input / Output for enable signal DIR selects Input or Output. Connect EIO1 (input) of 1st LSI to L. For a cascade connection, connect EIO2 (output) to EIO1 (input) of next LSI.	
/ DSPOF	Input	(Display Off) /DSPOF = L : Display−off mode, (o1 to o120) remain at the V_{SS} / V_5 level. The latch output becomes non−illuminated data (V_2 / V_3 level) after display−off mode release. /DSPOF = H : Display−on mode, (o1 to o120) are operational.	
V_{DD}	—	Power supply for internal logic	—
V_{SS} / V_5	—	Power supply for internal logic	
V_0, V_2, V_3	—	Power supply for LCD drive circuit	

Relationship between FR, Data Input and Output Levels

FR	Data Input (D11 to D12)	/ DSPOF	Output Level
L	L	H	V_2
L	H	H	V_0
H	L	H	V_3
H	H	H	V_{SS} / V_5
X	X	L	V_{SS} / V_5

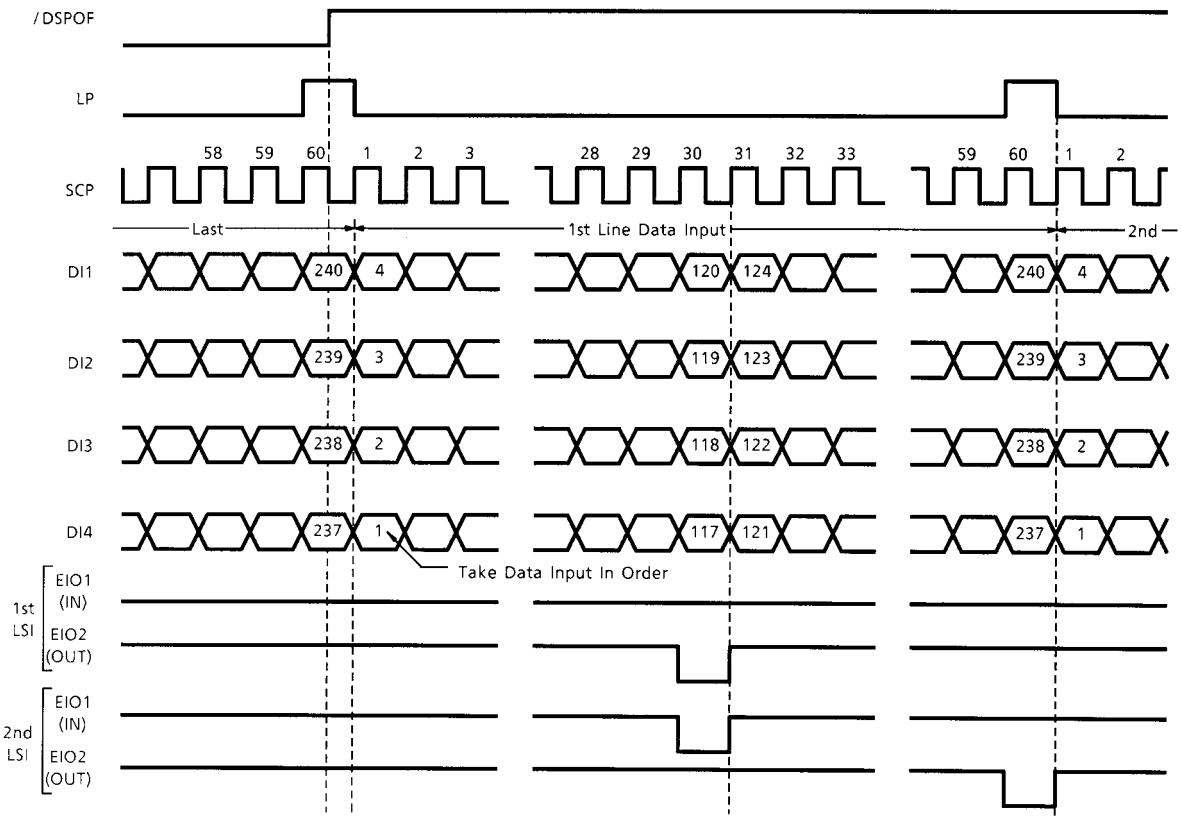
X: Don't care

Data Input Format

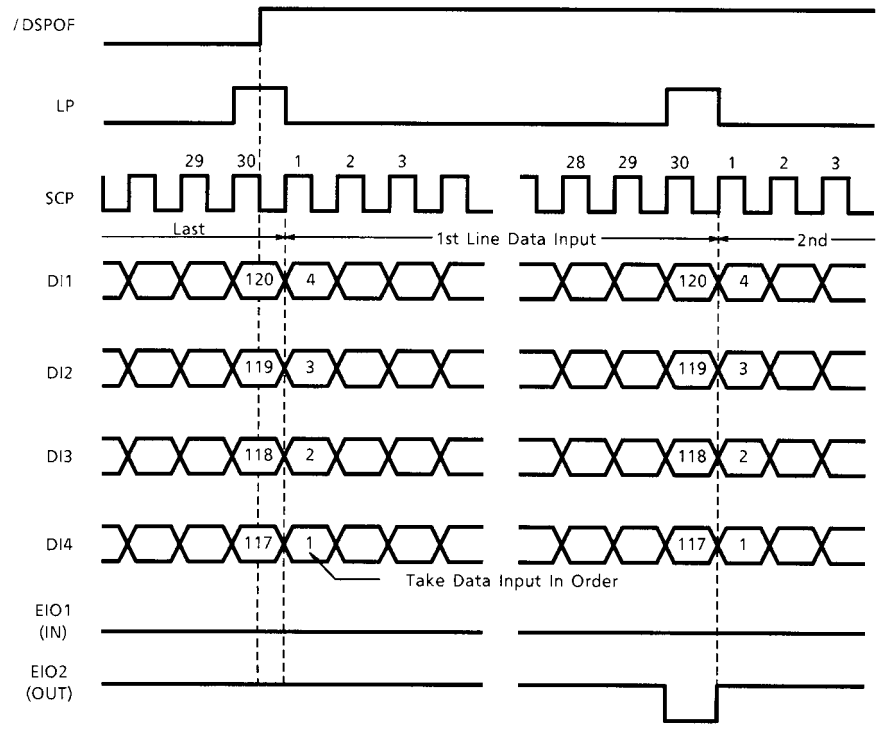
Direction	Enable Input			Data Format			
DIR	EIO1	EIO2		DI1	DI2	DI3	DI4
H	Input	Output	Last data	o120	o119	o118	o117
			First data	o4	o3	o2	o1
L	Output	Input	Last data	o1	o2	o3	o4
			First data	o117	o118	o119	o120

Timing Diagram

- **Use of JT6J14A−AS 2 pcs (DIR = "H")**



- **Use of JT6J14A−AS 1 pc (DIR = "H")**



Absolute Maximum Ratings
(Ensure that the following conditions are maintained, $V_0 \geq V_2 \geq V_3 \geq V_{SS} / V_5$)

Item	Symbol	Pin Name	Rating	Unit
Power Supply Voltage (1)	V_{DD}	V_{DD}	−0.3 to 6.0	V
Power Supply Voltage (2)	V_0	V_0	−0.3 to 30.0	V
Power Supply Voltage (3)	V_2, V_3	V_2, V_3	−0.3 to V_0	V
Input Voltage	V_{IN}	(Note 1)	−0.3 to V_{DD}	V
Operating Temperature	T_{opr}	—	−20 to 75	°C
Storage Temperature	T_{stg}	—	−40 to 125	°C

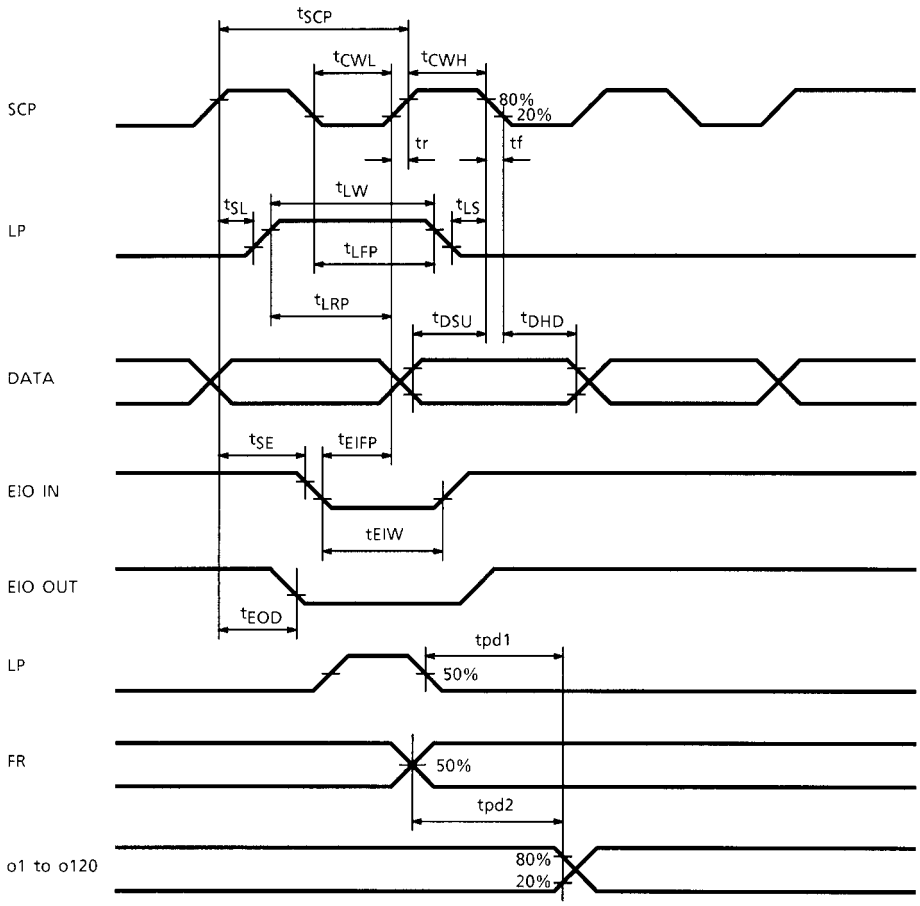
Note 1: SCP, FR, LP, DIR, EIO1, EIO2, DI1 to DI4, / DSPOF

Electrical Characteristics
DC Characteristics
(Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, V_0 = 11 to 28 V, Ta = −20 to 75°C)

Item		Symbol	Test Circuit	Test Condition			Min	Typ.	Max	Unit	Pin Name
Supply Voltage (1)		V_{DD}	—	—			2.7	5.0	5.5	V	V_{DD}
Supply Voltage (2)		V_0	—	—			11	—	28		V_0
Input Voltage	"H" Level	V_{IH}	—	—			0.8 V_{DD}	—	V_{DD}		SCP, FR, LP, DIR, EIO1, EIO2, DI1 to DI4, / DSPOF
	"L" Level	V_{IL}	—	—			0	—	0.2 V_{DD}		
Output Voltage	"H" Level	V_{OH}	—	I_{OH} = −0.5 mA			V_{DD} − 0.5	—	V_{DD}		EIO1, EIO2
	"L" Level	V_{OL}	—	I_{OL} = 0.5 mA			0	—	0.5		
Output Resistance	"H" Level	R_{OH}	—	V_{OUT} = V_0 − 0.5 V (Note 2)			—	1.2	2.2	kΩ	o1 to o120
	"M" Level	R_{OM}	—	V_{OUT} = V_2 ± 0.5 V (Note 2)			—	1.2	2.2		
		R_{OM}	—	V_{OUT} = V_3 ± 0.5 V (Note 2)			—	1.2	2.2		
	"L" Level	R_{OL}	—	V_{OUT} = V_{SS} / V_5 + 0.5 V (Note 2)			—	1.2	2.2		
Input Current		IIL1	—	V_{IN} = 0 to V_{DD}			−1.0	—	1.0	μA	SCP, FR, LP, DIR, EIO1, EIO2, DI1 to DI4, / DSPOF
Current Consumption		I_{DD} OPE	—	V_{DD} = 5.5 V	V_0 = 28 V	During operations (Note 4)	—	250	500	μA	V_{DD}
			—	V_{DD} = 3.3 V			—	150	300		
		I_{DD} ST / BY	—	V_{DD} = 5.5 V		During operations (Note 5)	—	75	100		
			—	V_{DD} = 3.3 V			—	40	60		
		I_{DD} LEAK	—	V_{DD} = 5.5 V		When no operation	—	—	1.0		
		IO OPE	—	V_{DD} = 5.5 V		During operations (Note 3)	—	110	150		V_0
		IO LEAK	—	V_{DD} = 5.5 V		When no operation	—	—	1.0		

Note 2: V_0 = 12.8 V, 1 / 7 to 1 / 14 bias
Note 3: fSCP = 672 kHz, f_{FP} = 70 Hz, f_{FR} = 35 Hz, f_{LP} = 11.2 kHz,
input data: every bit inverted, no load
Note 4: fSCP = 672 kHz, f_{FP} = 70 Hz, f_{FR} = 35 Hz, f_{LP} = 11.2 kHz,
input data: every bit inverted, Internal data receiver operating, no load
Note 5: fSCP = 672 kHz, f_{FP} = 70 Hz, f_{FR} = 35 Hz, f_{LP} = 11.2 kHz,
input data: every bit inverted, Internal data receiver sleeping, no load
f_{FP}: screen switching frequency

AC Characteristics



Test Conditions 1: $t_{SCP} = t_{CWH} + t_{CWL} + tr + tf$
(Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, V_0 = 11 to 28 V, Ta = −20 to 75°C)

Item	Symbol	Test Condition	Min	Max	Unit
SCP Cycle	t_{SCP}	—	100	—	ns
SCP Pulse Width	t_{CWH}	—	40	—	ns
SCP Pulse Width	t_{CWL}	—	40	—	
Data Set−up Time	t_{DSU}	—	15	—	
Data Hold Time	t_{DHD}	—	5	—	
SCP Rising / Falling Time	t_r, t_f	—	—	50	
LP Set−up Time	t_{LRP}	—	5	—	
LP Hold Time	t_{LFP}	—	15	—	
LP Pulse Width	t_{LW}	—	15	—	
SCP−Rise to LP−Rise Time	t_{SL}	—	10	—	
LP−Fall to SCP−Fall Time	t_{LS}	—	17	—	
EIO IN Set−up Time	t_{EIFP}	—	20	—	
EIO IN Hold Time	t_{EIW}	—	15	—	
SCP−Rise to EIO−Rise Time	t_{SE}	—	5	—	
EIO OUT Delay Time	t_{EOD}	(Note 6)	—	55	
Output Delay Time (LP → OUT)	t_{pd1}	—	—	400	
Output Delay Time (FR → OUT)	t_{pd2}	—	—	400	

Note 6: C_L = 10 pF

Test Conditions 2: $t_{SCP} = t_{CWH} + t_{CWL} + tr + tf$
(Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, V_0 = 11 to 28 V, Ta = −20 to 75°C)

Item	Symbol	Test Condition	Min	Max	Unit
SCP Cycle	t_{SCP}	—	154	—	ns
SCP Pulse Width	t_{CWH}	—	50	—	ns
SCP Pulse Width	t_{CWL}	—	50	—	
Data Set−up Time	t_{DSU}	—	30	—	
Data Hold Time	t_{DHD}	—	10	—	
SCP Rise / Fall Time	t_r, t_f	—	—	50	
LP Set−up Time	t_{LRP}	—	30	—	
LP Hold Time	t_{LFP}	—	30	—	
LP Pulse Width	t_{LW}	—	30	—	
SCP−Rise to LP−Rise Time	t_{SL}	—	20	—	
LP−Fall to SCP−Fall Time	t_{LS}	—	40	—	
EIO IN Set−up Time	t_{EIFP}	—	40	—	
EIO IN Hold Time	t_{EIW}	—	30	—	
SCP−Rise to EIO−Rise Time	t_{SE}	—	5	—	
EIO OUT Delay Time	t_{EOD}	(Note 7)	—	80	
Output Delay Time (LP → OUT)	t_{pd1}	—	—	500	
Output Delay Time (FR → OUT)	t_{pd2}	—	—	500	

Note 7: C_L = 10 pF

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