TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

JBT6L78–AS

Gate Driver for TFT LCD Panel

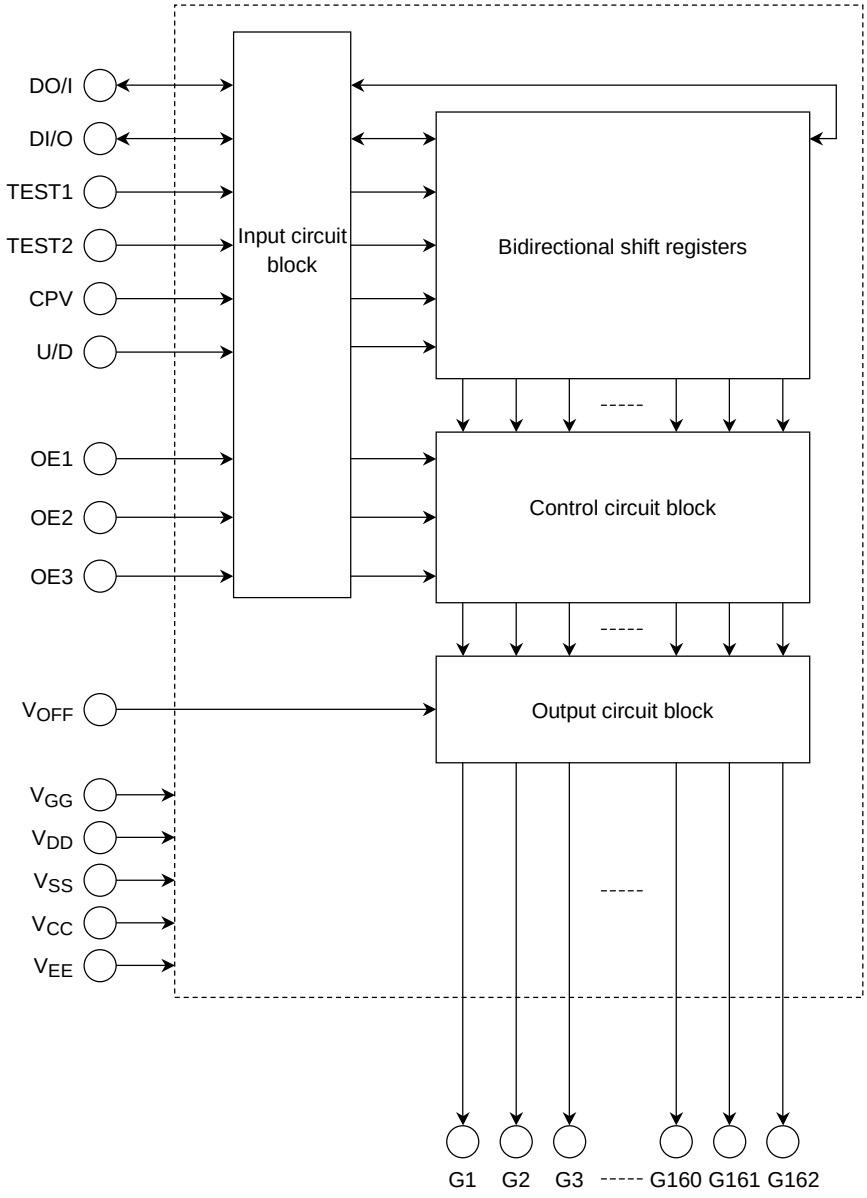
The JBT6L78-AS is a 162-channel output gate driver for TFT LCD panels. This device accepts external input of the panel drive voltage, allowing you to change the low-level output voltage. Thus, the can be used for various TFT LCD panel drive systems.

The JBT6L78-AS offers high integration circuit due to CMOS technology.

Features

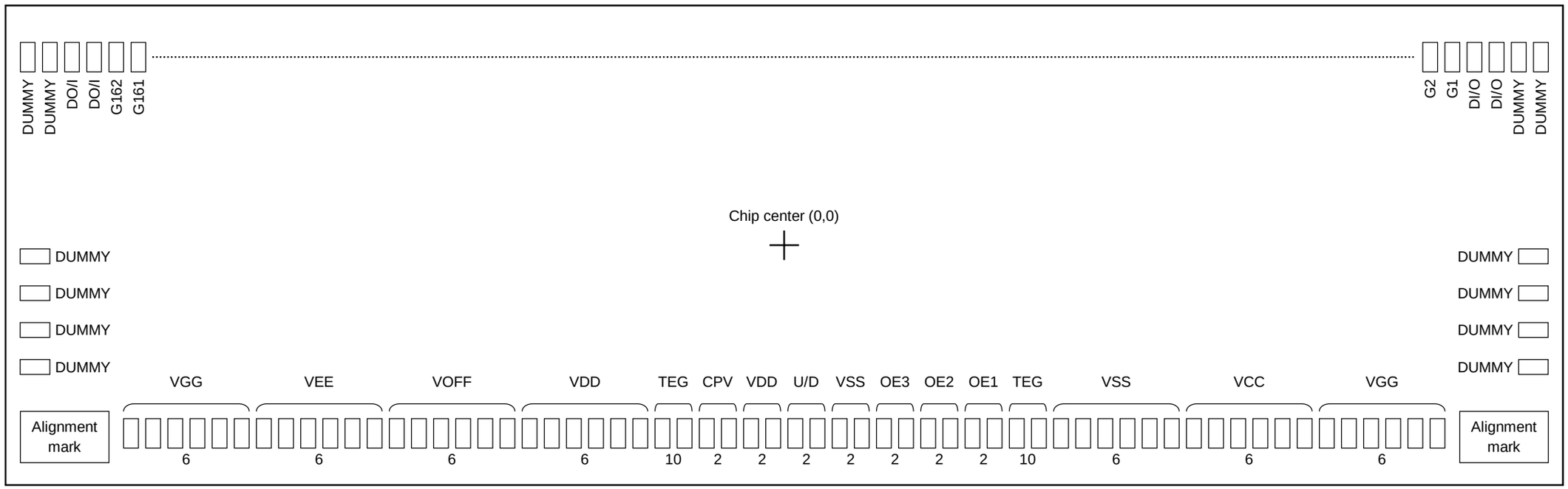
- LCD drive output pins : 162 pins
- LCD drive output voltage : V_{EE} + 36 V (max)
- Data transfer method : Bidirectional shift registers
- Operating temperature : −20 to 75°C

Block Diagram

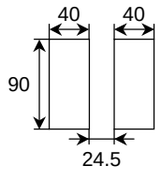


PAD Layout

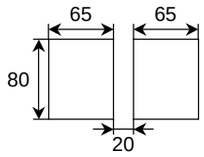
Chip size: 1.09 × 11.51 (mm)



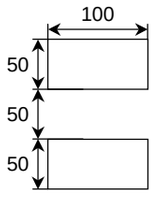
◆ Long-side Output PAD



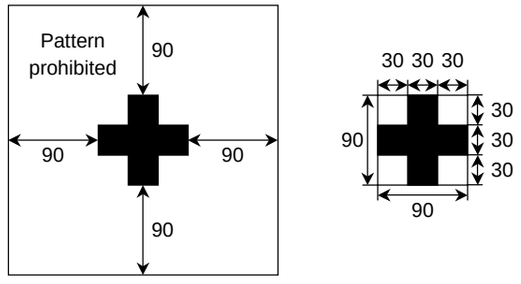
◆ Long-side Input PAD



◆ Short-side PAD



◆ Alignment mark



【Unit: μm】

PAD Coordinates

Chip size: 11.51 × 1.09 (mm)
Number of PAD: 254

[Unit: μm]

No.	Name	X Point	Y Point
1	V_{GG}	−5328	−420
2	V_{GG}	−5243	−420
3	V_{GG}	−5158	−420
4	V_{GG}	−5073	−420
5	V_{GG}	−4988	−420
6	V_{GG}	−4903	−420
7	V_{EE}	−4618	−420
8	V_{EE}	−4533	−420
9	V_{EE}	−4448	−420
10	V_{EE}	−4363	−420
11	V_{EE}	−4278	−420
12	V_{EE}	−4193	−420
13	V_{OFF}	−3908	−420
14	V_{OFF}	−3823	−420
15	V_{OFF}	−3738	−420
16	V_{OFF}	−3653	−420
17	V_{OFF}	−3568	−420
18	V_{OFF}	−3483	−420
19	V_{DD}	−3198	−420
20	V_{DD}	−3113	−420
21	V_{DD}	−3028	−420
22	V_{DD}	−2943	−420
23	V_{DD}	−2858	−420
24	V_{DD}	−2773	−420
25	TEG	−2488	−420
26	TEG	−2348	−420
27	TEG	−2208	−420
28	TEG	−2068	−420
29	TEG	−1928	−420
30	TEG	−1788	−420
31	TEG	−1648	−420
32	TEG	−1508	−420
33	TEG	−1368	−420
34	TEG	−1228	−420
35	CPV	−943	−420
36	CPV	−858	−420
37	V_{DD}	−573	−420
38	V_{DD}	−488	−420
39	U/D	−203	−420
40	U/D	−118	−420
41	V_{SS}	167	−420
42	V_{SS}	252	−420
43	OE3	537	−420
44	OE3	622	−420
45	OE2	907	−420
46	OE2	992	−420
47	OE1	1277	−420
48	OE1	1362	−420
49	TEST1	1647	−420
50	TEST2	1932	−420
51	TEG	2217	−420
52	TEG	2357	−420
53	TEG	2497	−420
54	TEG	2637	−420
55	TEG	2777	−420
56	TEG	2917	−420
57	TEG	3057	−420
58	TEG	3197	−420
59	V_{SS}	3482	−420
60	V_{SS}	3567	−420
61	V_{SS}	3652	−420
62	V_{SS}	3737	−420
63	V_{SS}	3822	−420
64	V_{SS}	3907	−420
65	V_{CC}	4192	−420
66	V_{CC}	4277	−420
67	V_{CC}	4362	−420
68	V_{CC}	4447	−420
69	V_{CC}	4532	−420
70	V_{CC}	4617	−420
71	V_{GG}	4902	−420
72	V_{GG}	4987	−420
73	V_{GG}	5072	−420
74	V_{GG}	5157	−420
75	V_{GG}	5242	−420
76	V_{GG}	5327	−420
77	DUMMY	5620	−147
78	DUMMY	5620	−47
79	DUMMY	5620	53
80	DUMMY	5620	153
81	DUMMY	5450.5	415
82	DUMMY	5386	415
83	DI/O	5321.5	415
84	DI/O	5257	415
85	G1	5192.5	415
86	G2	5128	415
87	G3	5063.5	415
88	G4	4999	415
89	G5	4934.5	415
90	G6	4870	415
91	G7	4805.5	415
92	G8	4741	415
93	G9	4676.5	415
94	G10	4612	415
95	G11	4547.5	415
96	G12	4483	415
97	G13	4418.5	415
98	G14	4354	415
99	G15	4289.5	415
100	G16	4225	415
101	G17	4160.5	415
102	G18	4096	415
103	G19	4031.5	415
104	G20	3967	415
105	G21	3902.5	415
106	G22	3838	415
107	G23	3773.5	415
108	G24	3709	415
109	G25	3644.5	415
110	G26	3580	415
111	G27	3515.5	415
112	G28	3451	415
113	G29	3386.5	415
114	G30	3322	415

[Unit: μm]

No.	Name	X Point	Y Point
115	G31	3257.5	415
116	G32	3193	415
117	G33	3128.5	415
118	G34	3064	415
119	G35	2999.5	415
120	G36	2935	415
121	G37	2870.5	415
122	G38	2806	415
123	G39	2741.5	415
124	G40	2677	415
125	G41	2612.5	415
126	G42	2548	415
127	G43	2483.5	415
128	G44	2419	415
129	G45	2354.5	415
130	G46	2290	415
131	G47	2225.5	415
132	G48	2161	415
133	G49	2096.5	415
134	G50	2032	415
135	G51	1967.5	415
136	G52	1903	415
137	G53	1838.5	415
138	G54	1774	415
139	G55	1709.5	415
140	G56	1645	415
141	G57	1580.5	415
142	G58	1516	415
143	G59	1451.5	415
144	G60	1387	415
145	G61	1322.5	415
146	G62	1258	415
147	G63	1193.5	415
148	G64	1129	415
149	G65	1064.5	415
150	G66	1000	415
151	G67	935.5	415
152	G68	871	415
153	G69	806.5	415
154	G70	742	415
155	G71	677.5	415

No.	Name	X Point	Y Point
156	G72	613	415
157	G73	548.5	415
158	G74	484	415
159	G75	419.5	415
160	G76	355	415
161	G77	290.5	415
162	G78	226	415
163	G79	161.5	415
164	G80	97	415
165	G81	32.5	415
166	G82	−32	415
167	G83	−96.5	415
168	G84	−161	415
169	G85	−225.5	415
170	G86	−290	415
171	G87	−354.5	415
172	G88	−419	415
173	G89	−483.5	415
174	G90	−548	415
175	G91	−612.5	415
176	G92	−677	415
177	G93	−741.5	415
178	G94	−806	415
179	G95	−870.5	415
180	G96	−935	415
181	G97	−999.5	415
182	G98	−1064	415
183	G99	−1128.5	415
184	G100	−1193	415
185	G101	−1257.5	415
186	G102	−1322	415
187	G103	−1386.5	415
188	G104	−1451	415
189	G105	−1515.5	415
190	G106	−1580	415
191	G107	−1644.5	415
192	G108	−1709	415
193	G109	−1773.5	415
194	G110	−1838	415
195	G111	−1902.5	415
196	G112	−1967	415

No.	Name	X Point	Y Point
197	G113	−2031.5	415
198	G114	−2096	415
199	G115	−2160.5	415
200	G116	−2225	415
201	G117	−2289.5	415
202	G118	−2354	415
203	G119	−2418.5	415
204	G120	−2483	415
205	G121	−2547.5	415
206	G122	−2612	415
207	G123	−2676.5	415
208	G124	−2741	415
209	G125	−2805.5	415
210	G126	−2870	415
211	G127	−2934.5	415
212	G128	−2999	415
213	G129	−3063.5	415
214	G130	−3128	415
215	G131	−3192.5	415
216	G132	−3257	415
217	G133	−3321.5	415
218	G134	−3386	415
219	G135	−3450.5	415
220	G136	−3515	415
221	G137	−3579.5	415
222	G138	−3644	415
223	G139	−3708.5	415
224	G140	−3773	415
225	G141	−3837.5	415
226	G142	−3902	415
227	G143	−3966.5	415
228	G144	−4031	415
229	G145	−4095.5	415
230	G146	−4160	415
231	G147	−4224.5	415
232	G148	−4289	415
233	G149	−4353.5	415
234	G150	−4418	415
235	G151	−4482.5	415
236	G152	−4547	415
237	G153	−4611.5	415

[Unit: μm]

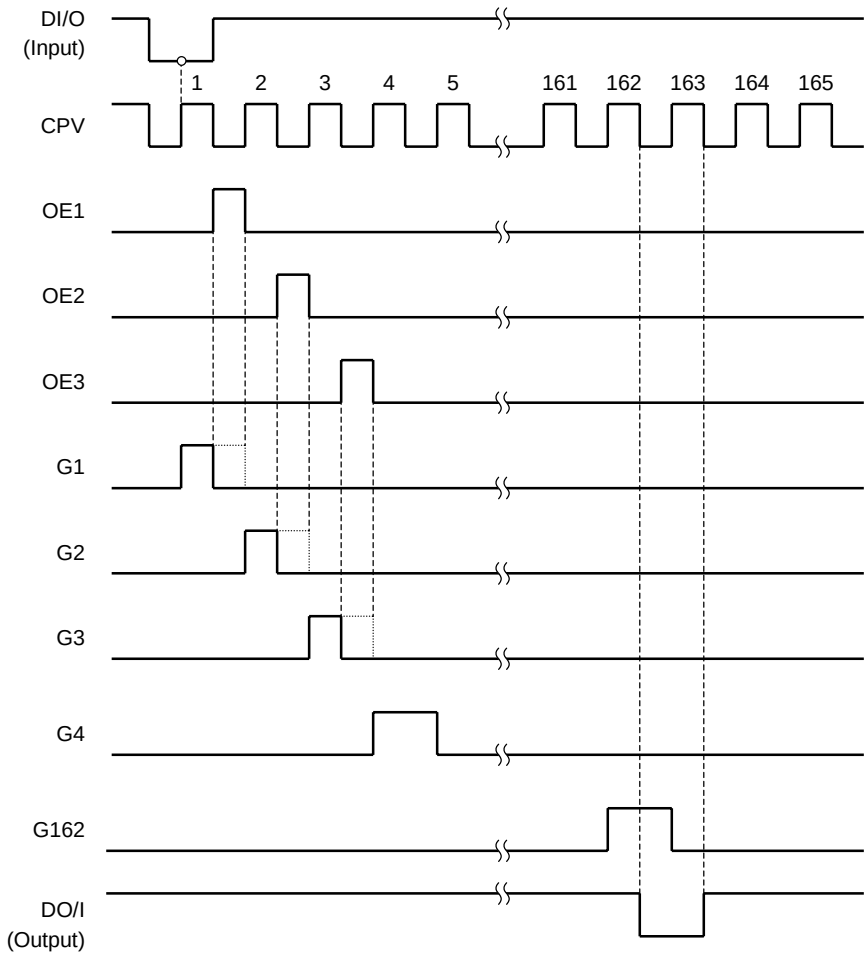
No.	Name	X Point	Y Point
238	G154	−4676	415
239	G155	−4740.5	415
240	G156	−4805	415
241	G157	−4869.5	415
242	G158	−4934	415
243	G159	−4998.5	415
244	G160	−5063	415
245	G161	−5127.5	415
246	G162	−5192	415
247	DO/I	−5256.5	415
248	DO/I	−5321	415
249	DUMMY	−5385.5	415
250	DUMMY	−5450	415
251	DUMMY	−5620	153
252	DUMMY	−5620	53
253	DUMMY	−5620	−47
254	DUMMY	−5620	−147
—	Alignment mark	5543	−333
—	Alignment mark	−5543	−333

Pin Description

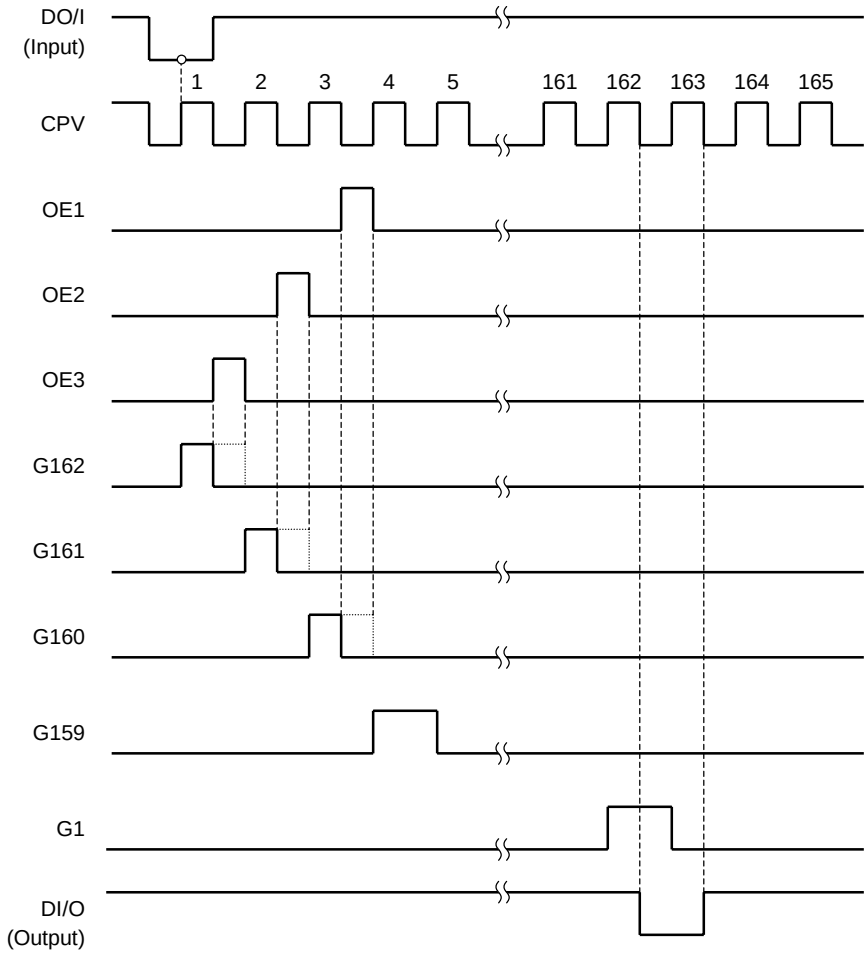
<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>DI/O
DO/I</td><td>I/O</td><td>Vertical shift data input/output pins
Input/output shift data. The pin function is switched between input and output by the U/D pin as follows:
<table>
<tr><th>U/D</th><th>DI/O</th><th>DO/I</th></tr>
<tr><td>H</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
</table>
At input
Data are latched into the shift registers in sync with the rising edge of CPV.
At output:
If the JBT6L78-AS is cascade-connected, data to be input at the next stage are output from the pin. The data state changes in sync with the falling edge of CPV.</td></tr>
<tr><td>U/D</td><td>I</td><td>Data transfer direction switching pin
Specifies the shift direction of the shift registers.
Data in the shift registers shift in sync with the rising edge of CPV as follows:
• U/D = H: G1 → G2→ G3 → ⋯ → G162
• U/D = L: G162 → G161→ G160 → ⋯ → G1
Use the pin at DC level. For High, V_{DD}; for Low, V_{SS}.
Note that if U/D mode is switched during data transfer, misoperation occurs to a display page.</td></tr>
<tr><td>CPV</td><td>I</td><td>Vertical shift clock
Shift clock for the shift registers. Data are shifted in sync with the rising edge of CPV.</td></tr>
<tr><td>OE1 to OE3</td><td>I</td><td>Output enable pin
These pins control output data from the output pins (G1 to G162).
• OE = L: Normal output state (1-pulse scanning)
• OE = H: Outputs V_{OFF} voltage.
Note that the contents of the shift registers are not cleared. Those operations are performed asynchronously to CPV.</td></tr>
<tr><td>G1 to G162</td><td>O</td><td>LCD panel drive pins.</td></tr>
<tr><td>TEST1, TEST2,
TEG</td><td>I</td><td>Test pin.
Leave the pin open.</td></tr>
<tr><td>V_{GG}</td><td></td><td>Power supply pin for controlling LCD.</td></tr>
<tr><td>V_{OFF}</td><td></td><td>LCD off level input pin</td></tr>
<tr><td>V_{DD}</td><td></td><td>Power supply pin for internal logic</td></tr>
<tr><td>V_{SS}</td><td></td><td>Power supply pin for cascade output</td></tr>
<tr><td>V_{CC}</td><td></td><td>Power supply pin for LCD control and internal logic</td></tr>
<tr><td>V_{EE}</td><td></td><td>Power supply pin for controlling LCD</td></tr>
</table>

Timing Chart

UP mode (U/D = High level)



DOWN mode (U/D = Low level)



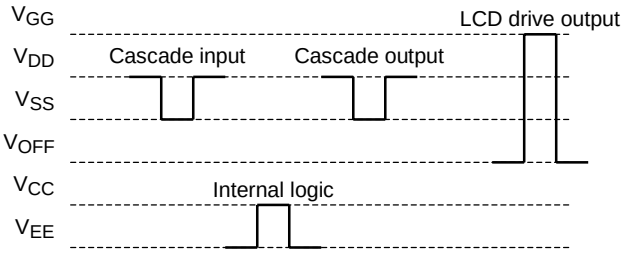
Maximum Ratings (V_{SS} = 0 V)

Characteristics	Symbol	Rating	Unit
Supply voltage (1)	$V_{GG} - V_{EE}$	−0.3 to 45.0	V
Supply voltage (2)	V_{EE}	−20 to 0.3	V
Supply voltage (3)	V_{DD}	−0.3 to 6.5	V
Supply voltage (4)	$V_{CC} - V_{EE}$	−0.3 to 6.5	V
Input voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V
LCD off level input voltage	V_{OFF}	V_{EE} − 0.3 to V_{GG} + 0.3	V
Storage temperature	T_{stg}	−55 to 125	°C

Operating Range (V_{SS} = 0 V)

Characteristics	Symbol	Rating	Unit
Supply voltage (1)	$V_{GG} - V_{EE}$	20 to 36	V
Supply voltage (2)	V_{EE}	−18 to −5	V
Supply voltage (3)	V_{DD}	2.5 to 3.6	V
Supply voltage (4)	$V_{CC} - V_{EE}$	3.0 to 5.5	V
Input voltage	V_{IN}	0 to V_{DD}	V
LCD OFF level input voltage	V_{OFF}	V_{EE} to V_{EE} + 8	V
Operating temperature	T_{opr}	−20 to 75	°C
Operating frequency	f_{CPV}	DC to 50	kHz
Output load capacitance	C_L	100 (max)	pF

Relations between power supplies



Electrical Characteristics

DC Characteristics (V_{DD} = 2.5 to 3.6 V, $V_{GG} - V_{EE}$ = 20 to 33 V, $V_{OFF} = V_{EE}$ to V_{EE} + 5 V, $V_{CC} = V_{EE}$ + 5 V, V_{SS} = 0 V, Ta = –20 to 75°C)

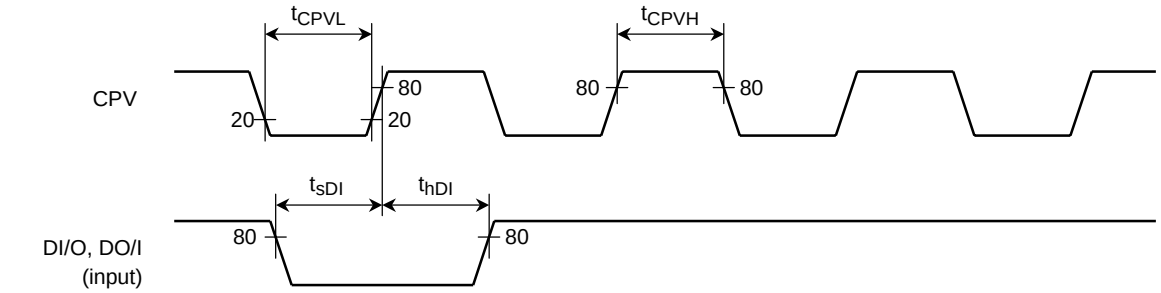
Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Relevant Pin
Input voltage	Low level	V_{IL}	—	—	0	—	$V_{DD} \times 0.2$	V	(Note 1)
	High level	V_{IH}	—	—	$V_{DD} \times 0.8$	—	V_{DD}		
Output voltage	Low level	V_{OL}	—	I_{OL} = 100 μA	—	—	0.4	V	DI/O, DO/I
	High level	V_{OH}	—	I_{OH} = –100 μA	$V_{DD} - 0.4$	—	—		
Input leakage current		I_{IN}	—	—	—	—	1.0	μA	
Output resistance		R_{OL}	—	V_{OFF} level output	—	—	1.0	kΩ	G1 to G162
		R_{OH}	—	V_{GG} level output					
Current dissipation (1)		I_{GG}	—	(Note 2)	—	—	50	μA	
Current dissipation (2)		I_{DD}	—		—	—	500	μA	
Current dissipation (3)		I_{CC}	—		—	—	80	μA	
Current dissipation (4)		I_{OFF}	—		—	—	40	μA	
Current dissipation (5)		I_{EE}	—		–400	—	—	μA	

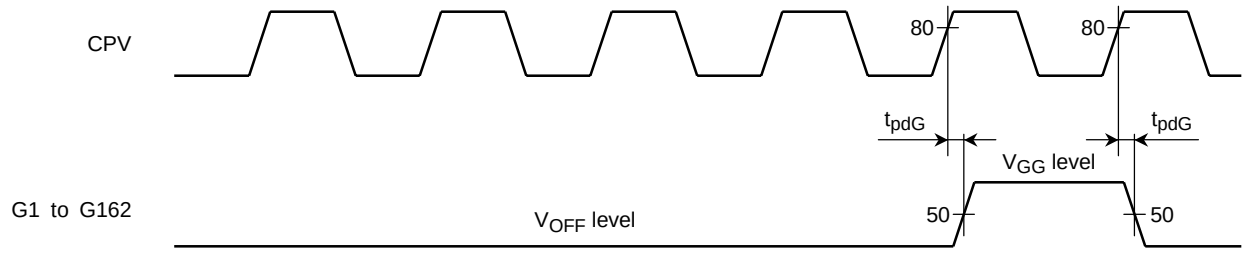
Note 1: DI/O, DO/I, CPV, OE1 to OE3

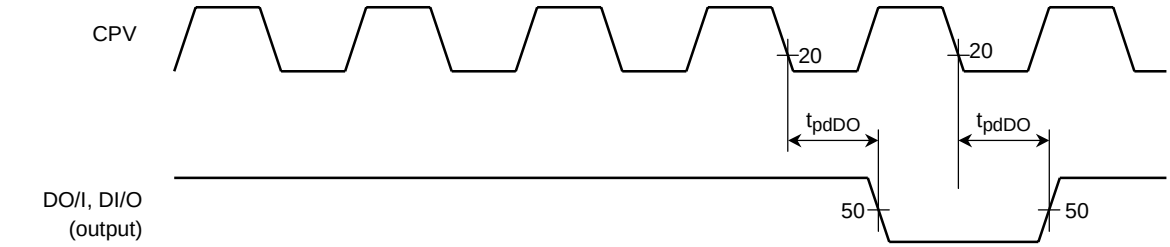
Note 2: No load, CPV = 21 kHz, DI/O input cycle = 60 Hz, V_{DD} = 3.6 V, V_{EE} = –15 V, CPV High width = 23.8 μs, 1-clock cycle DI/O input, OE1 to OE3 = Low, U/D = High

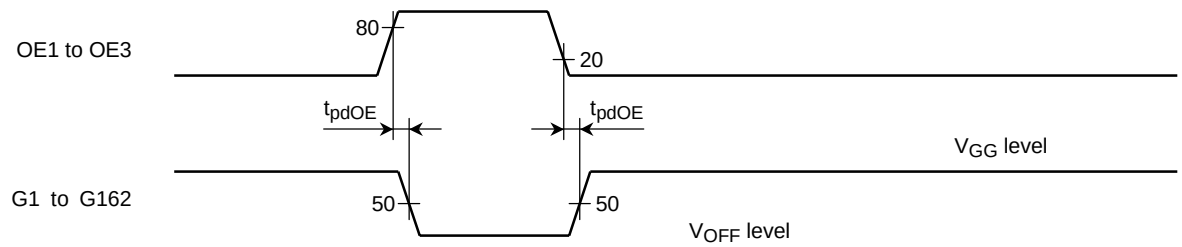
AC Characteristics (V_{DD} = 2.5 to 3.6 V, $V_{GG} - V_{EE}$ = 20 to 33 V, $V_{OFF} = V_{EE}$ to V_{EE} + 5 V, $V_{CC} = V_{EE}$ + 5 V, V_{SS} = 0 V, Ta = –20 to 75°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Max	Unit
Clock pulse width (H)	t_{CPVH}	—	—	10	—	μs
Clock pulse width (L)	t_{CPVL}	—	—	10	—	μs
Data setup time	t_{sDI}	—	—	1	—	μs
Data hold time	t_{hDI}	—	—	1	—	μs
Output delay time (1)	t_{pdDO}	—	C_L = 20 pF	—	1	μs
Output delay time (2)	t_{pdG}	—	C_L = 100 pF	—	2	μs
Output delay time (3)	t_{pdOE}	—	C_L = 100 pF	—	2	μs


tCPVL
tCPVH
CPV
80
20
80
20
80
80
tsDI
thDI
DI/O, DO/I
(input)
80
80

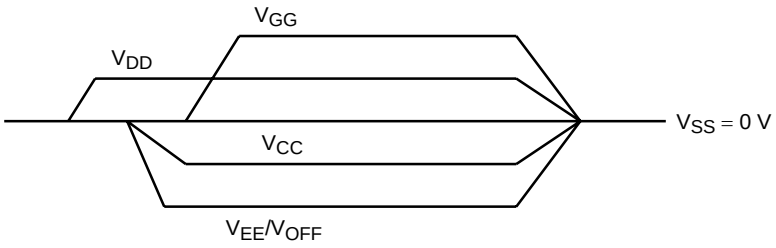

CPV
80
80
tpdG
tpdG
VGG level
G1 to G162
VOFF level
50
50


CPV
20
20
tpdDO
tpdDO
DO/I, DI/O
(output)
50
50


OE1 to OE3
80
20
tpdOE
tpdOE
VGG level
G1 to G162
50
50
VOFF level

Power Supply Sequence

At power on, supply power in order of V_{DD} → logic signal → V_{CC}, V_{EE}, V_{OFF} → V_{GG}. At power off, turn off in order of V_{GG} → V_{CC}, V_{EE}, V_{OFF} → logic signal → V_{DD}.



RESTRICTIONS ON PRODUCT USE

000707EBM

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the “Handling Guide for Semiconductor Devices,” or “TOSHIBA Semiconductor Reliability Handbook” etc..
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury (“Unintended Usage”). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer’s own risk.
- Light striking a semiconductor device generates electromotive force due to photoelectric effects. In some cases this can cause the device to malfunction.
  This is especially true for devices in which the surface (back), or side of the chip is exposed. When designing circuits, make sure that devices are protected against incident light from external sources. Exposure to light both during regular operation and during inspection must be taken into account.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
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