TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

JBT6K49-AS

Power supply IC for TFT LCD Panels

The JBT6K49-AS chip is an integrated circuit (IC) for generating the supply voltages necessary for a TFT LCD panel driver. When used in combination with the T6K47 source driver and the T6K48 gate driver for TFT LCD panels, the JBT6K49-AS enables the module set to operate with low power consumption.

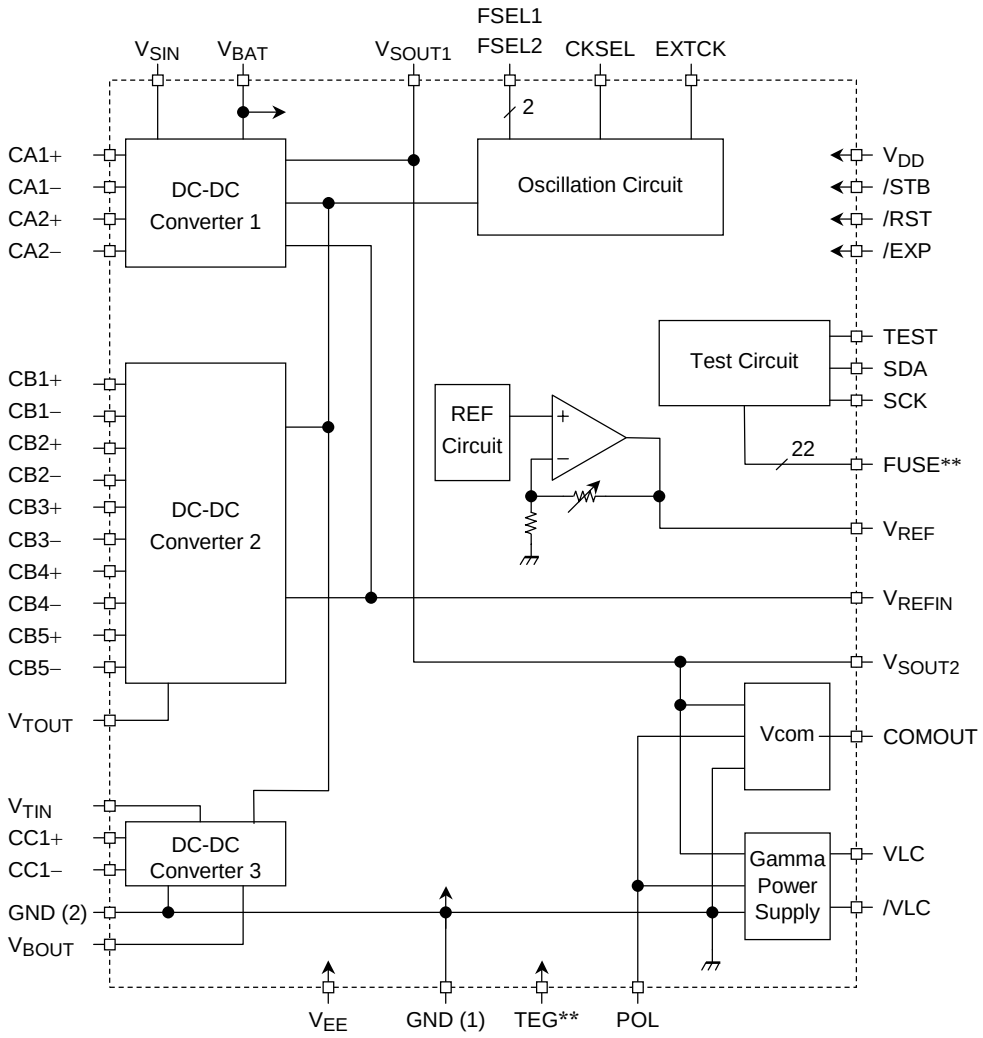
A high-speed CMOS process is employed to achieve low power consumption and high-speed operation for the JBT6K49-AS.

Features

- Built-in circuits : DC-DC converters and oscillation circuit for DC-DC converters
  High-precision regulator
  Binary buffer for γ-correction
  Level shifter circuit for V_{com}
- Supply voltage (V_{DD}) : 2.7 V to 3.3 V
- Supply voltage (V_{BAT}) : 2.7 V to 4.2 V
- Low power consumption
- Operating temperature : −20°C to 75°C
- CMOS process
- Recommended drivers : T6K47 source driver for TFT LCD
  T6K48 gate driver for TFT LCD
- Package :

Product Name	Description
JBT6K49-AS (PI)	Gold bump chip

Block Diagram



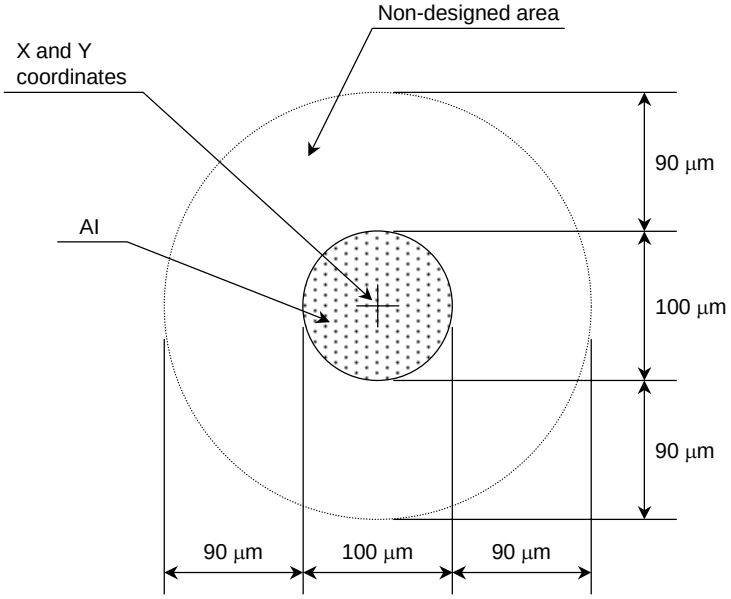
PAD Specifications

Characteristics		Size	Unit
Chip Size		4600 × 3050	μm
Chip End Coordinates	(1)	−2300, 1525	μm
	(2)	−2300, −1525	
	(3)	2300, −1525	
	(4)	2300, 1525	
Bump Pitch		140	μm
Bump Height		15	μm

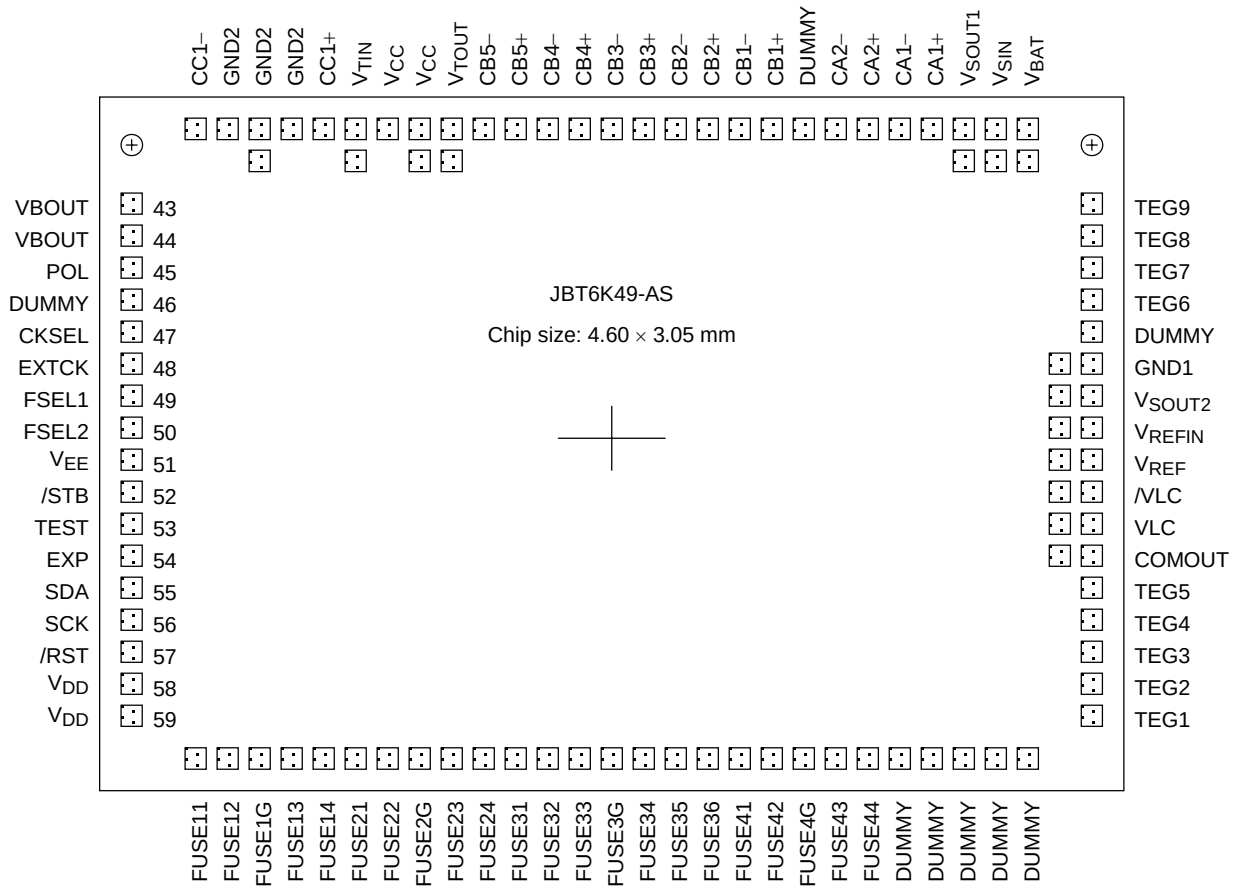
Characteristics	Number of Pins
TEG pin	9
FUSE pin	22

Note 1: The TEG1 to TEG9 pins and the FUSE** pins are reserved for testing by Toshiba. They are not intended to for use in the operation of the JBT6K49-AS. They must always be left open during normal operation.

Alignment Mark Specifications

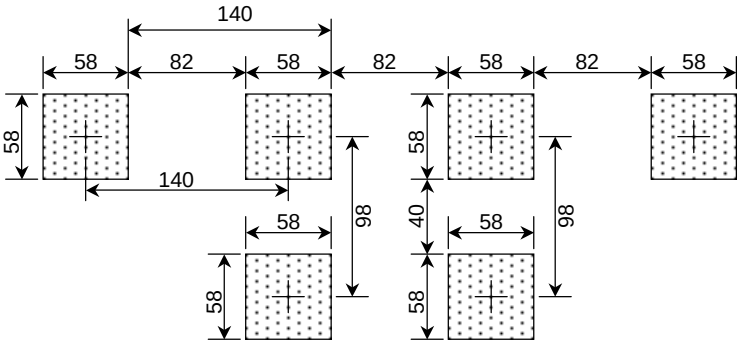


PAD Layout



Input/Output Pins

Unit: μm



Pad Coordinates

[Unit: μm]

No.	Pin Name	X-Coordinate	Y-Coordinate
1	FUSE11	−1890	−1340
2	FUSE12	−1750	−1340
3	FUSE1G	−1610	−1340
4	FUSE13	−1470	−1340
5	FUSE14	−1330	−1340
6	FUSE21	−1190	−1340
7	FUSE22	−1050	−1340
8	FUSE2G	−910	−1340
9	FUSE23	−770	−1340
10	FUSE24	−630	−1340
11	FUSE31	−490	−1340
12	FUSE32	−350	−1340
13	FUSE33	−210	−1340
14	FUSE3G	−70	−1340
15	FUSE34	70	−1340
16	FUSE35	210	−1340
17	FUSE36	350	−1340
18	FUSE41	490	−1340
19	FUSE42	630	−1340
20	FUSE4G	770	−1340
21	FUSE43	910	−1340
22	FUSE44	1050	−1340
23	DUMMY	1190	−1340
24	DUMMY	1330	−1340
25	DUMMY	1470	−1340
26	DUMMY	1610	−1340
27	DUMMY	1750	−1340
28	TEG1	2115	−1240
29	TEG2	2115	−1100
30	TEG3	2115	−960
31	TEG4	2115	−820
32	TEG5	2115	−680
33	COMOUT	2115	−540
34	COMOUT	2015	−540
35	VLC	2115	−400
36	VLC	2015	−400
37	/VLC	2115	−260
38	/VLC	2015	−260
39	V_{REF}	2115	−120
40	V_{REF}	2015	−120
41	V_{REFIN}	2115	20
42	V_{REFIN}	2015	20
43	V_{SOUT2}	2115	160
44	V_{SOUT2}	2015	160
45	GND1	2115	300
46	GND1	2015	300
47	DUMMY	2115	440
48	TEG6	2115	580
49	TEG7	2115	720
50	TEG8	2115	860
51	TEG9	2115	1000
52	V_{BAT}	1750	1340
53	V_{BAT}	1750	1240
54	V_{SIN}	1610	1340
55	V_{SIN}	1610	1240
56	V_{SOUT1}	1470	1340
57	V_{SOUT1}	1470	1240
58	CA1+	1330	1340
59	CA1−	1190	1340
60	CA2+	1050	1340
61	CA2−	910	1340
62	DUMMY	770	1340
63	CB1+	630	1340
64	CB1−	490	1340
65	CB2+	350	1340
66	CB2−	210	1340
67	CB3+	70	1340
68	CB3−	−70	1340
69	CB4+	−210	1340
70	CB4−	−350	1340
71	CB5+	−490	1340
72	CB5−	−630	1340
73	V_{TOUT}	−770	1340
74	V_{TOUT}	−770	1240
75	V_{CC}	−910	1340
76	V_{CC}	−910	1240
77	V_{CC}	−1050	1340
78	V_{TIN}	−1190	1340
79	V_{TIN}	−1190	1240
80	CC1+	−1330	1340
81	GND2	−1470	1340
82	GND2	−1610	1340
83	GND2	−1610	1240
84	GND2	−1750	1340
85	CC1−	−1890	1340
86	V_{BOUT}	−2115	1000
87	V_{BOUT}	−2115	860
88	POL	−2115	720
89	DUMMY	−2115	580
90	CKSEL	−2115	440
91	EXTCK	−2115	300
92	FSEL1	−2115	160
93	FSEL2	−2115	20
94	V_{EE}	−2115	−120
95	/STB	−2115	−260
96	TEST	−2115	−400
97	EXP	−2115	−540
98	SDA	−2115	−680
99	SCK	−2115	−820
100	/RST	−2115	−960
101	V_{DD}	−2115	−1100
102	V_{DD}	−2115	−1240
103	A/M_1	2110	1335
104	A/M_2	−2110	1335

Pin Function Description (1)

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>CKSEL</td><td>I</td><td>External clock pulse selection pin
CKSEL = “L” ・・・ the built-in oscillator is used.
CKSEL = “H” ・・・ an external clock pulse is accepted. It must be input on the EXTCK pin.</td></tr>
<tr><td>EXTCK</td><td>I/O</td><td>External clock pulse input pin
Input an external clock pulse on this pin if External Clock Pulse Supply Mode has been selected. If the built-in oscillator is selected (Self-Oscillation Mode), this pin must be fixed Low.</td></tr>
<tr><td>FSEL1
FSEL2</td><td>I</td><td>Oscillation frequency switching input pins
These pins can be used to select the oscillation frequency for the DC-DC converters.
<table>
<tr><th>FSEL2</th><th>FSEL1</th><th>DC-DC converter clock frequency (typ.)</th></tr>
<tr><td>0</td><td>0</td><td>3.5 kHz</td></tr>
<tr><td>0</td><td>1</td><td>5.0 kHz</td></tr>
<tr><td>1</td><td>0</td><td>7.5 kHz</td></tr>
<tr><td>1</td><td>1</td><td>10.0 kHz</td></tr>
</table></td></tr>
<tr><td>CA1+、CA1−
CA2+、CA2−</td><td>I/O</td><td>DC-DC converter 1 capacitor connection pins
These pins can be connected to voltage booster capacitors. The recommended capacitance for the DC-DC converter capacitors is 1 μF.</td></tr>
<tr><td>V_{SOUT1}
V_{SOUT2}</td><td>O</td><td>DC-DC converter 1 output pins
These pins output the supply voltage (AV_{DD}) for the T6K47. They are electrically connected via an aluminum wire inside the IC chip.
Normally a capacitor with a capacitance of approximately 10 μF is connected across the V_{SS} pins in order to maintain the voltage level.</td></tr>
<tr><td>V_{SIN}</td><td>I</td><td>DC-DC converter 1 power supply input pin
This is the power supply feedback pin for DC-DC converter 1. It is normally connected to the V_{SOUT1} pin.</td></tr>
<tr><td>V_{REFIN}</td><td>I</td><td>Reference voltage input pin
An operational-amplifier output feedback voltage is input on this pin to generate the VS voltage. It should normally be connected to the V_{REF} pin.</td></tr>
<tr><td>V_{REF}</td><td>O</td><td>Reference power supply output pin
This is an operational-amplifier output pin which generates the VS voltage. It is normally connected to a capacitor with a capacitance of 0.1 μF to 0.47 μF. The capacitance should be adjusted as necessary to suit the conditions in which the device is used.</td></tr>
</table>

Pin Function Description (2)

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>CB1+、CB1−
CB2+、CB2−
CB3+、CB3−
CB4+、CB4−
CB5+、CB5−</td><td>I/O</td><td>DC-DC converter 2 capacitor connection pins
Connect these pins to external voltage booster capacitors in order to generate negative voltages for the T6K48. The recommended capacitance for the capacitors is 1 μF.</td></tr>
<tr><td>V_{TOUT}</td><td>O</td><td>DC-DC converter 2 output pin
This pin outputs the supply high-level voltage (+13 V) used for the T6K48.</td></tr>
<tr><td>V_{TIN}</td><td>I</td><td>DC-DC converter 3 supply voltage input pin
The voltage for DC-DC converter 3 used to generate a voltage on the VBOUT pin is input on this pin. It must be connected to the VTOUT pin.</td></tr>
<tr><td>CC1+、CC1−</td><td>I/O</td><td>DC-DC converter 3 capacitor connection pins
Connect these pins to an external voltage booster capacitor in order to generate negative voltages for the T6K48. The recommended capacitance for the DC-DC converter capacitor is 1 μF.</td></tr>
<tr><td>V_{BOUT}</td><td>O</td><td>DC-DC converter 3 output pin
This pin outputs the supply low-level voltage (−13 V) used for the T6K48.</td></tr>
<tr><td>/STB</td><td>I</td><td>Standby signal input pin
The chip stays in standby state while /STB = L. Enabling the /STB pin halts all the built-in circuits.</td></tr>
<tr><td>/RST</td><td>I</td><td>Reset signal input pin
A reset signal must be input on this pin after the power is turned on.</td></tr>
<tr><td>POL</td><td>I</td><td>Alternating signal input pin
This POL signal inverts the phase of the COMOUT, VLC and /VLC signals. See Fig. 2 for an explanation of how to invert the phase.</td></tr>
<tr><td>VLC
/VLC</td><td>—</td><td>γ-correction power supply voltage pin
This pin outputs a voltage whose phase is under the control of the POL signal. The following table lists the output voltages and their phases.
<table>
<tr><th>POL</th><th>VLC</th><th>BVLC</th></tr>
<tr><td>H</td><td>VSO</td><td>0 V</td></tr>
<tr><td>L</td><td>0 V</td><td>VSO</td></tr>
</table></td></tr>
<tr><td>COMOUT</td><td>O</td><td>Common signal output pin
This pin outputs, in phase with the POL signal, a signal whose level has been converted to the board level necessary for the LCD.</td></tr>
<tr><td>EXP</td><td>I</td><td>DC-DC converter ON/OFF switching pin
This pin is used to turn the DC-DC converters ON/OFF. Normally it should be connected to GND.</td></tr>
</table>

Pin Function Description (3)

Pin Name	I/O	Function
V_{BAT}	—	Analog circuit supply voltage
V_{DD}	—	Logic circuit supply voltage
V_{CC}	—	DC-DC converter 2 supply voltage
V_{EE}	—	DC-DC converter 3 supply voltage
GND1、GND2	—	Ground pins Note 2: The GND1 and GND2 pins serve different circuit blocks. Connect both pins to ground.

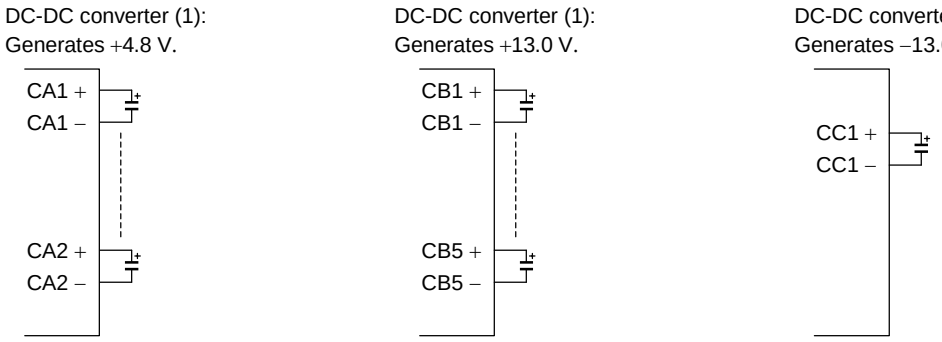
Pin Function Description (4)

Pin Name	I/O	Function
TEST	I	Test mode switching pin This is an enable pin for Toshiba Test Mode. Normally it should be grounded.
SCK	I	Test mode clock pin A clock pulse for serial data transfer used in Toshiba Test Mode is input on this pin. Normally it should be grounded.
SDA	I	Test mode data pin Serial data used in Toshiba Test Mode is input on this pin. Normally it should be grounded.
FUSE**	I	Toshiba test pin (1) This pin is a dedicated pin used only in Toshiba Test Mode. Normally it should be left open.
FUSE*G	I	Toshiba test pin (2) This pin is a dedicated pin used only in Toshiba Test Mode. Normally it should be left open.
TEG**	I	Toshiba test pin (3) This pin is a dedicated pin used only in Toshiba Test Mode. Normally it should be left open.

Description of Functions and Operation

DC-DC converter

The JBT6K49-AS generates an analog supply voltage for the source driver (T6K47) and an LCD-driving voltage for the gate driver (T6K48). The DC-DC converter consists of three circuit blocks which output +4.8 V, +13.0 V and −13.0 V. The ways in which the DC-DC converter can be used are shown below.



Note 2: Connect a voltage boosting kick capacitor or capacitors to each circuit block. Normally the capacitance of the kick capacitor should be 1.0 μF. Connect a 10 μF capacitor across the boosted-voltage output pin and the VSS pin of DC-DC converter (1), since the voltage generated in the DC-DC converter is unstable. In addition, connect a 1 μF capacitor across the boosted-voltage output pin and the V_{SS} pin of DC-DC converter (1).

Oscillation Circuit

The JBT6K49-AS generates the clock pulse used by the DC-DC converter. The FSEL1 and FSEL2 pins can be used to select the clock oscillation frequency. The following table lists the correspondence between the pin settings and the selected frequency.

FSEL2	FSEL1	Oscillation Frequency (initial value)
0	0	3.5 kHz
0	1	5.0 kHz
1	0	7.0 kHz
1	1	10.0 kHz

Note 3: The relationship of the oscillation frequency and the oscillation resistance depends on assembly and measuring conditions.
Therefore, select the oscillation resistance after enough evaluating.

γ-Correction Reference Voltage

The +4.8 V generated by DC-DC converter (1) is used to generate γ-correction reference voltages used by the source driver (T6K47). The voltages generated serve as the maximum and minimum γ-correction voltages. These two voltage levels are switched by the signal input on the POL pin, allowing the γ-correction voltage circuit to be configured easily. Fig.1 is an example of a γ-correction voltage circuit.

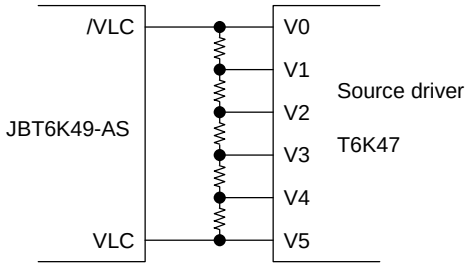


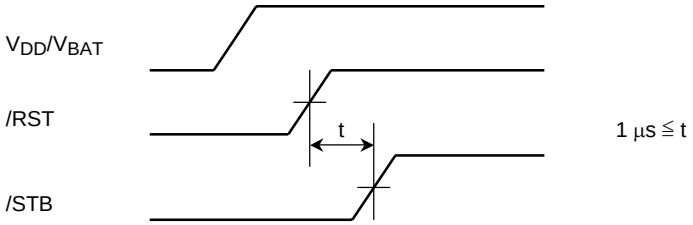
Fig.1 Example of a γ-correction voltage circuit

The following table lists the voltages output from the VLC and /VLC pins and the corresponding levels on the POL pin.

POL	VLC	/VLC	COMOUT
0	0	VSO	0
1	VSO	0	VSO

Power-on

The JBT6K49-AS incorporates a trimming circuit designed to increase the precision of the LCD-driving output voltage. After the power is turned on, the trimming circuit is reset on the leading edge of the signal input on the reset pin. Use the following /RST pin processing sequence after power-on.



Absolute Maximum Ratings (unless otherwise specified, V_{SS} = 0 V and Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Supply Voltage (1)		V_{DD}	−0.3 to 6.0	V
Supply Voltage (2)	(Note 5)	V_{BAT}	−0.3 to 6.5	V
Supply Voltage (3)	(Note 5)	V_{CC}	−0.3 to 20	V
Supply Voltage (4)		V_{EE}	−20 to 0.3	V
Input Voltage		V_{IN}	−0.3 to V_{DD} + 0.3	V
Output Voltage		V_{OUT}	0 to 6.0	V
Operating Temperature		T_{opr}	−20 to 75	°C
Storage Temperature		T_{stg}	−55 to 125	°C

Note 4: The voltages listed in the table are referenced to ground (0 V).

Note 5: $V_{BAT} \leqq V_{CC}$

Electrical Characteristics

DC Characteristics (1)

(unless otherwise specified, V_{DD} = 2.7 V to 3.3 V, V_{BAT} = 2.7 V to 4.2 V and Ta = –20°C to 75°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Related Pins
Operating Supply Voltage (1)	V_{DD}	—	—	2.7	—	3.3	V	V_{DD}
Operating Supply Voltage (2)	V_{BAT}	—	—	2.7	—	4.2	V	V_{BAT}
Input Voltage	V_{IL}	—	—	0	—	0.2 V_{DD}	V	CKSEL, POL, /STB, EXTCK, FSEL1/2, /RST
	V_{IH}	—	—	0.8 V_{DD}	—	V_{DD}		
Input Leakage Current	I_{IL}	—	V_{inp} = V_{DD} to GND	−1.0	—	1.0	μA	CKSEL, POL, /STB, EXTCK, FSEL1/2, /RST
External Clock Frequency	f_{ex}	—	CKSEL = "H"	2	—	8	kHz	EXTCK
External Clock Pulse Duty Ratio	f_{duty}	—		45	50	55	%	EXTCK
External Clock Pulse Rise/Fall Time	t_r/t_f	—		—	—	50	ns	EXTCK

DC Characteristics (2)

(unless otherwise specified, V_{DD} = 2.7 V to 3.3 V, V_{BAT} = 2.7 V to 4.2 V and Ta = –20°C to 75°C, For typical ratings the conditions are: V_{DD} = 3.0V, V_{BAT} = 3.0V and Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Related Pins
Static Drain	I_{DDSTB}	—	/STB = "L"	—	1	5	μA	GND
Dynamic Drain (1)	I_{DD1}	—	With no load	—	0.2	2	μA	V_{DD}
Dynamic Drain (2)	I_{DD2}	—	With typical load F_{osc} = 3.5 kHz	—	0.2	2	μA	V_{DD}
Dynamic Drain (3)	I_{BAT}	—		—	350	500	μA	V_{BAT}

DC Characteristics (3)

(unless otherwise specified, V_{DD} = 2.7 V to 3.3 V, V_{BAT} = 2.7 V to 4.2 V and Ta = –20°C to 75°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Related Pins
DC-DC Converter Characteristic (1)	V_{SO1}	—	I_{load} = 42 μA Ta = 25°C	4.75	4.80	4.85	V	VSOUT
	V_{SO2}	—	I_{load} = 42 μA Ta = –20°C Ta = 75°C	4.75	4.80	4.90		
	V_{SO3}	—	I_{load} = 2.5mA	4.70	—	—		
DC-DC Converter Characteristic (2)	V_{TO1}	—	I_{load} = 0 μA	—	13.0	13.7	V	VTOUT
	V_{TO2}	—	I_{load} = 100 μA	12.3	—	—		
DC-DC Converter Characteristic (3)	V_{BO1}	—	I_{load} = 0 μA	–13.7	–13.0	—	V	VBOUT
	V_{BO2}	—	I_{load} = 100 μA	—	—	–12.3		

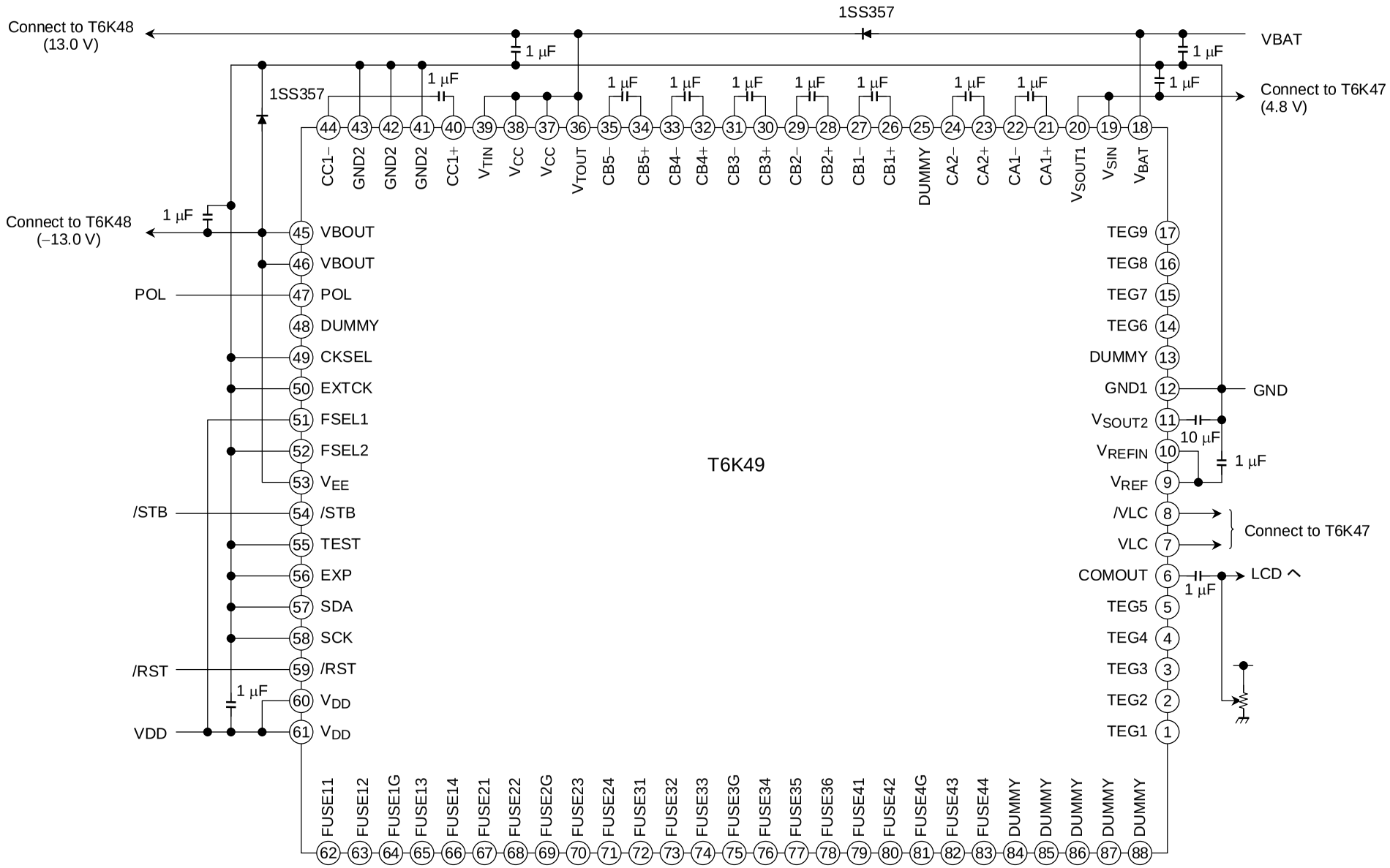
DC Characteristics (4)

(unless otherwise specified, V_{DD} = 2.7 V to 3.3 V, V_{BAT} = 2.7 V to 4.2 V and Ta = –20°C to 75°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Related Pins
γ-Output Voltage Characteristic (1)	V_{LC1H}	—	POL = "H"	V_{SO1} – 0.05	V_{SO1}	V_{SO1} + 0.05	V	VLC
	V_{LC2H}	—		– 0.05	0	0.05	V	/VLC
γ-Output Voltage Characteristic (2)	V_{LC1L}	—	POL = "L"	– 0.05	0	0.05	V	VLC
	V_{LC2L}	—		V_{SO1} – 0.05	V_{SO1}	V_{SO1} + 0.05	V	/VLC
COM Output Voltage Characteristic	V_{comL}	—	POL = "L"	– 0.05	0	0.05	V	COMOUT
	V_{comH}	—	POL = "H"	V_{SO1} – 0.05	V_{SO1}	V_{SO1} + 0.05	V	

Application circuit

Internal CR oscillator used (5 kHz)
Using DC-DC converter



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