

3000-pixel CCD Linear Image Sensor (B/W)

Description

The ILX526A is a rectangular reduction type CCD linear image sensor designed for bar code POS hand scanner and optical measuring equipment use. A built-in timing generator and clock-drivers ensure single 5V power supply for easy use.

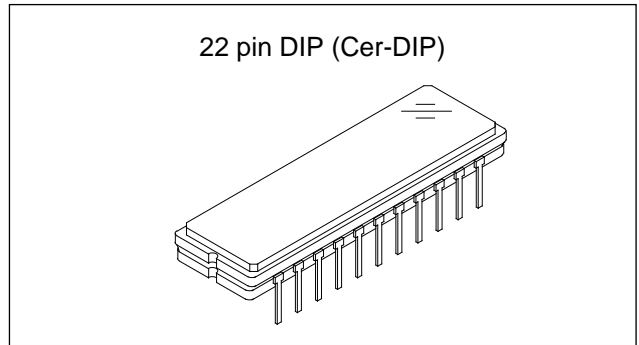
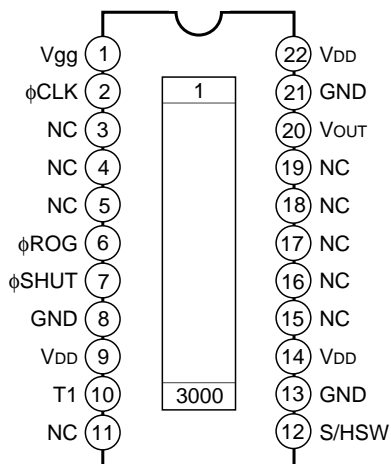
Features

- Number of effective pixels: 3000 pixels
- Pixel size: 7µm × 200µm (7µm pitch)
- Single 5V power supply
- High sensitivity: 300V/(lx · s)
- Built-in timing generator and clock-drivers
- Built-in sample-and-hold circuit
- Electrical shutter function
- Clock frequency: 100kHz (Min), 1MHz (Max)

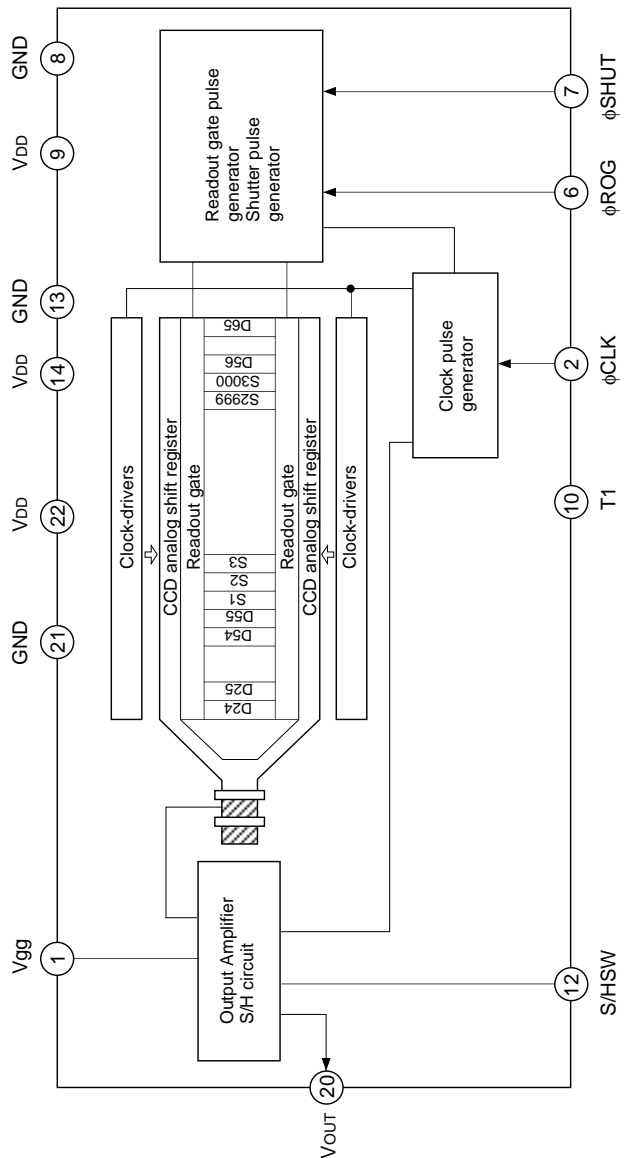
Absolute Maximum Ratings

- Supply voltage V_{DD} 6 V
- Operating temperature -10 to +60 °C
- Storage temperature -30 to +80 °C

Pin Configuration (Top View)



Internal Structure



Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Pin Description

Pin No.	Symbol	Description
1	V _{gg}	Output circuit gate bias
2	ϕ CLK	Clock pulse input
3	NC	NC
4	NC	NC
5	NC	NC
6	ϕ ROG	Readout gate pulse input
7	ϕ SHUT	Electrical Shutter pulse input
8	GND	GND
9	V _{DD}	5V
10	T1	TEST
11	NC	NC
12	S/HSW	Switch (with S/H or without S/H)
13	GND	GND
14	V _{DD}	5V
15	NC	NC
16	NC	NC
17	NC	NC
18	NC	NC
19	NC	NC
20	V _{OUT}	Signal output
21	GND	GND
22	V _{DD}	5V

Mode Description

Mode in Use	12 pin S/HSW
With S/H	GND
Without S/H	V _{DD}

Recommended Voltage

Item	Min.	Typ.	Max.	Unit
V _{DD}	4.5	5.0	5.5	V

Input Pin Capacity

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of ϕ CLK pin	C ϕ CLK	—	10	—	pF
Input capacity of ϕ ROG pin	C ϕ ROG	—	10	—	pF
Input capacity of ϕ SHUT pin	C ϕ ROG	—	10	—	pF

Electro-optical Characteristics (Note 1)

Ta = 25°C, VDD = 5V, Clock frequency: 500kHz, Light source = 3200K, IR cut filter: CM-500S (t = 1.0mm), Without S/H mode

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity 1	R1	210	300	390	V/(lx · s)	Note 2
Sensitivity 2	R2	—	3700	—	V/(lx · s)	Note 3
Sensitivity nonuniformity	PRNU	—	5.0	10.0	%	Note 4
Saturation output voltage	VSAT	0.6	0.8	—	V	—
Dark voltage average	VDRK	—	2.5	6.0	mV	Note 5
Dark signal nonuniformity	DSNU	—	5.0	12.0	mV	Note 6
Image lag	IL	—	5.0	—	%	Note 7
Dynamic range	DR	—	320	—	—	Note 8
Saturation exposure	SE	—	0.003	—	lx · s	Note 9
5V current consumption	IVDD	—	7.0	17.0	mA	—
Total transfer efficiency	TTE	92.0	97.0	—	%	—
Output impedance	Zo	—	250	—	Ω	—
Offset level	Vos	—	2.5	—	V	Note 10

Note)

- In accordance with the given electrooptical characteristics, the even black level is defined as the average value of D24, D26 to D52. The odd black level is defined as the average value of D25, D27 to D53.
- For the sensitivity test light is applied with a uniform intensity of illumination.
- Light source: LED λ = 660nm
- PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 2.

$$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100 [\%]$$

Where the 3000 pixels are divided into blocks of even and odd pixels, respectively, the maximum output of each block is set to VMAX, the minimum output to VMIN and the average output to VAVE.

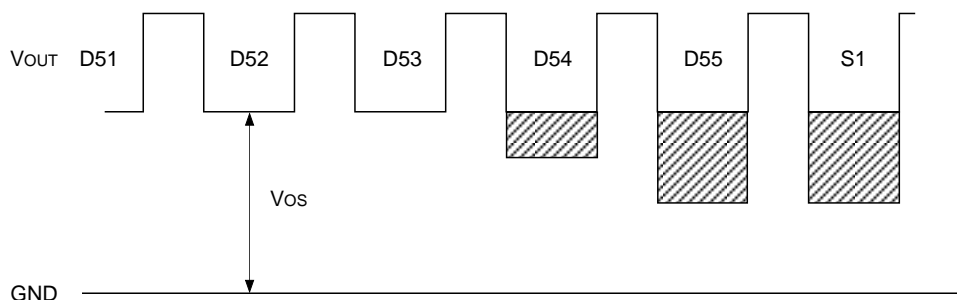
- Integration time is 10ms.
- The difference between the maximum and average values of the dark output voltage is calculated for even and odd respectively. Integration time is 10ms.
- Typical value is used for clock pulse and readout pulse. VOUT = 500mV.

$$8. \quad DR = \frac{V_{SAT}}{V_{DRK}}$$

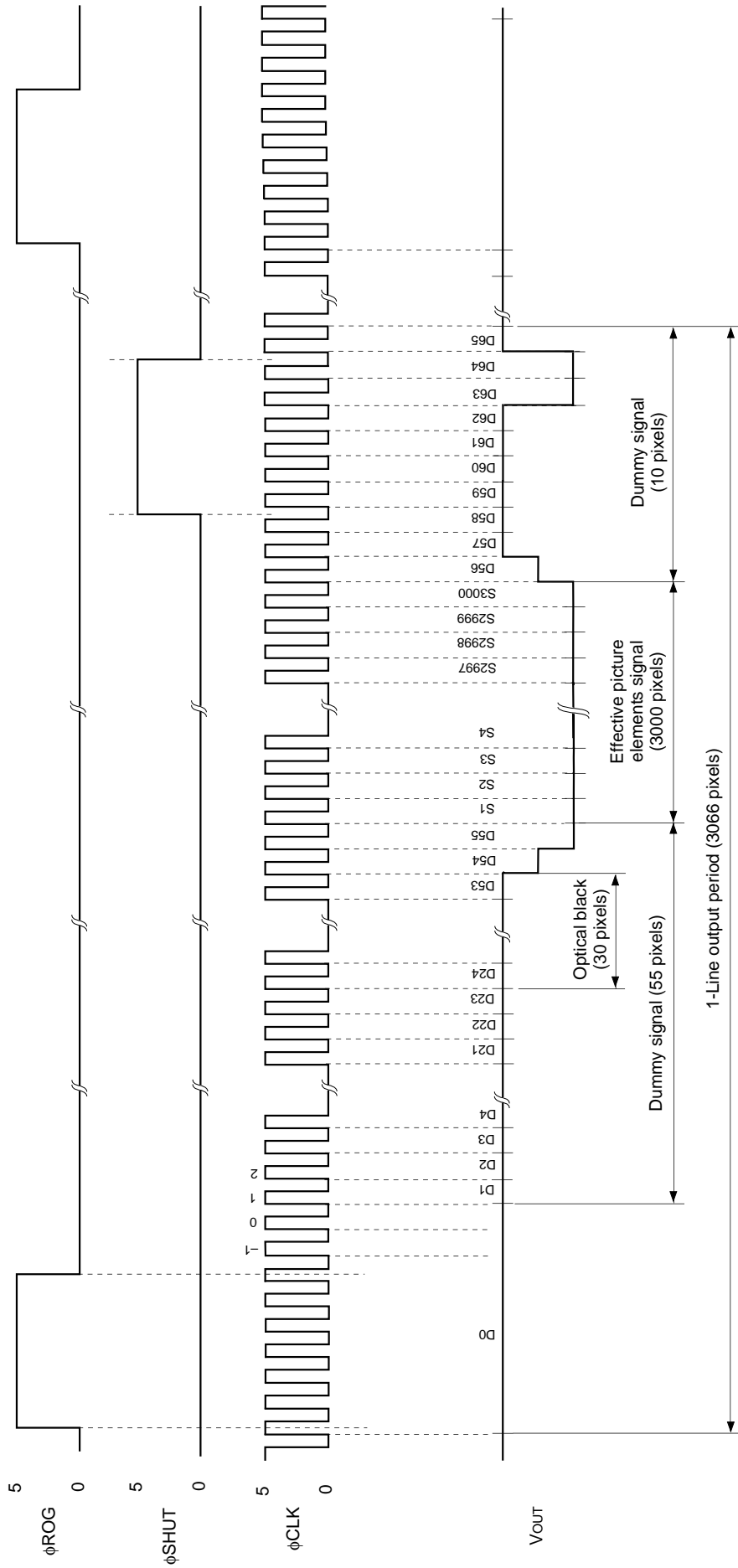
When optical integration time is shorter, the dynamic range sets wider because dark voltage is in proportion to optical integration time.

$$9. \quad SE = \frac{V_{SAT}}{R1}$$

- Vos is defined as indicated below.

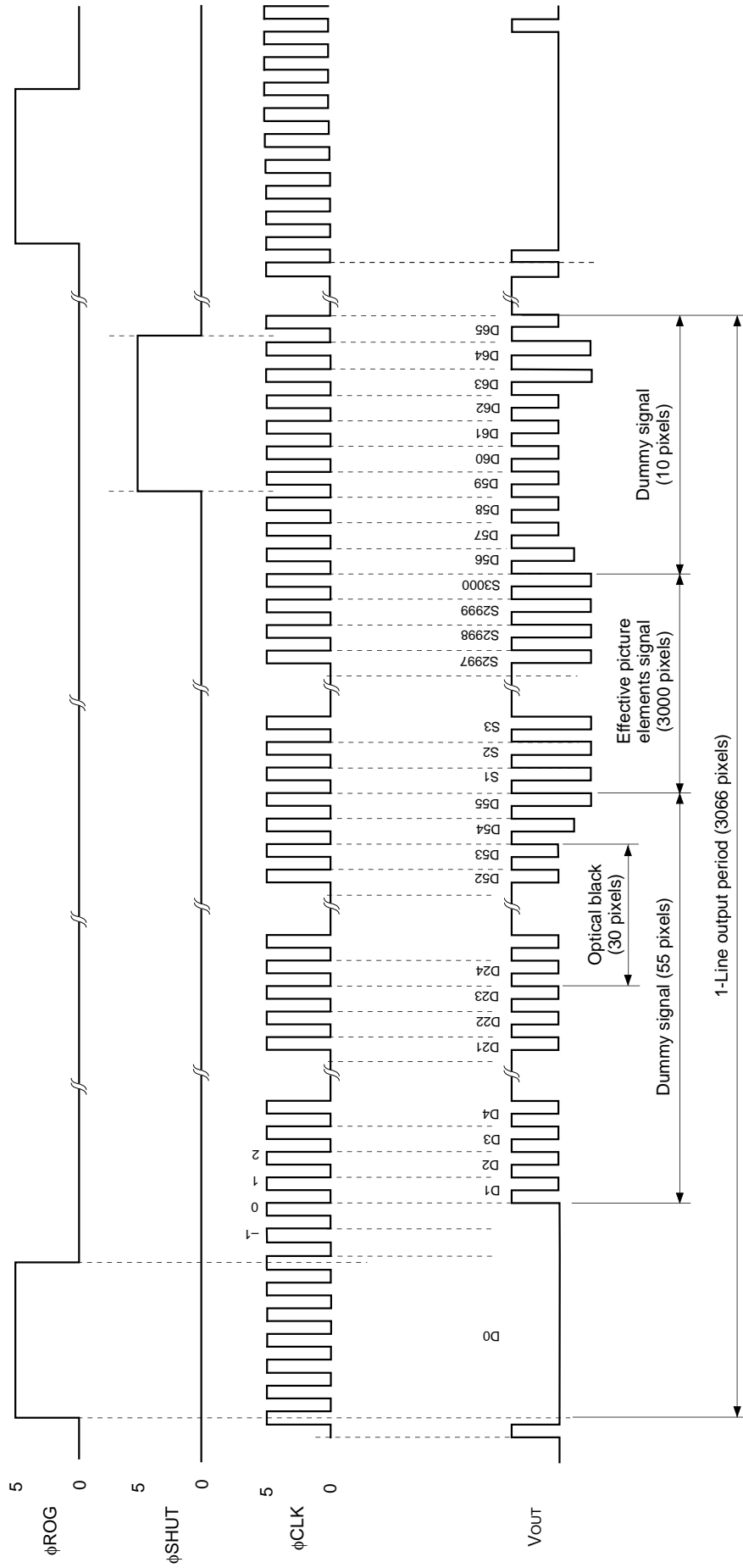


Clock Timing Diagram (With S/H mode)



3100 or more clock pulses are required.

Clock Timing Diagram (Without S/H mode)



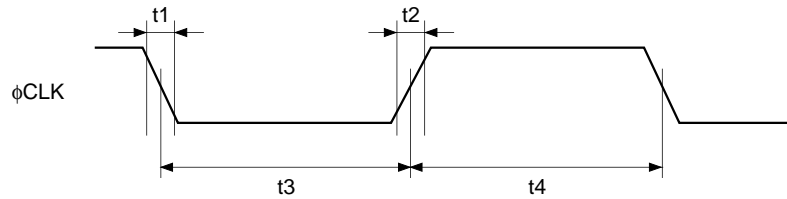
3100 or more clock pulses are required.

Input Clock Voltage Condition

Item	Min.	Typ.	Max.	Unit
V _{IH}	4.5	V _{DD}	5.5	V
V _{IL}	0.0	—	0.1	V

* This is applied to the all external pulses.
(ϕ CLK, ϕ ROG, ϕ SHUT)

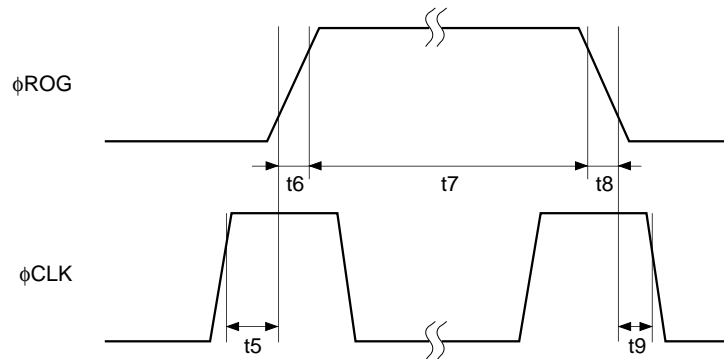
ϕ CLK Timing (For all modes)



Item	Symbol	Min.	Typ.	Max.	Unit
ϕ CLK pulse rise/fall time	t_1, t_2	0	10	100	ns
ϕ CLK pulse Duty*1	—	40	50	60	%

*1 $100 \times t_4 / (t_3 + t_4)$

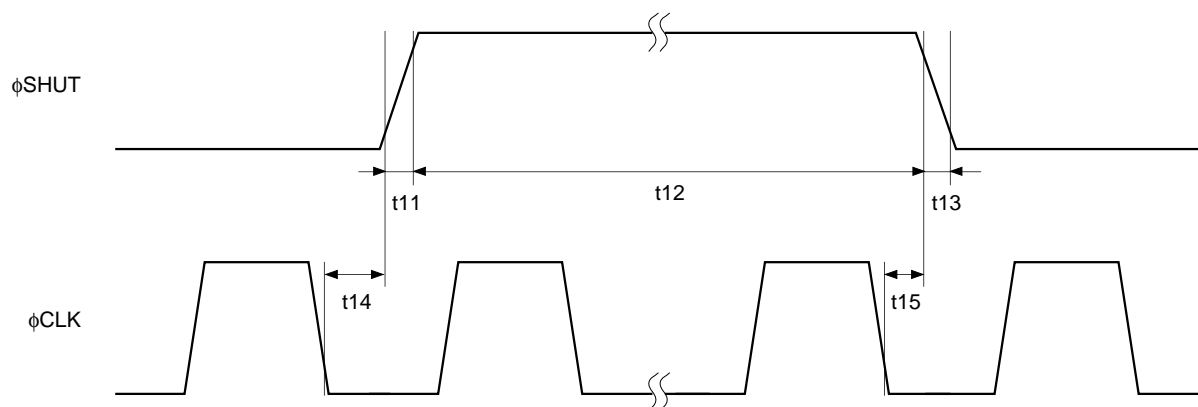
ϕ ROG, ϕ CLK Timing



Item	Symbol	Min.	Typ.	Max.	Unit
ϕ ROG, ϕ CLK pulse timing 1	t_5	$(1/8) \tau$	$(1/4) \tau$	$(3/8) \tau$	ns
ϕ ROG, ϕ CLK pulse timing 2	t_9	$(1/8) \tau$	$(1/4) \tau$	$(3/8) \tau$	ns
ϕ ROG pulse rise/fall time	t_6, t_8	0	10	100	ns
ϕ ROG pulse period	t_7	6τ	10τ	20τ	ns

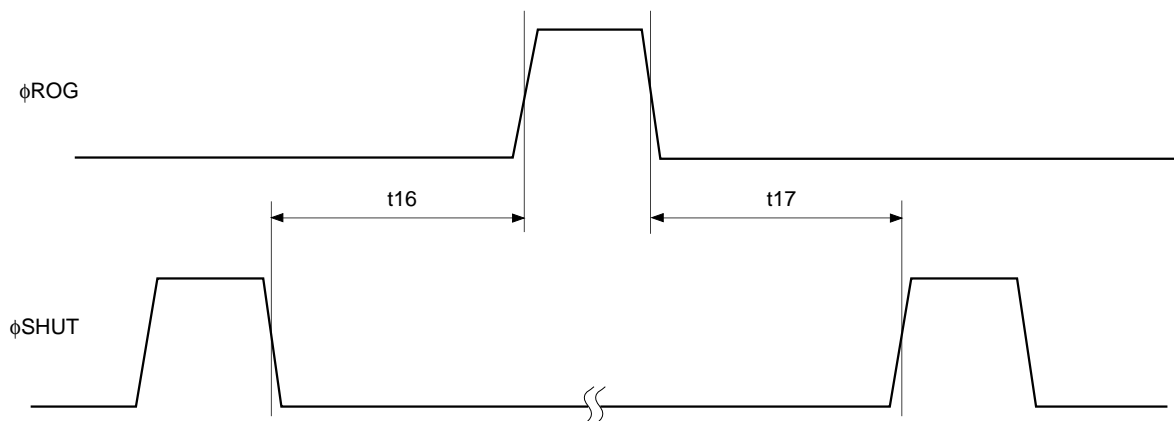
Note) τ is the period of ϕ CLK.

ϕ SHUT, ϕ CLK Timing



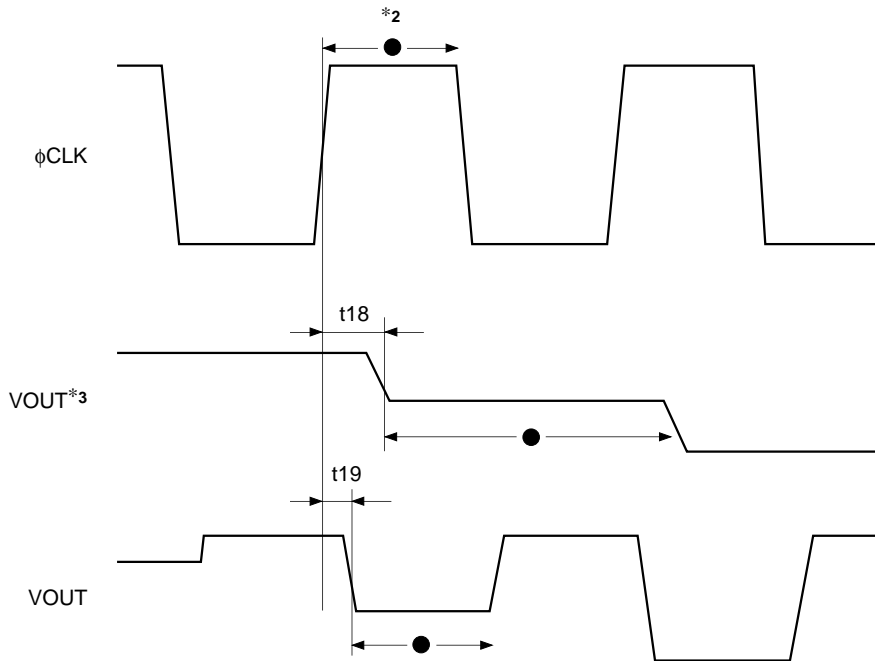
Item	Symbol	Min.	Typ.	Max.	Unit
ϕ SHUT pulse rise/fall time	t11, t13	0	10	100	ns
ϕ SHUT pulse period	t12	4000	5000	—	ns
ϕ SHUT, ϕ CLK pulse timing 1	t14	150	200	250	ns
ϕ SHUT, ϕ CLK pulse timing 2	t15	150	200	250	ns

ϕ ROG, ϕ SHUT Timing



Item	Symbol	Min.	Typ.	Max.	Unit
ϕ ROG, ϕ SHUT pulse timing	t16, t17	10 τ	—	—	ns

ϕ CLK-VOUT Timing *1



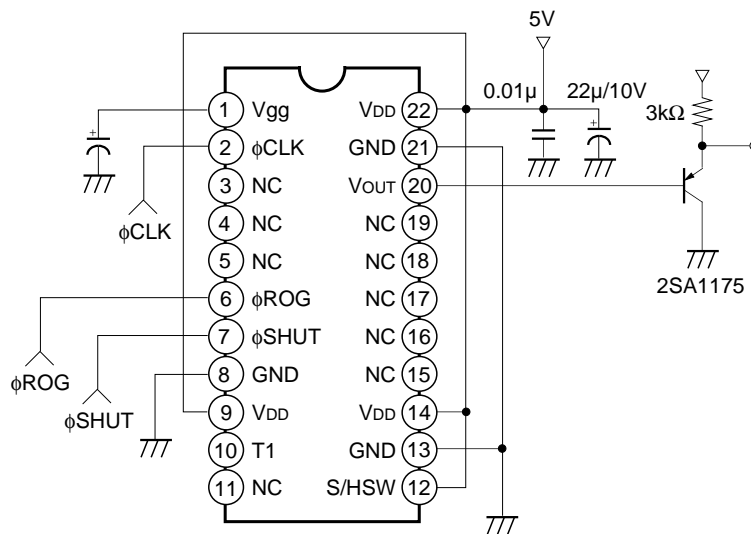
Item	Symbol	Min.	Typ.	Max.	Unit
ϕ CLK-VOUT output delay time1	t18	—	230	—	ns
ϕ CLK-VOUT output delay time2	t19	—	210	—	ns

*1 fck = 500kHz, ϕ CLK Duty = 50%, ϕ CLK rise/fall time = 10ns

*2 ● is data period

*3 Using internal sample-and-hold circuit

Application Circuit (Without S/H mode (Note))

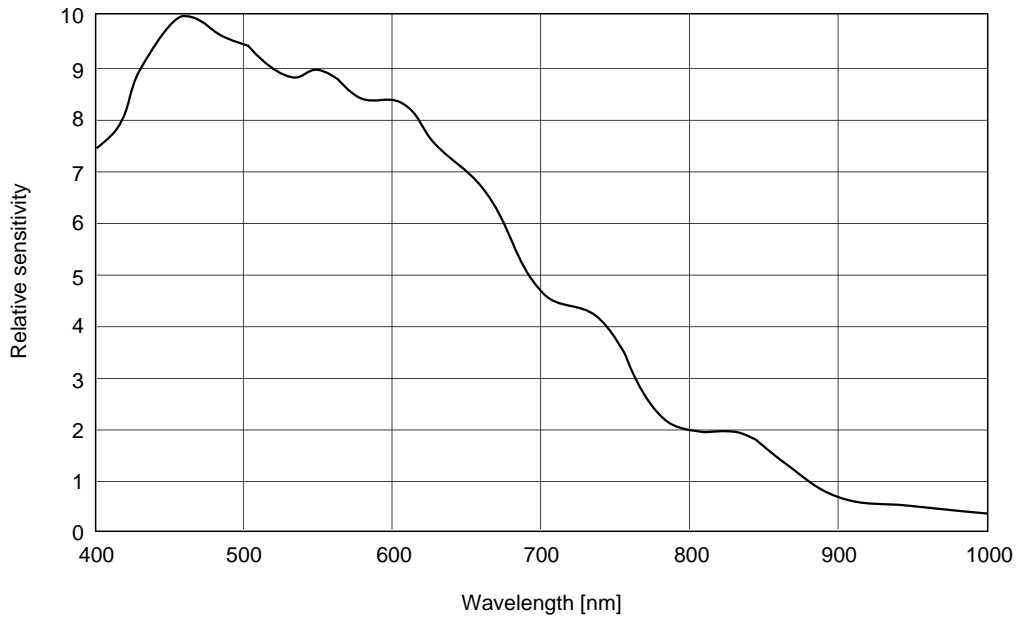


Note) This circuit diagram is the case when internal S/H is not used.

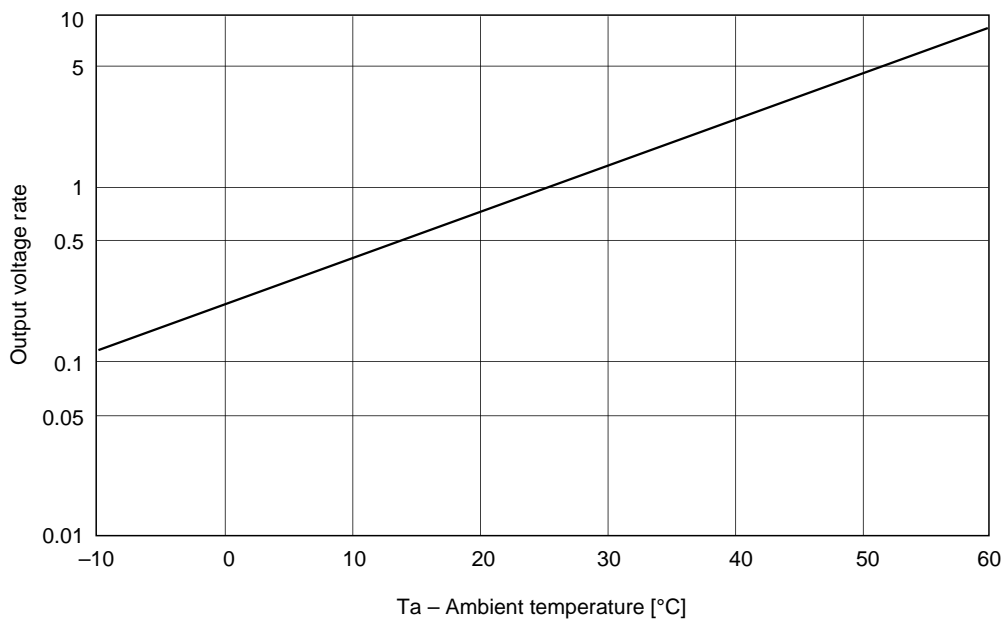
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics ($V_{DD} = 5V$, $T_a = 25^\circ C$)

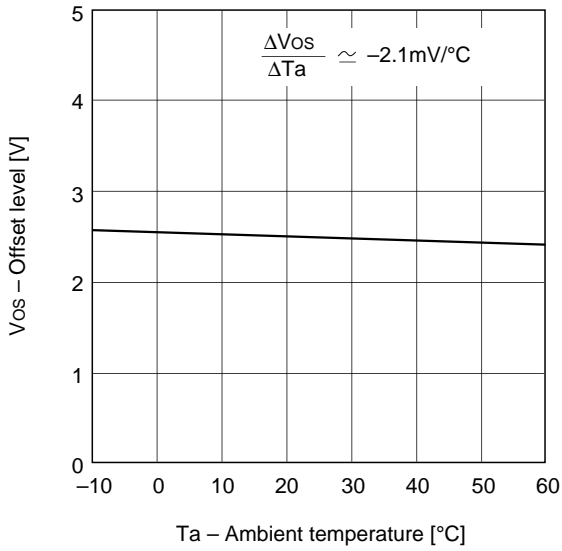
Spectral sensitivity characteristics (Standard characteristics)



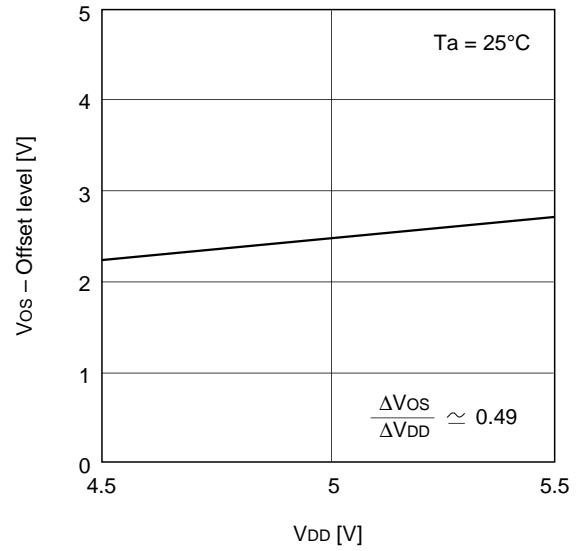
Dark signal output temperature characteristics (Standard characteristics)



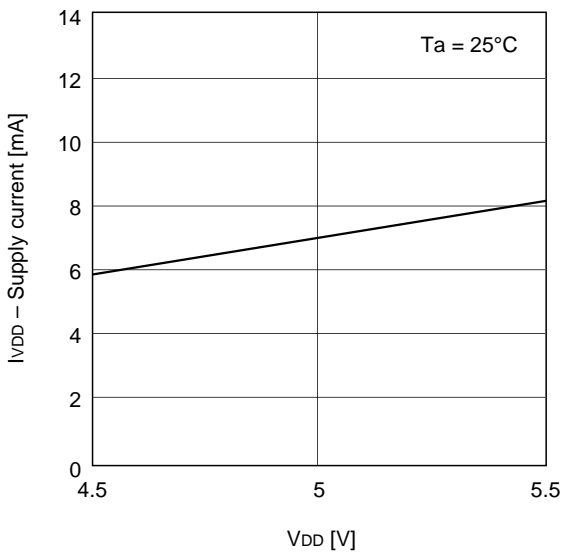
**Offset level vs. Temperature characteristics
(Standard characteristics)**



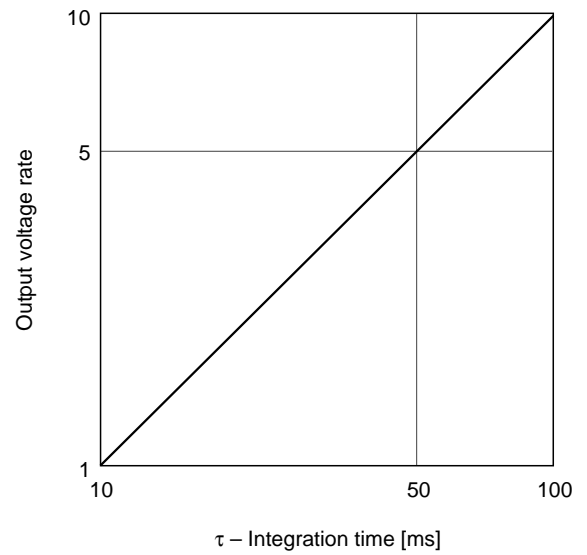
**Offset level vs. VDD characteristics
(Standard characteristics)**



**Supply current vs. VDD characteristics
(Standard characteristics)**



**Output voltage vs. Integration time
(Standard characteristics)**



Notes of Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

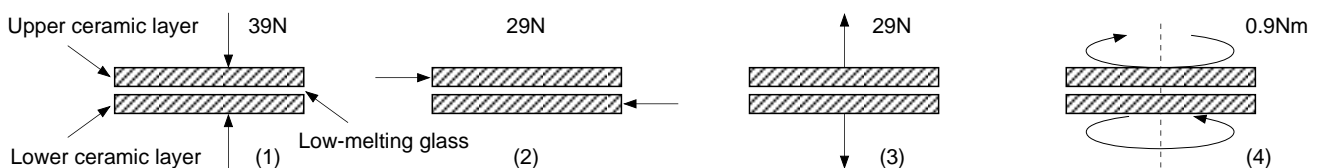
- a) Either handle bare handed or use non chargeable gloves, clothes or material.
Also use conductive shoes.
- b) When handling directly use an earth band.
- c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
- d) Ionized air is recommended for discharge when handling CCD image sensor.
- e) For the shipment of mounted substrates, use boxes treated for prevention of static charges.

2) Notes on Handling CCD Cer-DIP Packages

The following points should be observed when handling and installing cer-DIP packages.

a) Remain within the following limits when applying static load to the ceramic portion of the package:

- (1) Compressive strength: 39N/surface (Do not apply load more than 0.7mm inside the outer perimeter of the glass portion.)
- (2) Shearing strength: 29N/surface
- (3) Tensile strength: 29N/surface
- (4) Torsional strength: 0.9Nm



b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.

c) Be aware that any of the following can cause the glass to crack: because the upper and lower ceramic layers are shielded by low-melting glass,

- (1) Applying repetitive bending stress to the external leads.
- (2) Applying heat to the external leads for an extended period of time with soldering iron.
- (3) Rapid cooling or heating.
- (4) Applying a load or impact to a limited portion of the low-melting glass with a small-tipped tool such as tweezers.
- (5) Prying the upper or lower ceramic layers away at a support point of the low-melting glass.

Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.

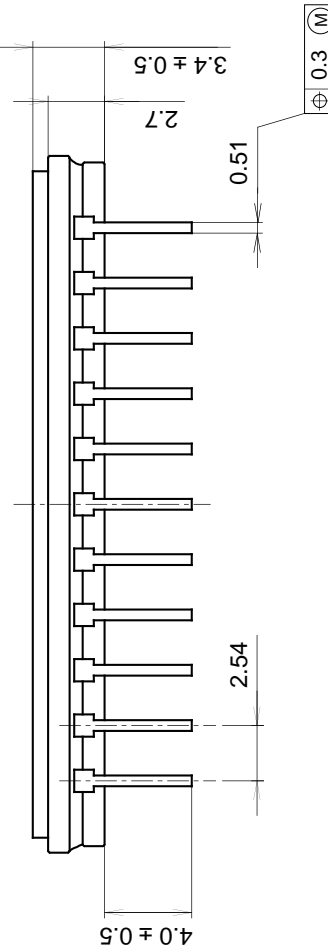
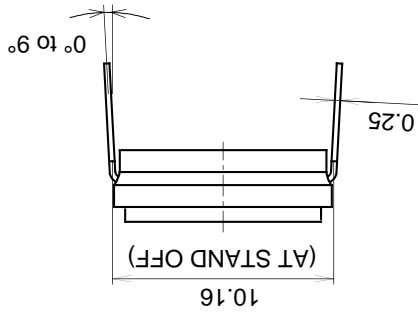
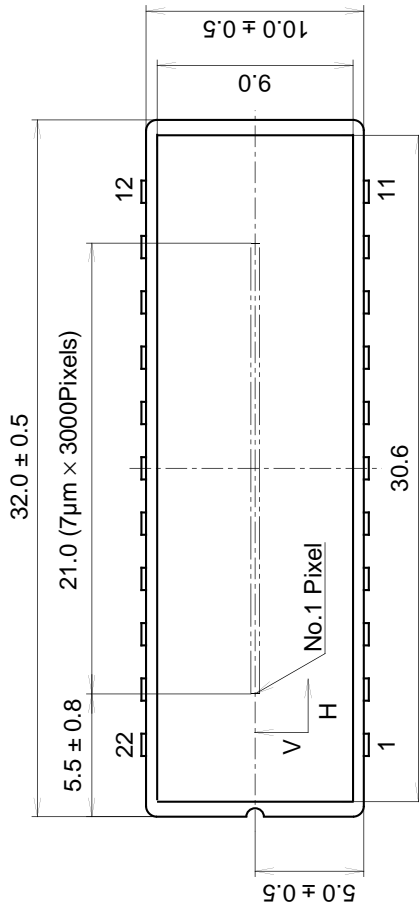
3) Soldering

- a) Make sure the package temperature does not exceed 80°C.
- b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
- c) To dismount an imaging device, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

- 4) Dust and dirt protection
 - a) Operate in clean environments.
 - b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
 - c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
 - d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
- 5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
- 6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.
- 7) Normal output signal is not obtained immediately after device switch on.

Package Outline Unit: mm

22pin DIP (400mil)



1. The height from the bottom to the sensor surface is 1.61 ± 0.3mm.
2. The thickness of the cover glass is 0.7mm, and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Cer-DIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	3.0g