



3.3V FAST CMOS REGISTERED ADDRESS LINE DRIVER

IDT74FCT16V345

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical tsk(o) (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Vcc = 3.3V ± 0.3V, Normal Range or Vcc = 2.7 to 3.6V, Extended Range Vcc = 2.5V ± 0.2V
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in SSOP, TSSOP, and TVSOP Packages

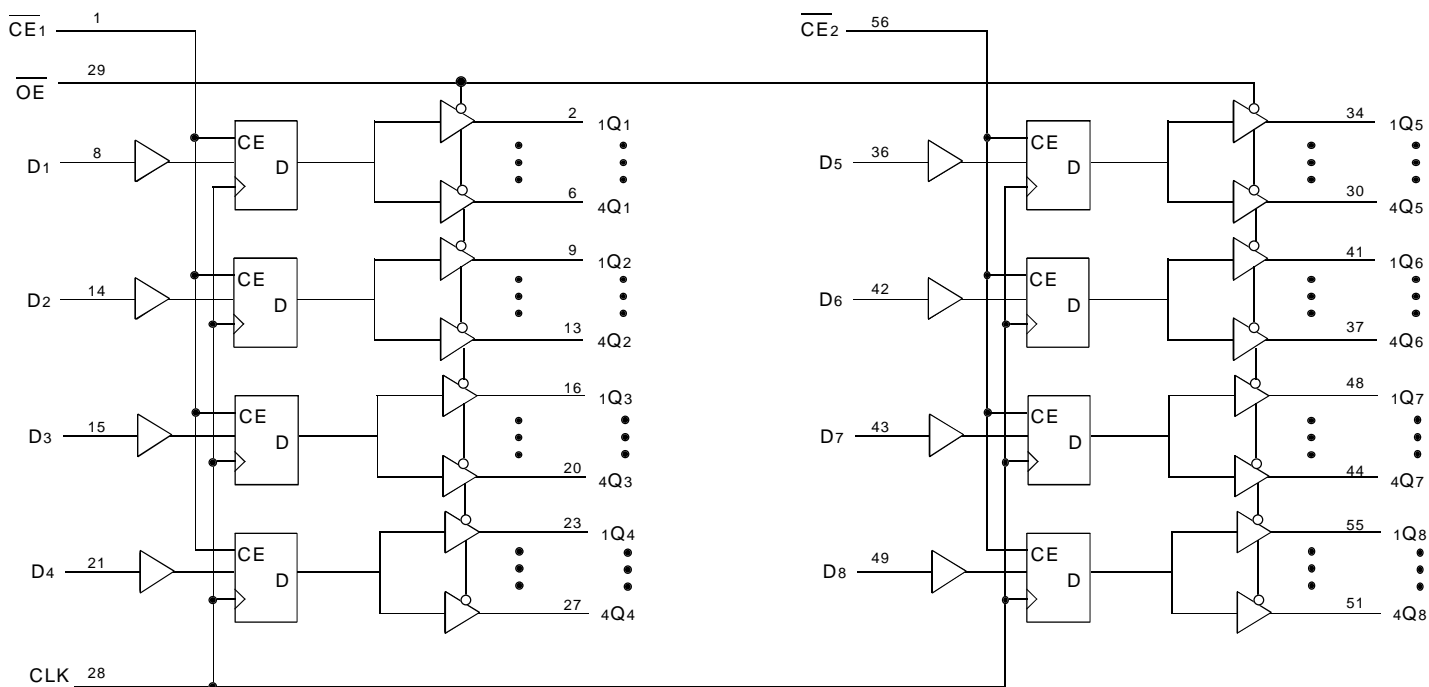
DESCRIPTION:

The FCT16V345 is a registered address driver built using advanced dual metal CMOS technology. The device is configured with fan out of four for use in high speed synchronous memory applications.

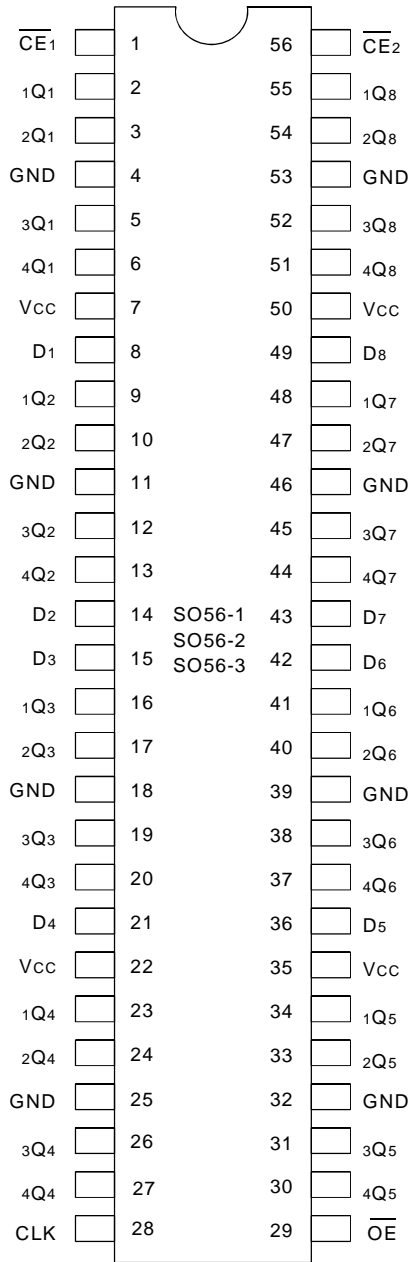
The FCT16V345 is ideal for driving memory modules in systems where multiple memory modules are used. If each of the four output banks drives a different module, modules can be added or removed without affecting the signal integrity of the other modules in the system.

Dual Clock Enables (\overline{CE}_x) allow use of the FCT16V345 in high speed memory interleaving applications where the clock can be alternately enabled and disabled, allowing the address to be held for additional clock cycles during memory access.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Description | Max | Unit |
|----------------------|--------------------------------------|-----------------|------|
| VTERM ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +4.6 | V |
| VTERM ⁽³⁾ | Terminal Voltage with Respect to GND | -0.5 to VCC+0.5 | V |
| TSTG | Storage Temperature | -65 to +150 | °C |
| IOUT | DC Output Current | -60 to +60 | mA |

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Non bus-hold input terminals and Vcc terminals.
- Output, I/O terminals, and bus-hold input terminals.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Typ. | Max. | Unit |
|--------|--------------------------|------------|------|------|------|
| CIN | Input Capacitance | VIN = 0V | 3.5 | 6 | pF |
| COU | Output Capacitance | VOUT = 0V | 3.5 | 8 | pF |

3v16-link

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

| Pin Names | Description |
|-------------------|--|
| \overline{OE} | 3-State Output Enable Input (Active LOW) |
| Dx | Inputs |
| xQx | 3-State Outputs |
| CLK | Clock Input |
| \overline{CE}_x | Clock Enable (Active LOW) |

FUNCTION TABLE(1)

| Inputs | | | | Outputs |
|-------------------|-----|-----------------|----|------------------|
| \overline{CE}_x | CLK | \overline{OE} | Dx | xQx |
| H | X | L | X | B ⁽²⁾ |
| X | L | L | X | B ⁽²⁾ |
| L | ↑ | L | L | L |
| L | ↑ | L | H | H |
| X | X | H | X | Z |

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
Z = High-Impedance
- Output level before indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

| Symbol | Parameter | Test Conditions | | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|---|--|--|----------------------------------|------|---------------------|------|------|
| V _{IH} | Input HIGH Voltage Level | V _{CC} = 2.3V to 2.7V | | 1.7 | — | 3.6 | V |
| | | V _{CC} = 2.7V to 3.6V | | 2 | — | 3.6 | |
| V _{IL} | Input LOW Voltage Level | V _{CC} = 2.3V to 2.7V | | -0.5 | — | 0.7 | V |
| | | V _{CC} = 2.7V to 3.6V | | -0.5 | — | 0.8 | |
| I _{IH} | Input HIGH Current | V _{CC} = 3.6V | V _I = V _{CC} | — | — | ±1 | μA |
| I _{IL} | Input LOW Current | V _{CC} = 3.6V | V _I = GND | — | — | ±1 | |
| IoZH IoZL | High Impedance Output Current (3-State Output pins) | V _{CC} = 3.6V | V _O = V _{CC} | — | — | ±1 | μA |
| | | | V _O = GND | — | — | ±1 | |
| V _{IK} | Clamp Diode Voltage | V _{CC} = 2.3V, I _{IN} = -18mA | | — | -0.7 | -1.2 | V |
| V _H | Input Hysteresis | — | | — | 100 | — | mV |
| I _{CC} L I _{CC} H I _{CC} Z | Quiescent Power Supply Current | V _{CC} = 3.6V V _{IN} = GND or V _{CC} | | — | 0.1 | 10 | μA |

NOTE:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Max. | Unit |
|-----------------|---------------------|--------------------------------|-------------------------|-----------------------|------------------------|------|
| V _{OH} | Output HIGH Voltage | V _{CC} = 2.3V | I _{OH} = 0.1mA | V _{CC} - 0.2 | — | V |
| | | | I _{OH} = -6mA | 2 | — | |
| | | V _{CC} = 2.7V | I _{OH} = -12mA | 1.7 | — | |
| | | | | 2.2 | — | |
| | | | | 2.4 | — | |
| | | V _{CC} = 3V | I _{OH} = -24mA | 2.2 | — | |
| V _{OL} | Output LOW Voltage | V _{CC} = 2.3V | I _{OL} = 0.1mA | — | 0.2 | V |
| | | | I _{OL} = 6mA | — | 0.4 | |
| | | | I _{OL} = 12mA | — | 0.7 | |
| | | V _{CC} = 2.7V | I _{OL} = 12mA | — | 0.4 | |
| | | | | V _{CC} = 3V | I _{OL} = 24mA | |

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range.

POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|-----------------|---|--|--|------|---------------------|------|---------------|
| ΔI_{CC} | Quiescent Power Supply Current TTL Inputs HIGH | $V_{CC} = \text{Max.}$ $V_{IN} = V_{CC} - 0.6V^{(3)}$ | | — | 2 | 3 | μA |
| I_{CCD1} | Dynamic Power Supply Current ⁽⁴⁾ | $V_{CC} = \text{Max.}$ Outputs Open $\overline{OE} = GND$ One Clock Input Bit Toggling No Output Bits Toggling 50% Duty Cycle | $V_{IN} = V_{CC}$ $V_{IN} = GND$ | — | 37 | 50 | $\mu A / MHz$ |
| I_{CCD2} | Dynamic Power Supply Current ⁽⁴⁾ | $V_{CC} = \text{Max.}$ Outputs Open $\overline{OE} = GND$ One Input Bit Toggling Four Output Bits Toggling One Clock Input Toggling 50% Duty Cycle | $V_{IN} = V_{CC}$ $V_{IN} = GND$ | — | 252 | 300 | $\mu A / MHz$ |
| I_C | Total Power Supply Current ⁽⁶⁾ | $V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10MHz$ 50% Duty Cycle $\overline{OE} = \overline{CE}_X = GND$ At $f_i = 5MHz$ 50% Duty Cycle One Input Bit Toggling Four Output Bits Toggling One Clock Input Toggling | $V_{IN} = V_{CC}$ $V_{IN} = GND$ | — | 1.63 | 2.01 | mA |
| | | | $V_{IN} = V_{CC} - 0.6V$ $V_{IN} = GND$ | — | 1.63 | 2.04 | |
| | | $V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10MHz$ 50% Duty Cycle $\overline{OE} = \overline{CE}_X = GND$ At $f_i = 2.5MHz$ 50% Duty Cycle Eight Input Bits Toggling Thirty Two Output Bits Toggling One Clock Input Toggling | $V_{IN} = V_{CC}$ $V_{IN} = GND$ | — | 5.41 | 6.51 | |
| | | | $V_{IN} = V_{CC} - 0.6V$ $V_{IN} = GND$ | — | 5.42 | 6.65 | |

NOTES:

- $V_{CC} (\text{max.}) = 3.6V$
- Typical values are at $V_{CC} = 3.3V$, $+25^\circ C$ ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (I}_{CCL}, I_{CC}H \text{ and } I_{CC}Z)$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

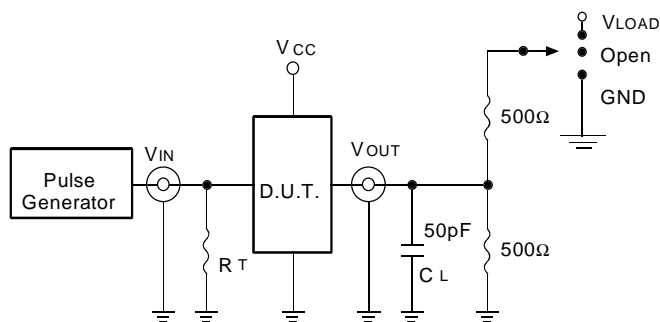
| Symbol | Parameter | Condition ⁽¹⁾ | V _{CC} = 2.5V±0.2V | | V _{CC} = 2.7V | | V _{CC} = 3.3V±0.3V | | Unit |
|--------------------------------------|---|--------------------------|-----------------------------|------|------------------------|------|-----------------------------|------|------|
| | | | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | |
| t _{PLH} t _{PHL} | Propagation Delay CLK to xQx | CL = 50pF RL = 500Ω | 1.5 | 7 | 1.5 | 6 | 1.5 | 5.5 | ns |
| t _{PZH} t _{PZL} | Output Enable Time \overline{OE} to xQx | | 1.5 | 7.7 | 1.5 | 6.9 | 1.5 | 6 | ns |
| t _{PHZ} t _{PLZ} | Output Disable Time \overline{OE} to xQx | | 1.5 | 6.2 | 1.5 | 5.2 | 1.5 | 4.9 | ns |
| t _{SU} | Set-Up Time HIGH or LOW \overline{CE} to CLK | | 2 | — | 2 | — | 1.2 | — | ns |
| t _H | Hold Time HIGH or LOW \overline{CE} to CLK | | 0 | — | 0 | — | 0 | — | ns |
| t _{SU} | Set-Up Time HIGH or LOW Dx to CLK | | 2 | — | 2 | — | 0.8 | — | ns |
| t _H | Hold Time HIGH or LOW CLK to Dx | | 0 | — | 0 | — | 0 | — | ns |
| t _w | CLK Pulse Width HIGH or LOW ⁽⁵⁾ | | 3 | — | 3 | — | 3 | — | ns |
| t _{SK(o)} | Output Skew ⁽³⁾ | | — | 500 | — | 500 | — | 500 | ps |
| t _{SK(b)} | Bank Skew ⁽⁴⁾ | | — | 350 | — | 350 | — | 350 | ps |

NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on propagation delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. Skew between any two outputs with a common input signal. This parameter is guaranteed by design.
5. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



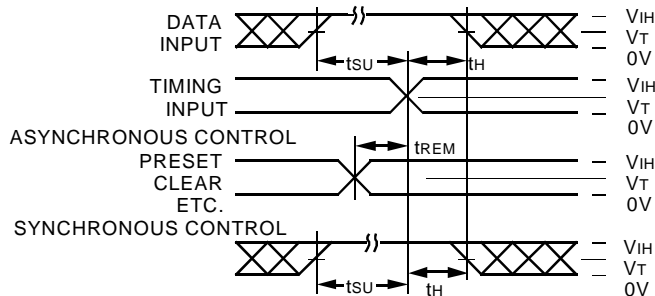
SWITCH POSITION

| Test | Switch |
|-----------------|--------|
| Disable Low | VLOAD |
| Enable Low | |
| Disable High | GND |
| Enable High | |
| All Other Tests | Open |

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

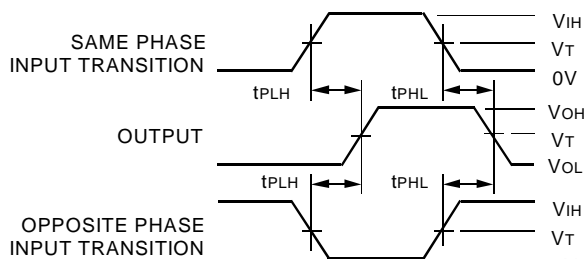
SET-UP, HOLD, AND RELEASE TIMES



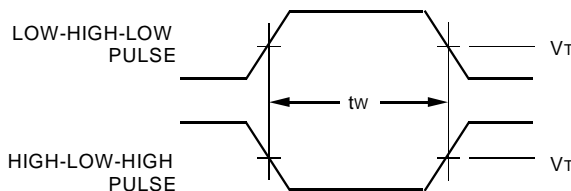
TEST VOLTAGES

| Symbol | Vcc=3.3V±0.3V | Vcc=2.7V | Vcc=2.7V±0.2V | Unit |
|--------|---------------|----------|---------------|------|
| VLOAD | 6 | 6 | 4.6 | V |
| VIH | 2.7 | 2.7 | 2.3 | V |
| VT | 1.5 | 1.5 | 1.2 | V |

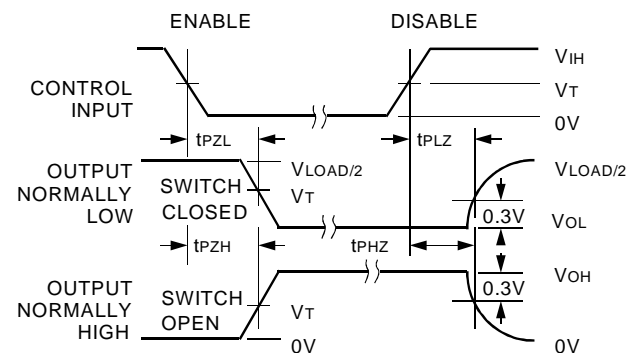
PROPAGATION DELAY



PULSE WIDTH



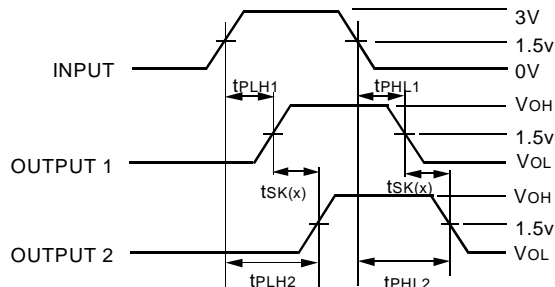
ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tf ≤ 2.5ns; tr ≤ 2.5ns.

OUTPUT SKEW - tsk(x)

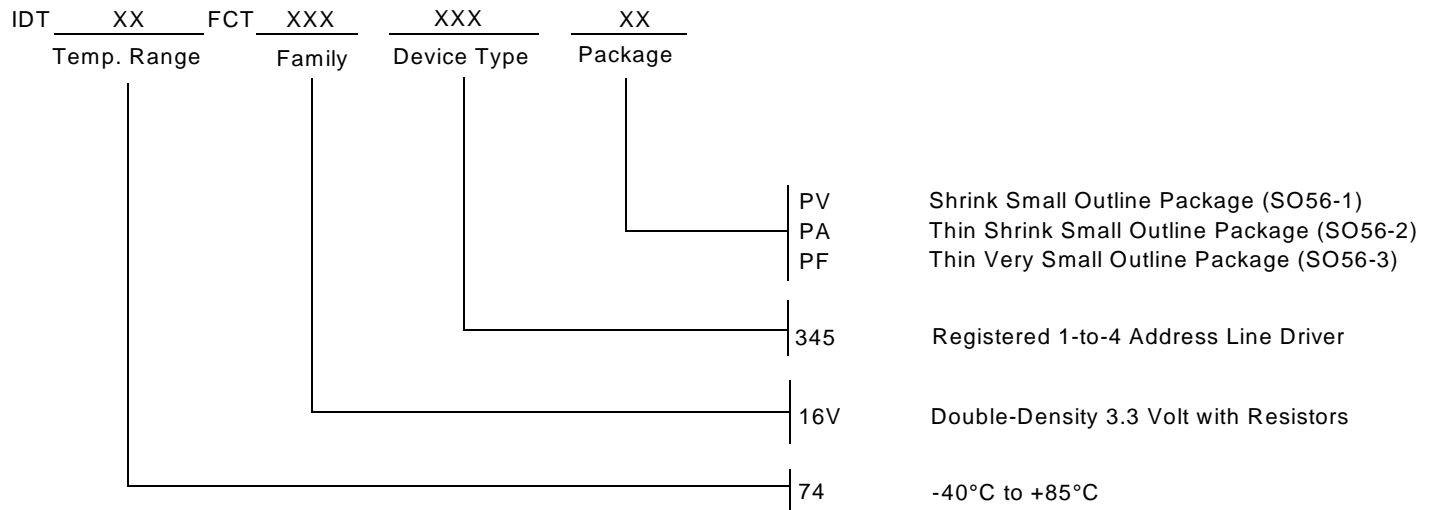


$$tsk(x) = |tPLH2 - tPLH1| \text{ or } |tPHL2 - tPHL1|$$

NOTES:

- For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.
- For tsk(o) OUTPUT1 and OUTPUT2 are in different banks on the same part.

ORDERING INFORMATION



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