# 32-Channel LCD Driver with Separate Backplane Output 

## Ordering Information

| Device | Package Options |  |  |
| :---: | :---: | :---: | :---: |
|  | 44 Lead Quad <br> Plastic Gullwing | 44 J-Lead Quad <br> Plastic Chip Carrier | Die <br> in waffle pack |
|  | HV66PG | HV66PJ | HV66X |

## Features

- Processed with HVCMOS ${ }^{\circledR}$ technology
- 32 push-pull CMOS output up to 60 V
- Low power level shifting
- Source/sink current minimum 1mA
- Shift register speed 5 MHz
$\square$ Latched data outputs
- Bidirectional shift register (DIR)
- Backplane output

Absolute Maximum Ratings ${ }^{1}$

| Supply voltage, $\mathrm{V}_{\mathrm{DD}}{ }^{2}$ | -0.5 V to +7.0 V |
| :--- | ---: |
| Output voltage, $\mathrm{V}_{\mathrm{PP}}{ }^{2}$ | -0.5 V to +70 V |
| Logic input levels ${ }^{2}$ | -0.5 V to $\mathrm{V}_{\mathrm{DD}}+0.5 \mathrm{~V}$ |
| Ground current ${ }^{3}$ | 1.5 A |
| Continuous total power dissipation ${ }^{4}$ | 1200 mW |
| Operating temperature range | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| Storage temperature range | $-65^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Lead temperature $1.6 \mathrm{~mm}(1 / 16$ inch $)$ | $260^{\circ} \mathrm{C}$ |
| from case for 10 seconds |  |

## Notes:

1. Device will survive (but operation may not be specified or guaranteed) at these extremes.
2. All voltages are referenced to $\mathrm{V}_{\mathrm{SS}}$.
3. Duty cycle is limited by the total power dissipated in the package.
4. For operation above $25^{\circ} \mathrm{C}$ ambient derate linearly to $85^{\circ} \mathrm{C}$ at $20 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$.

## General Description

## Not recommended for new designs.

The HV66 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. This device has been designed for use as a driver circuit for LCD displays. It can also be used in any application requiring multiple output high-voltage current sourcing and sinking capabilities. The inputs are fully CMOS compatible.

The device consists of a 32-bit shift register, 32 latches, and control logic to perform blanking and polarity control of the outputs. HVout1 is connected to the first stage of the shift register. Data is shifted through the shift register on the logic rising transition of the clock. A DIR pin causes data shifting clockwise when grounded and counterclockwise when connected to $\mathrm{V}_{\mathrm{DD}}$. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the LE (latch enable), BL (blank) or the POL (polarity) inputs. Transfer of data from the shift register to the latch occurs when the LE (latch enable) input is high. The data in the latch is stored after LE transitions from high to low.

## 09/30/02

Electrical Characteristics (over recommended operating conditions unless noted)
DC Characteristics ( $\mathrm{V}_{\mathrm{DD}}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{PP}}=60 \mathrm{~V}, \mathrm{~V}_{\mathrm{SS}}=\mathrm{GND}$ )

| Symbol | Parameter |  | Min | Max | Units | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{DD}}$ | $\mathrm{V}_{\mathrm{DD}}$ supply current |  |  | 15 | mA | $\begin{aligned} & \mathrm{V}_{\mathrm{DD}}=\mathrm{V}_{\mathrm{DD}} \max \\ & \mathrm{f}_{\mathrm{CLK}}=5 \mathrm{MHz} \end{aligned}$ |
| $\mathrm{I}_{\mathrm{PPQ}}$ | High voltage supply current |  |  | 0.5 | mA | Outputs high |
|  |  |  |  | 0.5 | mA | Outputs low |
| $\mathrm{I}_{\text {DDQ }}$ | Quiescent $\mathrm{V}_{\text {DD }}$ supply current |  |  | 0.5 | mA | All $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {SS }}$ or $\mathrm{V}_{\text {DD }}$ |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output | Q | 50 |  | V | $\mathrm{I}_{0}=-5 \mathrm{~mA}, \mathrm{~V}_{\mathrm{PP}}=60 \mathrm{~V}$ |
|  |  | Data out | 4.6 |  | V | $\mathrm{I}_{\mathrm{o}}=-100 \mu \mathrm{~A}$ |
| $\mathrm{V}_{\text {OL }}$ | Low-level output | Q |  | 8 | V | $\mathrm{I}_{0}=5 \mathrm{~mA}, \mathrm{~V}_{\mathrm{PP}}=60 \mathrm{~V}$ |
|  |  | Data out |  | 0.4 | V | $\mathrm{I}_{\mathrm{O}}=100 \mu \mathrm{~A}$ |
| $\mathrm{I}_{\mathrm{H}}$ | High-level logic input current |  |  | 1 | $\mu \mathrm{A}$ | $\mathrm{V}_{1 H}=\mathrm{V}_{\mathrm{DD}}$ |
|  | Low-level logic input current |  |  | -1 | $\mu \mathrm{A}$ | $\mathrm{V}_{\text {IL }}=0 \mathrm{~V}$ |
| $\mathrm{V}_{\text {OLBP }}$ | Low-level output voltage, backplane |  |  | 3 | V | $\mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}$ |
| $\mathrm{V}_{\text {OHBP }}$ | High-level output voltage, backplane |  | 29 |  | V | $\mathrm{I}_{0}=-10 \mathrm{~mA}$ |

AC Characteristics $\left(\mathrm{V}_{\mathrm{DD}}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{PP}}=60 \mathrm{~V}, \mathrm{~T}_{\mathrm{C}}=25^{\circ} \mathrm{C}\right)$, logic input rises/fall time $=10 \mathrm{~ns}$.

| Symbol | Parameter | Min | Max | Units | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{f}_{\mathrm{CLK}}$ | Clock frequency |  | 5 | MHz |  |
| $t_{\text {w }}$ | Clock width high or low | 100 |  | ns |  |
| $t_{S U}$ | Data set-up time before clock rises | 25 |  | ns |  |
| $\mathrm{t}_{\mathrm{H}}$ | Data hold time after clock rises | 50 |  | ns |  |
| $\mathrm{t}_{\text {ON }}, \mathrm{t}_{\text {OFF }}$ | Time from latch enable or POL to $\mathrm{HV}_{\text {OUT }}$ |  | 500 | ns | $\mathrm{C}_{\mathrm{L}}=20 \mathrm{pF}$ |
| $\mathrm{t}_{\text {ON }}, \mathrm{t}_{\text {OFF }}$ | Time from POL to BP output |  | 500 | ns | $\mathrm{C}_{\mathrm{L}}=20 \mathrm{pF}$ |
| $\mathrm{t}_{\mathrm{DHL}}$ | Delay time clock to data high to low |  | 200 | ns | $\mathrm{C}_{\mathrm{L}}=10 \mathrm{pF}$ |
| $\mathrm{t}_{\text {DLH }}$ | Delay time clock to data low to high |  | 200 | ns | $\mathrm{C}_{\mathrm{L}}=10 \mathrm{pF}$ |
| $\mathrm{t}_{\text {DLE }}$ | Delay time clock to LE low to high | 50 |  | ns |  |
| $\mathrm{t}_{\text {WLE }}$ | Width of LE pulse | 100 |  | ns |  |
| $\mathrm{t}_{\text {SLE }}$ | LE set-up time before clock rises | 50 |  | ns |  |
| $\mathrm{t}_{\mathrm{BR}}, \mathrm{t}_{\mathrm{BF}}$ | $\mathrm{BP}_{\text {OUT }}$ rise/fall time | 10 | 1000 | $\mu \mathrm{S}$ | $\mathrm{C}_{\mathrm{L}}=350 \mathrm{nF}$ |
| $\left\|t_{B R}-t_{B F}\right\|$ | $\mathrm{BP}_{\text {OUT }}$ rise and fall difference |  | 100 | $\mu \mathrm{s}$ | $\mathrm{C}_{\mathrm{L}}=350 \mathrm{nF}$ |

## Recommended Operating Conditions

| Symbol | Parameter | Min | Max | Units |
| :--- | :--- | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{DD}}$ | Logic supply voltage | 4.5 | 5.5 | V |
| $\mathrm{~V}_{\mathrm{PP}}$ | Output voltage $^{*}$ | 0 | 60 | V |
| $\mathrm{~V}_{\mathrm{IH}}$ | High-level input voltage | 2.4 | $\mathrm{~V}_{\mathrm{DD}}$ | V |
| $\mathrm{V}_{\mathrm{IL}}$ | Low-level input voltage | 0 | 0.8 | V |
| $\mathrm{f}_{\mathrm{CLK}}$ | Clock frequency | 0 | 5 | MHz |
| $\mathrm{T}_{\mathrm{A}}$ | Operating free-air temperature | -40 | +85 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\mathrm{OD}}$ | Allowable current through output diodes |  | 200 | mA |

Notes:
*Output will not switch below 12V.
Power-up sequence should be the following:

1. Connect ground.
2. Set all inputs (Data, CLK, Enable, etc.) to a known state.
3. Apply $V_{D D}$.
4. Apply $\mathrm{V}_{\mathrm{PP}}$.

Power-down sequence should be the reverse of the above.
The $\mathrm{V}_{\mathrm{PP}}$ should not drop below $\mathrm{V}_{\mathrm{DD}}$ during operation.

## Switching Waveforms



Functional Block Diagram


Function Table

| Function | Inputs |  |  |  |  |  | Outputs |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Data | CLK | LE | BL | POL | DIR | $\begin{aligned} & \text { Shift Reg } \\ & 1 \quad 2 \ldots . .32 \end{aligned}$ | $\begin{aligned} & \mathrm{H} \\ & 1 \end{aligned}$ | $\begin{array}{r} \text { Utputs } \\ 2 \ldots 32 \end{array}$ | $\begin{aligned} & \text { Data Out } \\ & 2 \ldots . .32 \end{aligned}$ | $\mathrm{BP}_{\star}{ }_{\text {out }}$ |
| Load S/R | H or L | $\uparrow$ | L | H | H | X | H or L *...* | * | *...* | * | H |
| Load latches | X | H or L | L | H | H | X | * *...* | * | *...* | * | H |
|  | X | H or L | L | H | L | X | * *...* | * | *...* | * | L |
| Transparent Mode | L | $\uparrow$ | H | H | H | X | L *...* | H | *...* | * | H |
|  | H | $\uparrow$ | H | H | H | X | H *...* | L | *...* | * | H |
|  | L | $\uparrow$ | H | H | L | X | L *...* | L | *...* | * | L |
|  | H | $\uparrow$ | H | H | L | X | H *...* | H | *...* | * | L |
| R/L Shift | X | $\uparrow$ | X | H | X | H | $\mathrm{Qn} \rightarrow \mathrm{Qn}+1$ | * | *...* | Q32 |  |
|  | X | $\uparrow$ | X | H | X | L | Qn $\rightarrow$ Qn-1 | * | *...* | Q1 |  |
| Blank <br> Control | X | X | X | L | L | X | * *...* | L | L...L | * | L |
|  | X | X | X | L | H | X | * *...* | H | H...H | * | H |

Notes:
$H=$ high level, $L=$ low level, $X=$ irrelevant, $\uparrow=$ low-to-high transition.
${ }^{*}=$ dependent on previous stage's state before the last CLK or last LE high.

## Pin Configuration

## HV66

44 Pin Plastic Gullwing (QFP) Package

| Pin | Function | Pin | Function |
| :---: | :---: | :---: | :---: |
| 1 | HV ${ }_{\text {OUT }} 22 / 11$ | 23 | Data Out |
| 2 | HV ${ }_{\text {OUT }} 21 / 12$ | 24 | GND |
| 3 | HV ${ }_{\text {OUT }} 20 / 13$ | 25 | N/C |
| 4 | HV ${ }_{\text {OUT }} 19 / 14$ | 26 | BL |
| 5 | HV ${ }_{\text {OUT }} 18 / 15$ | 27 | POL |
| 6 | $\mathrm{HV}_{\text {OUT }} 17 / 16$ | 28 | LE |
| 7 | HV ${ }_{\text {OUT }} 16 / 17$ | 29 | $V_{\text {D }}$ |
| 8 | HV ${ }_{\text {OUT }} 15 / 18$ | 30 | Clock |
| 9 | HV ${ }_{\text {OUT }} 14 / 19$ | 31 | DIR |
| 10 | HV ${ }_{\text {OUT }} 13 / 20$ | 32 | Data In |
| 11 | HV ${ }_{\text {OUT }} 12 / 21$ | 33 | $V_{\text {PP }}$ |
| 12 | HV ${ }_{\text {OUT }} 11 / 22$ | 34 | BP Out |
| 13 | HV ${ }_{\text {OUT }} 10 / 23$ | 35 | $\mathrm{HV}_{\text {Out }} 32 / 1$ |
| 14 | $\mathrm{HV}_{\text {OUT }} 9 / 24$ | 36 | $\mathrm{HV}_{\text {OUT }} 31 / 2$ |
| 15 | $\mathrm{HV}_{\text {OUT }} 8 / 25$ | 37 | $\mathrm{HV}_{\text {Out }} 30 / 3$ |
| 16 | $\mathrm{HV}_{\text {OUT }} 7 / 26$ | 38 | $\mathrm{HV}_{\text {Out }} 29 / 4$ |
| 17 | HV ${ }_{\text {OUT }} 6 / 27$ | 39 | $\mathrm{HV}_{\text {OUT }} 28 / 5$ |
| 18 | $\mathrm{HV}_{\text {OUT }} 5 / 28$ | 40 | $\mathrm{HV}_{\text {OUT }} 27 / 6$ |
| 19 | $\mathrm{HV}_{\text {OUT }} 4 / 29$ | 41 | $\mathrm{HV}_{\text {Out }} 26 / 7$ |
| 20 | $\mathrm{HV}_{\text {OUT }} 3 / 30$ | 42 | $\mathrm{HV}_{\text {OUT }} 25 / 8$ |
| 21 | $\mathrm{HV}_{\text {OUT }} \mathbf{2 / 3 1}$ | 43 | $\mathrm{HV}_{\text {OUT }} 24 / 9$ |
| 22 | $\mathrm{HV}_{\text {OUT }}{ }^{1 / 32}$ | 44 | $\mathrm{HV}_{\text {Out }} 23 / 10$ |

Note:
Pin designation for DIR $=\mathrm{L} / \mathrm{H}$
Example:for DIR $=\mathrm{L}$, Pin 1 is $\mathrm{HV}_{\text {OUT }} 22$ for $\operatorname{DIR}=\mathrm{H}$, Pin 1 is $\mathrm{HV}_{\text {OUT }} 11$

Package Outline


## Pin Configuration

Package Outline

| HV66 |  |  |  |
| :---: | :---: | :---: | :---: |
| 44 Pin J-Lead Package |  |  |  |
| Pin | Function | Pin | Function |
| 1 | HV ${ }_{\text {OUT }} 17 / 16$ | 23 | LE |
| 2 | HV ${ }_{\text {OUT }} 16 / 17$ | 24 | $V_{\text {D }}$ |
| 3 | HV ${ }_{\text {OUt }} 15 / 18$ | 25 | Clock |
| 4 | HV ${ }_{\text {OUt }} 14 / 19$ | 26 | DIR |
| 5 | HV ${ }_{\text {OUt }} 13 / 20$ | 27 | Data In |
| 6 | HV ${ }_{\text {OUt }} 12 / 21$ | 28 | $V_{\text {PP }}$ |
| 7 | HV ${ }_{\text {OUt }} 11 / 22$ | 29 | BP Out |
| 8 | HV ${ }_{\text {OUt }} 10 / 23$ | 30 | HV ${ }_{\text {OUt }} 32 / 1$ |
| 9 | HV ${ }_{\text {OUT }} 9 / 24$ | 31 | HV ${ }_{\text {Out }} 31 / 2$ |
| 10 | HV ${ }_{\text {OUT }} 8 / 25$ | 32 | HV ${ }_{\text {OUT }} 30 / 3$ |
| 11 | $\mathrm{HV}_{\text {OUT }} 7 / 26$ | 33 | HV ${ }_{\text {OUT }} 29 / 4$ |
| 12 | HV ${ }_{\text {OUT }} 6 / 27$ | 34 | HV ${ }_{\text {OUT }} 28 / 5$ |
| 13 | HV ${ }_{\text {OUT }} 5 / 28$ | 35 | HV ${ }_{\text {OUT }} 27 / 6$ |
| 14 | HV ${ }_{\text {OUT }} 4 / 29$ | 36 | HV ${ }_{\text {OUT }} 26 / 7$ |
| 15 | HV ${ }_{\text {OUT }} 3 / 30$ | 37 | HV ${ }_{\text {OUT }} 25 / 8$ |
| 16 | HV ${ }_{\text {OUT }}$ 2/31 | 38 | HV ${ }_{\text {OUT }} 24 / 9$ |
| 17 | HV ${ }_{\text {OUT }} 1 / 32$ | 39 | HV ${ }_{\text {OUT }} 23 / 10$ |
| 18 | Data Out | 40 | HV OUT $22 / 11$ |
| 19 | GND | 41 | HV ${ }_{\text {OUT }} 21 / 12$ |
| 20 | N/C | 42 | HV ${ }_{\text {OUT }} 20 / 13$ |
| 21 | BL | 43 | HV OUt 19/14 |
| 22 | POL | 44 | HV ${ }_{\text {OUT }} 18 / 15$ |

Note:

1. Pin designation for $\operatorname{DIR}=\mathrm{L} / \mathrm{H}$

Example: for DIR $=$ L, Pin $1=$ HV $_{\text {OUT }} 17$ for DIR $=\mathrm{H}$, Pin $1=$ HV $_{\text {OUT }} 16$

