

**480MHz, SOT-23, Video Buffer with Output Disable**

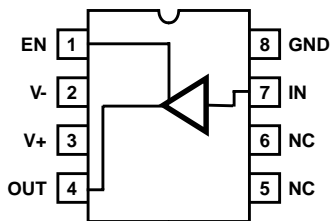
The HA4600 is a very wide bandwidth, unity gain buffer ideal for professional video switching, HDTV, computer monitor routing, and other high performance applications. The circuit features very low power dissipation (105mW Enabled, 1mW Disabled), excellent differential gain and phase, and very high off isolation. When disabled, the output is switched to a high impedance state, making the HA4600 ideal for routing matrix equipment and video multiplexers.

The HA4600 also features fast switching and symmetric slew rates. A typical application for the HA4600 is interfacing Intersil's wide range of video crosspoint switches.

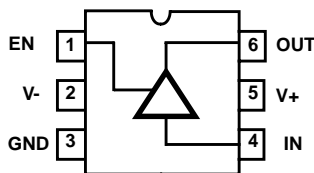
For applications requiring a tally output (enable indicator), please refer to the HA4201 data sheet.

**Pinouts**

**HA4600  
(PDIP, SOIC)  
TOP VIEW**



**HA4600  
(SOT-23)  
TOP VIEW**



**Features**

- Micro Package Available . . . . . SOT-23
- Low Power Dissipation . . . . . 105mW
- Symmetrical Slew Rates . . . . . 1700V/μs
- 0.1dB Gain Flatness . . . . . 250MHz
- Off Isolation (100MHz) . . . . . 85dB
- Differential Gain and Phase . . . . . 0.01%/0.01 Degrees
- High ESD Rating . . . . . >1800V
- TTL Compatible Enable Input
- Improved Replacement for GB4600

**Applications**

- Professional Video Switching and Routing
- Video Multiplexers
- HDTV
- Computer Graphics
- RF Switching and Routing
- PCM Data Routing

**Ordering Information**

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA4600CP	0 to 70	8 Ld PDIP	E8.3
HA4600CB (H4600CB)	0 to 70	8 Ld SOIC	M8.15
HA4600CB96 (H4600CB)	0 to 70	8 Ld SOIC Tape and Reel	M8.15
HA4600CH96 (4600)	0 to 70	6 Ld SOT-23 Tape and Reel	P6.064

**Truth Table**

EN	OUT
0	High Z
1	Active

## Absolute Maximum Ratings

Voltage Between V+ and V- . . . . .	12V
Input Voltage . . . . .	V <sub>SUPPLY</sub>
Digital Input Current (Note 2) . . . . .	±25mA
Output Current . . . . .	20mA
ESD Rating	
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . .	1800V

## Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (°C/W)
PDIP Package . . . . .	130
SOIC Package . . . . .	170
SOT-23 Package . . . . .	210
Maximum Junction Temperature (Die) . . . . .	175°C
Maximum Junction Temperature (Plastic Package) . . . . .	150°C
Maximum Storage Temperature Range . . . . .	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . .	300°C
(SOIC and SOT-23 - Lead Tips Only)	

## Operating Conditions

Temperature Range . . . . .	0°C to 70°C
-----------------------------	-------------

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTES:

1.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.
2. If an input signal is applied before the supplies are powered up, the input current must be limited to this maximum value.

## Electrical Specifications V<sub>SUPPLY</sub> = ±5V, R<sub>L</sub> = 10k $\Omega$ , V<sub>EN</sub> = 2.0V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
<b>DC SUPPLY CHARACTERISTICS</b>						
Supply Voltage		Full	±4.5	±5.0	±5.5	V
Supply Current (V <sub>OUT</sub> = 0V)	V <sub>EN</sub> = 2V	25, 70	-	10.5	13	mA
	V <sub>EN</sub> = 2V	0	-	-	14.5	mA
	V <sub>EN</sub> = 0.8V	25, 70	-	100	115	μA
	V <sub>EN</sub> = 0.8V	0	-	100	125	μA
<b>ANALOG DC CHARACTERISTICS</b>						
Output Voltage Swing without Clipping	V <sub>OUT</sub> = V <sub>IN</sub> ± V <sub>IO</sub> ± 20mV	25, 70	±2.7	±2.8	-	V
		0	±2.4	±2.5	-	V
Output Current		Full	15	20	-	mA
Input Bias Current		Full	-	30	50	μA
Output Offset Voltage		25	-10	-	10	mV
Output Offset Voltage Drift (Note 3)		Full	-	25	50	μV/°C
<b>SWITCHING CHARACTERISTICS</b>						
Turn-On Time		25	-	160	-	ns
Turn-Off Time		25	-	320	-	ns
<b>DIGITAL DC CHARACTERISTICS</b>						
Input Logic High Voltage		Full	2	-	-	V
Input Logic Low Voltage		Full	-	-	0.8	V
EN Input Current	0V to 4V	Full	-2	-	2	μA
<b>AC CHARACTERISTICS</b>						
Insertion Loss	1V <sub>P-P</sub>	Full	-	0.04	0.05	dB
-3dB Bandwidth	R <sub>S</sub> = 82 $\Omega$ , C <sub>L</sub> = 10pF	25	-	480	-	MHz
	R <sub>S</sub> = 43 $\Omega$ , C <sub>L</sub> = 15pF	25	-	380	-	MHz
	R <sub>S</sub> = 36 $\Omega$ , C <sub>L</sub> = 21pF	25	-	370	-	MHz

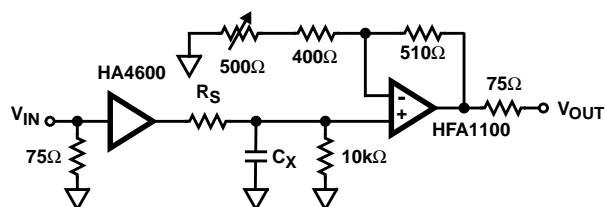
## Electrical Specifications $V_{SUPPLY} = \pm 5V$ , $R_L = 10k\Omega$ , $V_{EN} = 2.0V$ , Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
$\pm 0.1$ dB Flat Bandwidth	$R_S = 82\Omega$ , $C_L = 10$ pF	25	-	250	-	MHz
	$R_S = 43\Omega$ , $C_L = 15$ pF	25	-	175	-	MHz
	$R_S = 36\Omega$ , $C_L = 21$ pF	25	-	170	-	MHz
Input Resistance		Full	200	400	-	k $\Omega$
Input Capacitance		Full	-	1.0	-	pF
Enabled Output Resistance		Full	-	15	-	$\Omega$
Disabled Output Capacitance	$V_{EN} = 0.8V$	Full	-	2.0	-	pF
Differential Gain (Note 3)	4.43MHz	25	-	0.01	0.02	%
Differential Phase (Note 3)	4.43MHz	25	-	0.01	0.02	Degrees
Off Isolation	1V <sub>P-P</sub> , 100MHz, $V_{EN} = 0.8V$ , $R_L = 10\Omega$	Full	-	85	-	dB
Slew Rate (1.5V <sub>P-P</sub> , +SR/-SR)	$R_S = 82\Omega$ , $C_L = 10$ pF	25	-	1750/1770	-	V/ $\mu$ s
	$R_S = 43\Omega$ , $C_L = 15$ pF	25	-	1460/1360	-	V/ $\mu$ s
	$R_S = 36\Omega$ , $C_L = 21$ pF	25	-	1410/1360	-	V/ $\mu$ s
Total Harmonic Distortion (Note 3)		Full	-	0.01	0.1	%
Disabled Output Resistance		Full	-	12	-	M $\Omega$

NOTE:

- This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.

## AC Test Circuit



NOTE:  $C_L = C_X + \text{Test Fixture Capacitance}$ .

## PC Board Layout

The frequency response of this circuit depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10 $\mu$ F) tantalum in parallel with a small value (0.1 $\mu$ F) chip capacitor works well in most cases.

Keep input and output traces as short as possible, because trace inductance and capacitance can easily become the performance limiting items.

## Application Information

### General

The HA4600 is a unity gain buffer that is optimized for high performance video applications. The output disable function makes it ideal for the matrix element in small, high input-to-output isolation switchers and routers. This buffer contains no feedback or gain setting resistors, so the output is a true high impedance load when the IC is disabled ( $EN = 0$ ). The HA4600 also excels as an input buffer for routers with a large number of outputs (i.e. each input must connect to a large number of outputs) and delivers performance superior to most video amplifiers at a fraction of the cost. As an input buffer, the HA4600's low input capacitance and high input resistance provide excellent video terminations when used with an external 75 $\Omega$  resistor.

### Frequency Response

Most applications utilizing the HA4600 require a series output resistor,  $R_S$ , to tune the response for the specific load capacitance,  $C_L$ , driven. Bandwidth and slew rate degrade as  $C_L$  increases (as shown in the Electrical Specification table), so give careful consideration to component placement to minimize trace length. As an example, -3dB bandwidth decreases to 160MHz for  $C_L = 100$ pF,  $R_S = 0\Omega$ . In big matrix configurations where  $C_L$  is large, better

frequency response is obtained by cascading two levels of crosspoints in the case of multiplexed outputs (see Figure 2), or distributing the load between two drivers if  $C_L$  is due to bussing and subsequent stage input capacitance.

**Control Signals**

EN - The ENABLE input is a TTL/CMOS compatible, active high input. When driven low this input forces the output to a true high impedance state and reduces the power dissipation by two orders of magnitude. The EN input has no on-chip pull-up resistor, so it must be connected to a logic high (recommend V+) if the enable function isn't utilized.

**Switcher/Router Applications**

Figure 1 illustrates one possible implementation of a wideband, low power, 4 x 4 switcher/router. A 4 x 4 switcher/router allows any of the four outputs to be driven by any one of the four inputs (e.g. each of the four inputs may connect to a different output, or an input may connect to multiple outputs). This application utilizes the HA4600 for the input buffer, the HA4404 (4 x 1 crosspoint switch) as the switch matrix, and the HFA1112 (programmable gain buffer) as the gain of two output driver. Figure 2 details a 16 x 1 switcher (basically a 16:1 MUX) which uses the HA4600 in a cascaded stage configuration to minimize capacitive loading at each output node, thus increasing system bandwidth.

**Power Up Considerations**

No signals should be applied to the analog or digital inputs before the power supplies are activated. Latch-up may occur if the inputs are driven at the time of power up. To prevent latch-up, the input currents during power up must not exceed the values listed in the Absolute Maximum Ratings.

**Intersil's Crosspoint Family**

Intersil offers a variety of 1 x 1 and 4 x 1 crosspoint switches. In addition to the HA4600, the 1 x 1 family includes the HA4201 which is an essentially similar device that includes a Tally output (enable indicator). The 4 x 1 family is comprised of the HA4314, HA4404, and HA4344. The HA4314 is a 14 lead basic 4 x 1 crosspoint. The HA4404 is a 16 lead device with Tally outputs to indicate the selected channel. The HA4344 is a 16 lead crosspoint with synchronized control lines (A0, A1, CS). With synchronization, the control information for the next channel switch can be loaded into the crosspoint without affecting the current state. On a subsequent clock edge the stored control state effects the desired channel switch.

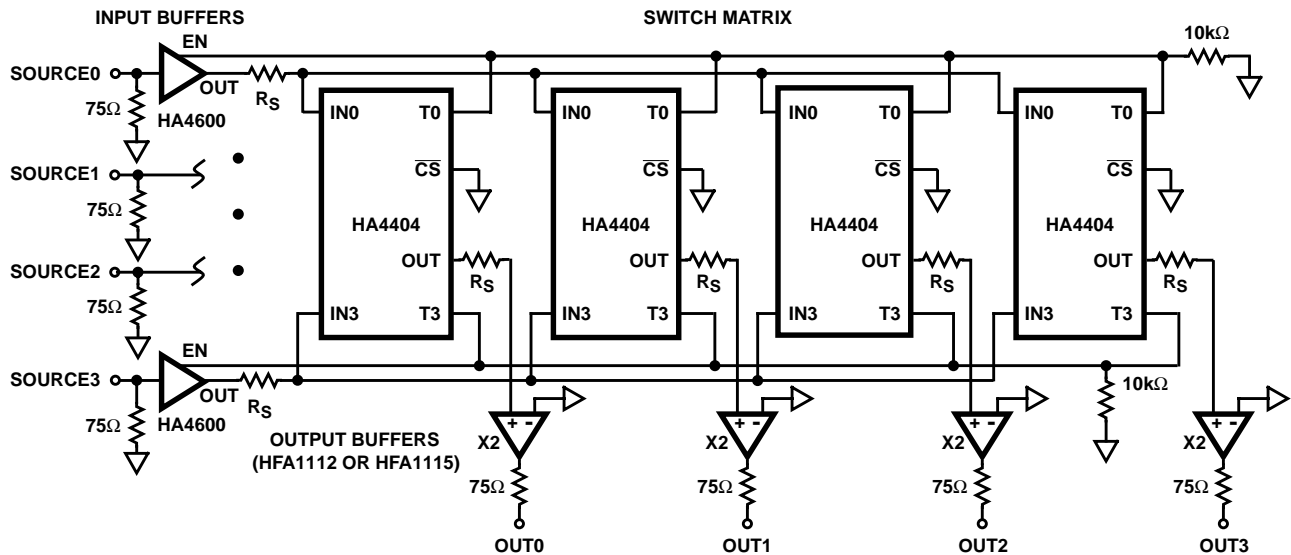


FIGURE 1. 4 x 4 SWITCHER/ROUTER APPLICATION

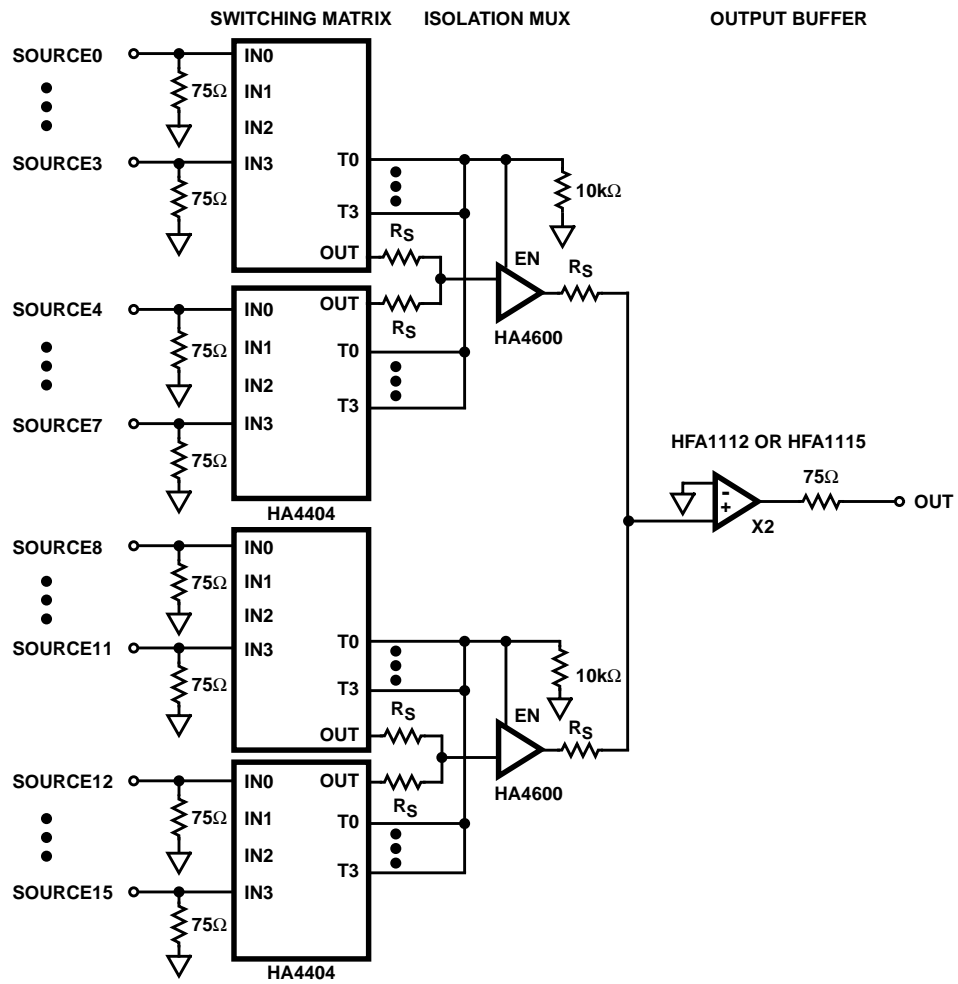


FIGURE 2. 16 x 1 SWITCHER APPLICATION

**Typical Performance Curves**  $V_{SUPPLY} = \pm 5V$ ,  $T_A = 25^\circ C$ ,  $R_L = 10k\Omega$ , Unless Otherwise Specified

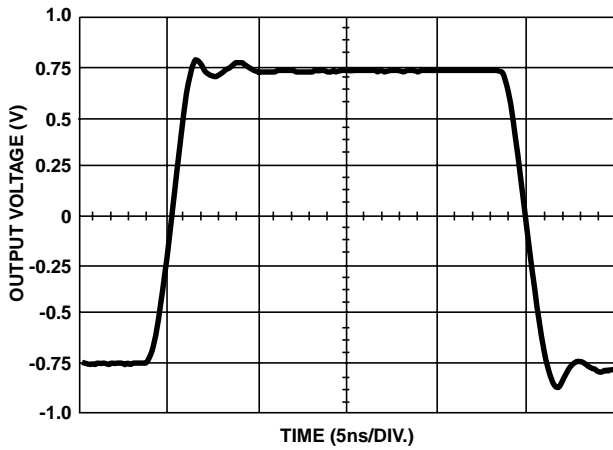


FIGURE 3. LARGE SIGNAL PULSE RESPONSE

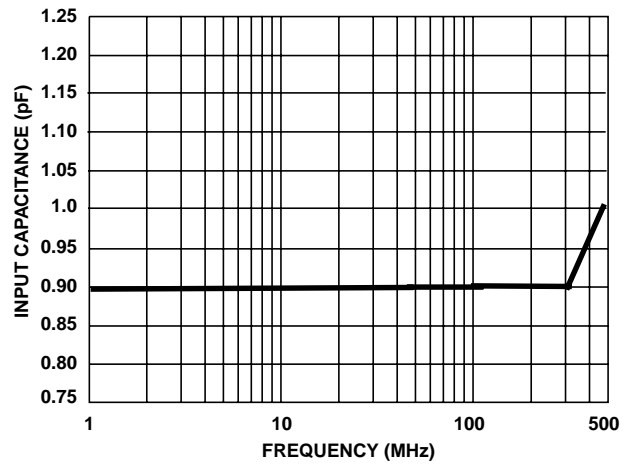


FIGURE 4. INPUT CAPACITANCE vs FREQUENCY

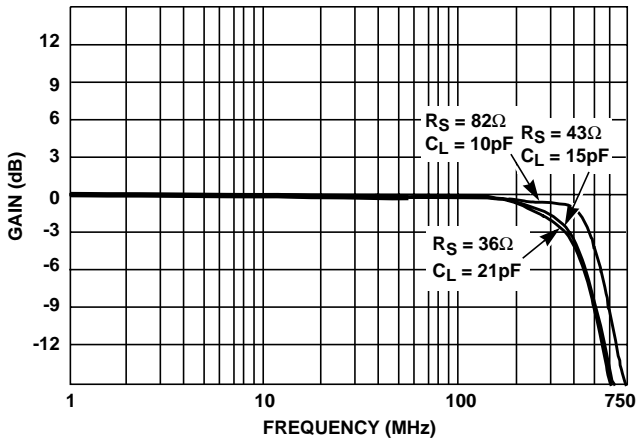


FIGURE 5. FREQUENCY RESPONSE

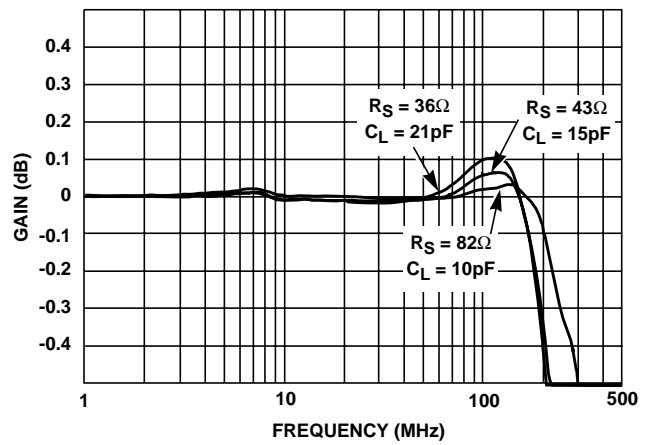


FIGURE 6. GAIN FLATNESS

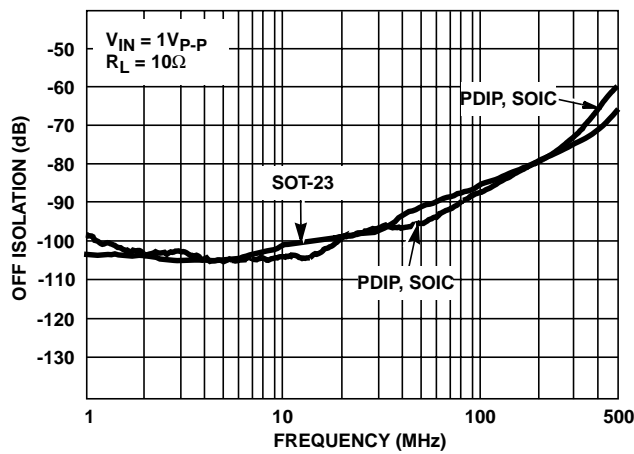


FIGURE 7. OFF ISOLATION

**Die Characteristics**

**DIE DIMENSIONS:**

51 mils x 36 mils x 19 mils  
 1290µm x 910µm x 483µm

**METALLIZATION:**

Type: Metal 1: AlCu (1%)/TiW  
 Thickness: Metal 1: 6kÅ ±0.8kÅ  
 Type: Metal 2: AlCu (1%)  
 Thickness: Metal 2: 16kÅ ±1.1kÅ

**SUBSTRATE POTENTIAL (Powered Up):**

V-

**PASSIVATION:**

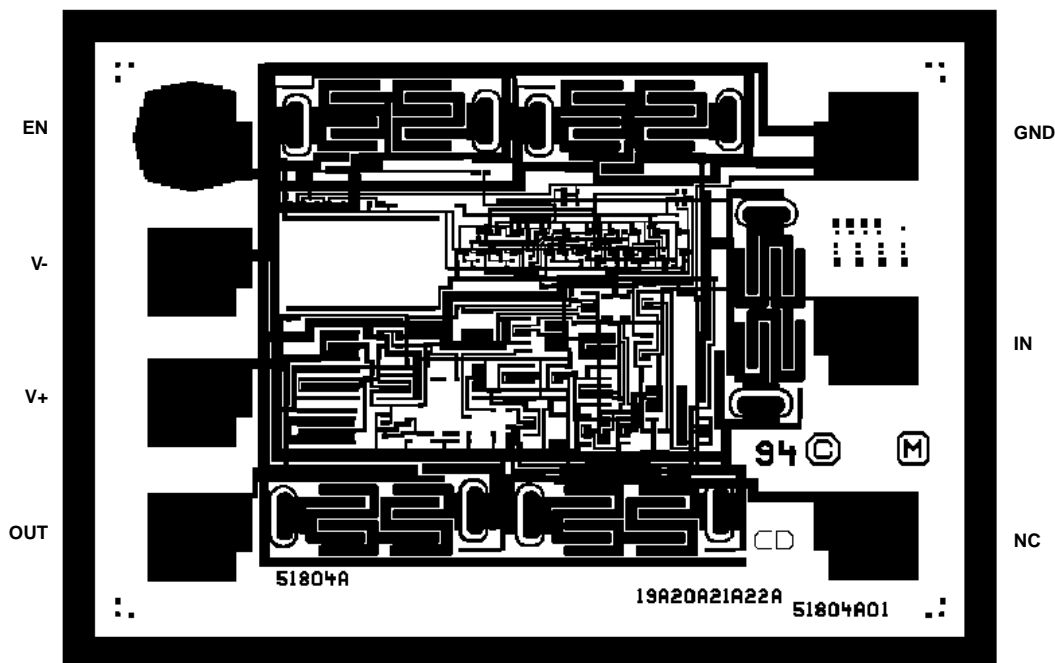
Type: Nitride  
 Thickness: 4kÅ ±0.5kÅ

**TRANSISTOR COUNT:**

53

**Metallization Mask Layout**

HA4600



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

*Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>