FUSB301A

Autonomous USB Type-C Controller with Configurable I²C Address

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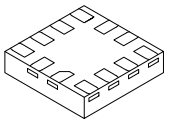


Bottom View

X2QFN12 1.6x1.6, 0.4P
CASE 722AD

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Description

The FUSB301A is a fully autonomous Type-C controller optimized for < 15 W applications. The FUSB301A offers CC logic detection for Source Mode, Sink Mode, DRP, accessory detection support, and dead battery support. The FUSB301A features configurable I²C address to support multiple ports per system. The FUSB301A features an extremely low power disable mode as well as low power during normal operation. It is available in an ultra thin, 12-Lead TMLP Package.

Features

- Fully Autonomous Type−C Controller Supports Type−C Versions 1.1 and 1.0
- V_{DD} Operating Range, 3.0 V – 5.5 V
- Low Disable Power: I_{CC} = 2.0 μA (Max.)
- Low Standby Power: I_{CC} = 7.0 μA (Max.)
- DRP Mode with Optional Accessory Support
- Configurable I²C Address
- Capable of Supporting Try.SNK and Try.SRC
- Dead Battery Support (SINK Support when No Power Applied)
- 2 kV HBM ESD Protection
- Small Packaging, 12 Lead TMLP (1.6 mm × 1.6 mm × 0.375 mm)

Applications

- Smartphones
- Tablets
- Notebooks
- Ultra Portable Applications

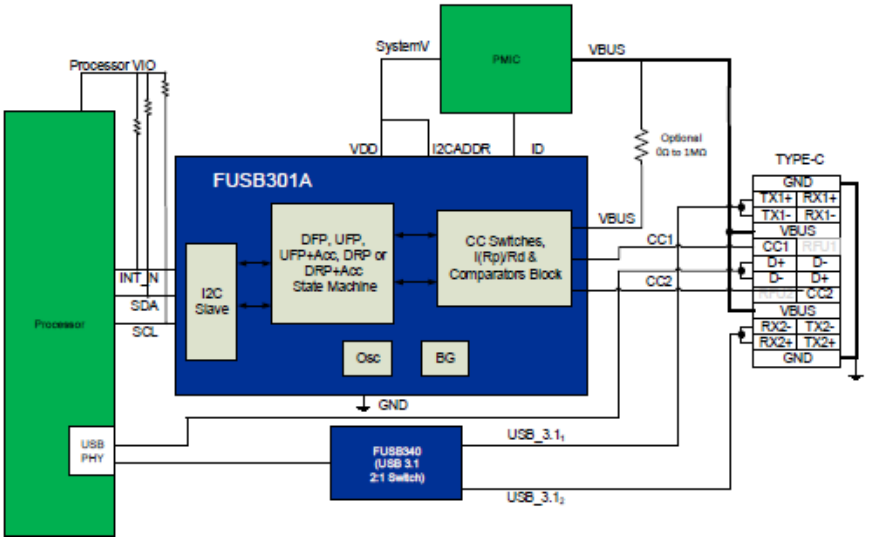


Figure 1. Typical Application

ORDERING INFORMATION

Part Number	Top Mark	Operating Temperature Range	Package	Packing Method†
FUSB301A	NX	−40 to 85°C	12−Lead Ultra−thin Molded Leadless Package (TMLP) 1.6 mm × 1.6 mm × 0.375 mm	Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

BLOCK DIAGRAM

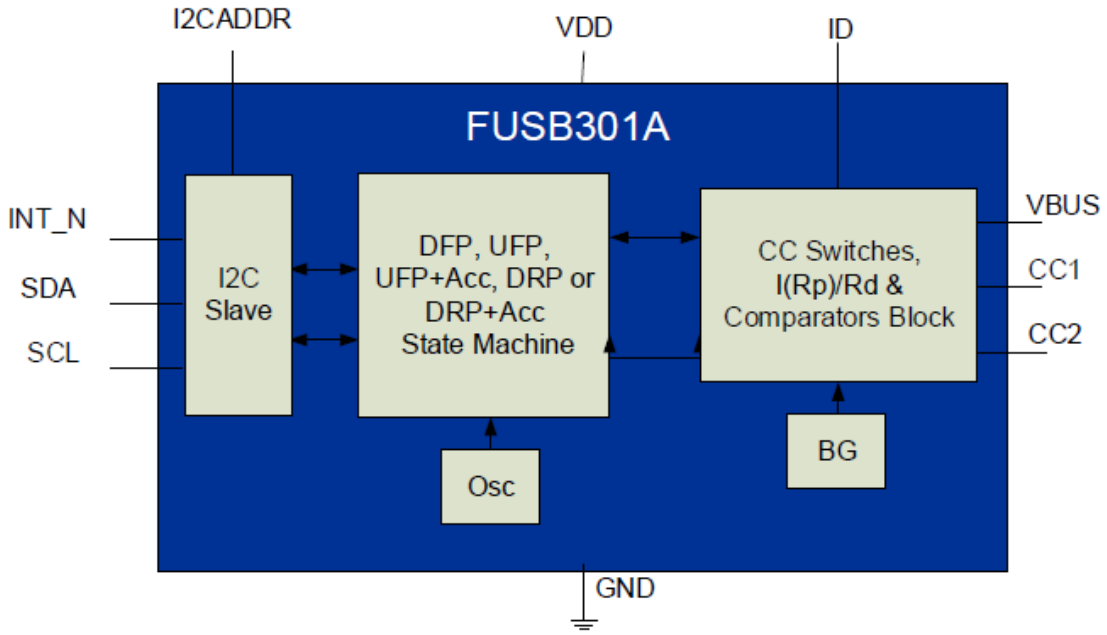


Figure 2. Block Diagram

PIN CONFIGURATION

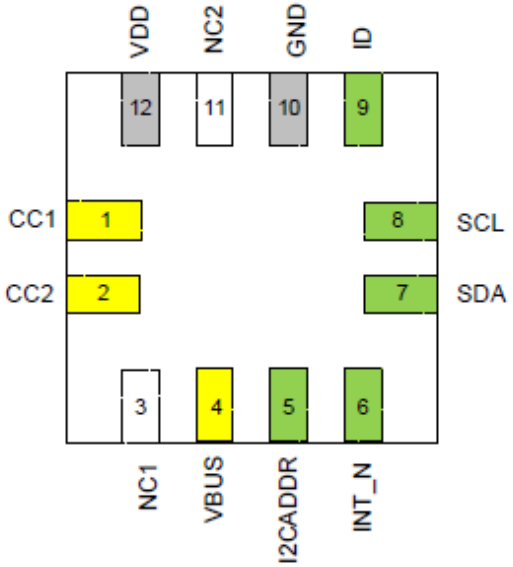


Figure 3. Pin Assignment (Top Through View)

PIN DESCRIPTIONS

Pin #	Name	Type	Description
USB Type−C Connector Interface			
1, 2	CC1, CC2	I/O	Type−C Configuration Channel
4	VBUS	Input	VBUS input pin for attach and detach detection
10	GND	Ground	Ground
Power Interface			
12	VDD	Power	Input Supply Voltage
Signal Interface			
8	SCL	Input	I^2C serial clock signal to be connected to the I^2C master
7	SDA	Open−Drain I/O	I^2C serial data signal to be connected to the I^2C master
6	INT_N	Open−Drain Output	Active LOW open drain interrupt output used to prompt the processor to read the I^2C register bits
9	ID	Open−Drain Output	Used to Identify if connected device is Source or Sink. The ID Pin can be used to interface with USB 2.0 Input on the processor.
5	I2CADDR	Input	Used to change bit 3 of the I2C address so that multiple addresses can be used in a system where two device addresses conflict
3	NC1	NC	No Connect − Tie to Ground or Float
11	NC2	NC	No Connect − Tie to Ground or Float

Dead Battery

If power is not applied to FUSB301A and it is attached to a Source device, then the Source would pull up the CC line connected through the cable. The FUSB301A in response would turn on the pull−down that will bring the CC voltage to a range that the Source can detect an attach and turn on VBUS.

Power Up, Initialization and Reset, Interrupt Operation

When power is first applied, the FUSB301A will power up in Sink mode with all interrupts masked. The local processor must configure the FUSB301A to the desired mode and clear the global interrupt mask bit, INT_MASK. The INT_N pin is an active low, open drain output. This pin indicates to the host processor that an interrupt has occurred in the FUSB301A which needs attention. The INT_N pin is in a high impedance state by default after power−up or device reset, and the global interrupt mask (INT_MASK in Control register) is set. After INT_MASK bit is cleared by the local processor, the INT_N pin stays high impedance in preparation of future interrupts. When an interruptible event occurs, INT_N is driven LOW and is in a high impedance state again when the processor clears the interrupt by reading the interrupt registers. Subsequent to the initial power up or reset; if the processor writes a “1” to global interrupt mask bit when the system is already powered up, the INT_N pin stays in a high impedance state and ignores all interrupts until the global interrupt mask bit is cleared. If an event happens that would ordinarily cause an interrupt when the global interrupt mask bit is set, the INT_N pin goes LOW when the global interrupt mask is cleared.

Table 1. ID PIN TRUTH TABLE

Type Register (h12, bit 4)	Description	ID
SINK = b0	SINK Not Detected	Hi−Z (default)
SINK = b1	SINK Detected	Low

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage from V_{DD}	−0.5	6.0	V
V_{BUS}	VBUS Supply Voltage	−0.5	28	V
V_{CC_HDDRP}	CC pins when configured as Host, Device or Dual Role Port	−0.5	6.0	V
$T_{STORAGE}$	Storage Temperature Range	−65	+150	°C

ABSOLUTE MAXIMUM RATINGS (continued)

Symbol	Parameter			Min.	Max.	Unit
T_J	Maximum Junction Temperature				+150	°C
T_L	Lead Temperature (Soldering, 10 seconds)				+260	°C
ESD	IEC 6100−4−2 System ESD	Connector Pins (VBUS, CC1 and CC2)	Air Gap	15		kV
			Contact	8		
	Human Body Model, JEDEC JESD22−A114	Connector Pins (VBUS, CC1 and CC2)		4		
		Others		2		
	Charged Device Model, JEDEC LESD22−C101	All Pins		1		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERAING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{BUS}	VBUS Supply Voltage	3.7	5.0	21	V
V_{DD}	Supply Voltage	2.8 (1)	3.3	5.5	V
T_A	Operating Temperature	−40		+85	°C

1. This is for functional operation only and isn't the lowest limit for all subsequent electrical specifications below. All electrical parameters have a minimum of 3 V operation.

DC AND TRANSIENT CHARACTERISTICS

Unless otherwise specified: Recommended T_A and T_J temperature ranges. All typical values are at T_A = 25°C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	T_A = −40 to +85°C T_J = −40 to +125°C			Unit
		Min.	Typ.	Max.	
Type C Specific Parameters					
I_{80_CCX}	Source 80 μA CC Current (Default) HOST_CUR1 = 0, HOST_CUR0 = 1	64	80	96	μA
I_{180_CCX}	Source 180 μA CC Current (1.5 A) HOST_CUR1 = 1, HOST_CUR0 = 0	166	180	194	μA
I_{330_CCX}	Source 330 μA CC Current (3 A) HOST_CUR1 = 1, HOST_CUR0 = 1	304	330	356	μA
V_{SNKDB}	Sink Pull−Down Voltage in Dead Battery Under all Pull−up SOURCE Loads			2.18	V
R_{DEVICE}	Sink Pull−Down Resistance when V_{DD} is within Operating Range	4.6	5.1	5.6	kΩ
zOPEN	CC Resistance for Disabled State	126			kΩ
vRa−SRCdef	Ra Detection Threshold for CC Pin for Source for Default Current on VBUS	0.15	0.20	0.25	V
vRa−SRC1.5A	Ra Detection Threshold for CC Pin for Source for 1.5 A Current on VBUS	0.35	0.40	0.45	V
vRa−SRC3A	Ra Detection Threshold for CC Pin for Source for 3 A Current on VBUS	0.75	0.80	0.85	V
vRd−SRCdef	Rd Detection Threshold for Source for Default Current (HOST_CUR1/0 = 01)	1.50	1.60	1.65	V
vRd−SRC1.5A	Rd Detection Threshold for Source for 1.5 A Current (HOST_CUR1/0 = 10)	1.50	1.60	1.65	V

DC AND TRANSIENT CHARACTERISTICS

Unless otherwise specified: Recommended T_A and T_J temperature ranges. All typical values are at T_A = 25°C and V_{DD} = 3.3 V unless otherwise specified. (continued)

Symbol	Parameter	T_A = −40 to +85°C, T_J = −40 to +125°C			Unit
		Min.	Typ.	Max.	
vRd−SRC3A	Rd Detection Threshold for Source for 3 A Current (HOST_CUR1/0 = 11)	2.45	2.60	2.75	V
vRa−SNK	Ra Detection Threshold for CC Pin for Sink	0.15	0.20	0.25	V
vRd−def	Rd Default Current Detection Threshold for Sink	0.61	0.66	0.70	V
vRd−1.5A	Rd 1.5 A Current Detection Threshold for Sink	1.16	1.23	1.31	V
vRd−3.0A	Rd 3 A Current Detection Threshold for Sink	2.04	2.11	2.18	V
vVBUSthr	VBUS Threshold at which I_VBUSOK Interrupt is Triggered			3.7	V

CURRENT CONSUMPTION

Symbol	Parameter	V_{DD} (V)	Conditions	T_A = −40 to +85°C, T_J = −40 to +125°C			Unit
				Min.	Typ.	Max.	Unit
Idisable	Disabled Current	3.0 to 5.5	Disabled State		0.35	2.0	μA
Istby	Unattached Sink	3.0 to 5.5	Nothing attached		3.5	7.0	μA
	Unattached Sink + Acc, Source + Acc, or DRP		Nothing attached, Internally Toggling		5	20	μA
Iattach	Attach Current (Less Host Current)	3.0 to 5.5	Attached as a Sink		5	15	μA
			Attached as a Source		10	15	μA

TIMING PARAMETERS

Symbol	Parameter		T_A = −40 to +85°C, T_J = −40 to +125°C			Unit
			Min.	Typ.	Max.	Unit
tCCDebounce	Debounce Time for CC (Source or Accessory)		100	150	200	ms
	Debounce Time for CC (Sink)		63	75	87	ms
tPDDebounce	Debounce Time for CC Detach Detection		10	15	20	ms
tAccDetect	Debounce Time to Detect AudioAccessory, or DebugAccessory is Attached		50	100	200	ms
tErrorRecovery	Time staying in the ErrorRecovery State if sent there via the ERROR_REC bit or by a change of Modes		25	50	100	ms
tVBUSondeb	Debounce Time of VBUS Detection when acting as a Sink to Signal VBUS is present		0.167	0.200	0.375	ms
tVBUSoffdeb	Debounce Time of VBUS Detection when acting as a Sink to Signal VBUS has been removed		10	15	20	ms
tDRPToggle1	For DRP Operation, Time Spent in Unattached.Sink before going to Unattached.Source State	DRPROGGLE = 00	35		70	ms
		DRPROGGLE = 01	30		60	
		DRPROGGLE = 10	25		50	
		DRPROGGLE = 11	20		40	

TIMING PARAMETERS

Symbol	Parameter		T_A = −40 to +85°C, T_J = −40 to +125°C Min.	Typ.	Max.	Unit
tDRPToggle2	For DRP Operation, Time Spent in Unattached.Source before going to Unattached.Sink State	DRPROGGLE = 00	15		30	ms
		DRPROGGLE = 01	20		40	
		DRPROGGLE = 10	25		50	
		DRPROGGLE = 11	30		60	

IO SPECIFICATIONS

Symbol	Parameter	V_{DD} (V)	Conditions	T_A = −40 to +85°C, T_J = −40 to +125°C Min.	Typ.	Max.	Unit
Host Interface Pins (ID)							
V_{OLID}	Output Low Voltage	3.0 to 5.5	I_{OL} = 4 mA			0.4	V
Host Interface Pins (I2CADDR)							
V_{ILADDR}	Low−Level Input Voltage	3.0 to 5.5				$0.3V_{DD}$	V
V_{IHADDR}	High−Level Input Voltage	3.0 to 5.5		$0.7V_{DD}$			V
Host Interface Pins (INT_N)							
V_{OLINTN}	Output Low Voltage	3.0 to 5.5	I_{OL} = 4 mA			0.4	V
I^2C Interface Pins − Fast Mode SDA, SCL							
V_{ILI2C}	Low−Level Input Voltage	3.0 to 5.5				0.4	V
V_{IHI2C}	High−Level Input Voltage	3.0 to 5.5		1.2			V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	3.0 to 5.5		0.2			V
I_{I2C}	Input Current of SDA and SCL Pins	3.0 to 5.5	Input Voltage 0.26 V to 2 V	−10		10	μA
I_{CCTI2C}	VDD Current when SDA and SCL are HIGH	3.0 to 5.5	Input Voltage 1.8 V			10	μA
V_{OLSDA}	Low−Level Output Voltage at 3 mA Sink Current (Open−Drain)	3.0 to 5.5		0		0.3	V
C_I	Capacitance for Each I/O Pin (2)	3.0 to 5.5				10	pF

2. Guaranteed by characterization. Not production tested.

FAST MODE I^2C SPECIFICATIONS (Note 3) (see Figure 4)

Symbol	Parameter		Fast Mode Min.	Max.	Unit
f_{SCL}	I2C_SCL Clock Frequency		0	400	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition		0.6		μs
t_{LOW}	LOW Period of I2C_SCL Clock		1.3		μs
t_{HIGH}	HIGH Period of I2C_SCL Clock		0.6		μs
$t_{SU;STA}$	Set−up Time for Repeated START Condition		0.6		μs
$t_{HD;DAT}$	Data Hold Time		0	0.9	μs
$t_{SU;DAT}$	Data Set−up Time	(Note 4)	100		ns
t_r	Rise Time of I2C_SDA and I2C_SCL Signals	(Note 5)	$20*(V_{DD}/5.5V)$	250	ns
t_f	Fall Time of I2C_SDA and I2C_SCL Signals	(Note 5)	$20*(V_{DD}/5.5V)$	250	ns

FAST MODE I²C SPECIFICATIONS (Note 3)**(see Figure 4)** (continued)

Symbol	Parameter	Fast Mode		Unit
		Min.	Max.	
$t_{SU;STO}$	Set−up Time for STOP Condition	0.6		μs
t_{BUF}	BUS−Free Time between STOP and START Conditions	1.3		μs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns

3. Guaranteed by characterization. Not production tested.
4. A fast−mode I²C bus device can be used in a standard−mode I²C bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must be met. This is automatically the case of the device does not stretch the LOW period of the I2C_SCL signal. If such a device does stretch the LOW period I2C_SCL signal, it must output the next data bit to the I2C_SDA line tr_max + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard−mode I²C bus specification) before the I2C_SCL line is released.
5. Cb equals the total capacitance of one bus line in pF. If mixed with high−speed devices, faster fall times are allowed according to the I²C specification.

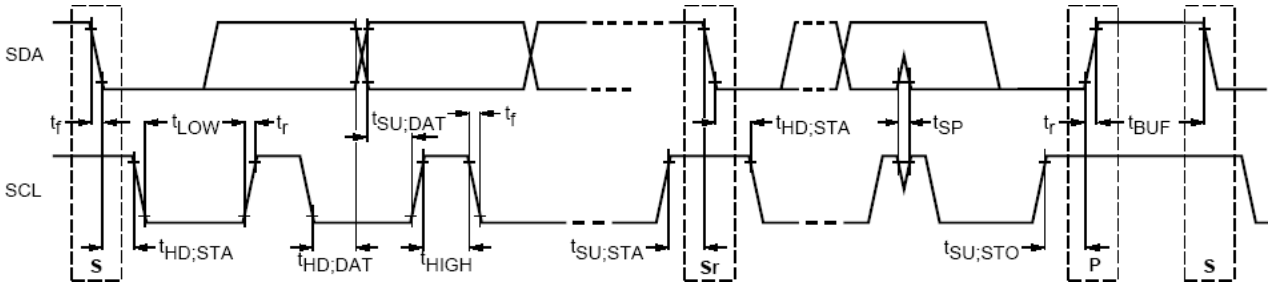
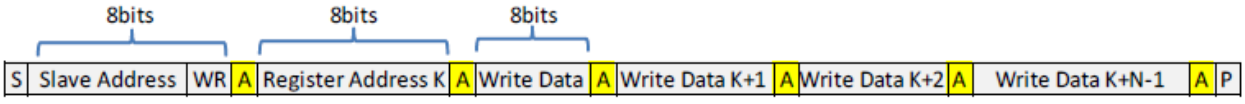


Figure 4. Definition of Timing for Full−Speed Mode Devices on the I²C Bus

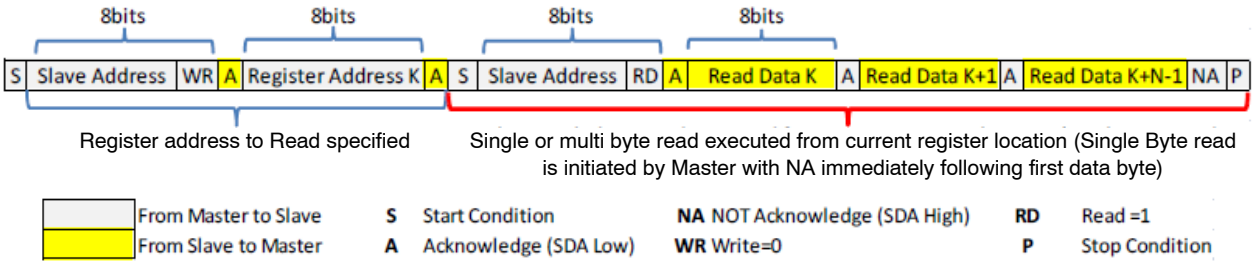
I²C INTERFACE

The FUSB301A includes a full I²C slave controller. The I²C slave fully complies with the I²C specification version 6 requirements. This block is designed for fast mode. Examples of an I²C write and read sequence are shown Figure 5 and Figure 6 respectively.



NOTE: Single Byte read is initiated by Master with P immediately following first data byte.

Figure 5. I²C Write Example



NOTE: If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed.

Figure 6. I²C Read Example

I²C ADDRESS

The I2CADDR bit high or low is indicated in bit3 of the slave address shown in Table 2.

Table 2. FUSB301A I²C SLAVE ADDRESS

Name	Size (Bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave Address	8	0	1	0	0	I2CADDR	0	1	R/W

REGISTER DEFINITIONS

Table 3. REGISTER MAP

Address	Register Name	Type	RST Val	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×01	Device ID	RO	12	Version ID [3:0]				Revision ID [3:0]			
0×02	Modes	R/W	04			DRP+ACC	DRP	Sink+ACC	Sink	Source+ACC	Source
0×03	Control	R/W	03			DRPTOGGLE			HOST_CUR1	HOST_CUR0	INT_MASK
0×04	Manual	W/C	00					UNATT_SNK	UNATT_SRC	DISABLED	ERROR_REC
0×05	Reset	W/C	00								SW_RES
0×06−0×0F	Reserved	X	xx	Do Not Use							
0×10	Mask	R/W	00					M_ACC_CH	M_BC_LVL	M_DETACH	M_ATTACH
0×11	Status	RO	00			ORIENT1	ORIENT0	VBUSOK	BC_LVL1	BC_LVL0	ATTACH
0×12	Type	RO	00				Sink	Source		DEBUGACC	AUDIOACC
0×13	Interrupt	R/C	00					I_ACC_CH	I_BC_LVL	I_DETACH	I_ATTACH
0×14−0×1F	Reserved	X	xx	Do Not Use							

6. Do not use registers that are blank.
7. Values read from undefined register bits are invalid. Do not write to undefined registers.

Table 4. DEVICE ID

Address: 01h
Reset Value: 0×0001_0010
Type: Read Only

Bit #	Name	Size (Bits)	Description
7:4	Version ID	4	Device version ID by Trim or etc. **A_[Version ID]: 0001 (FUSB301ATMX)**
3:0	Revision ID	4	Revision History of each version **[Revision ID]_revC: 0010**

Table 5. MODES

Address: 02h
Reset Value: 0×0000_0100
Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:6	Reserved	2	Do Not Use
5	DRP+ACC	1	1: Configure device as a Dual Role Port (DRP) with accessory support
4	DRP	1	1: Configure device as a Dual Role Port (DRP) without accessory support
3	Sink+ACC	1	1: Configure device as a Sink with accessory support
2	Sink	1	**1: Configure device as a Sink without accessory support**
1	Source+ACC	1	1: Configure device as a Source with accessory support
0	Source	1	1: Configure device as a Source without accessory support

Table 6. CONTROL
Address: 03h
Reset Value: 0×XX00_X011
Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:6	Reserved	2	Do Not Use
5:4	DRPTOGGLE	2	Selects different timing for Dual Role Port Toggle between Unattached. Sink State and Unattached.SOURCE State. **00: 35 ms min. in Unattached.Sink and 15 ms min. In Unattached.-SOURCE** 01: 30 ms min. In Unattached.Sink and 20 ms min. In Unattached.SOURCE 10: 25 ms min. In Unattached.Sink and 25 ms min. In Unattached.SOURCE 11: 20 ms min. In Unattached.Sink and 30 ms min. In Unattached.SOURCE
3	Reserved	1	Do Not Use
2:1	HOST_CUR [1:0]	2	1: Controls the pull−up current when device enabled as a Source 00: No Current **01: 80 μA − Default USB Power** 10: 180 μA − Medium Current Mode: 1.5 A 11: 330 μA − High Current Mode: 3 A
0	INT_MASK	1	**1: Global interrupt mask to mask all interrupts**

Table 7. MANUAL(Note 8)
Address: 04h
Reset Value: 0×XXXX_0000
Type: Write/Clear

Bit #	Name	Size (Bits)	Description
7:4	Reserved	4	Do Not Use
3	UNATT_SINK (Note 9)	1	1: Put device in Unattached.Sink state as defined in the Type C spec
2	UNATT_SOURCE	1	1: Put device in Unattached.Source state as defined in the Type C spec
1	DISABLED (Note 10)	1	1: Put device in Disabled state as defined in the Type C spec
0	ERROR_REC	1	1: Put device in ErrorRecovery state as defined in the Type C spec

8. If more than one bit is set to "b1" simultaneously then an order of priority will be used. 1st priority is DISABLED, 2nd is ERROR_REC, 3rd is UNATT_SOURCE, last is UNATT_SINK. The highest priority bit will take precedence and all other bits will be cleared automatically.
9. Wait 2 ms between Modes = Sink and Manual = UNATT_SINK writes.
10. The DISABLED bit must be manually cleared.

Table 8. RESET
Address: 05h
Reset Value: 0×XXXX_XXX0
Type: Write/Clear

Bit #	Name	Size (Bits)	Description
7:6	Reserved	7	Do Not Use
0	SW_RES	1	1: Reset the system and I2C Register.

Table 9. MASK
Address: 10h
Reset Value: 0×XXXX_0000
Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:4	Reserved	4	Do Not Use
3	M_ACC_CH	1	1: Mask a change from Accessory Present to Attached Accessory

Table 9. MASK (continued)
Address: 10h
Reset Value: 0×XXXX_0000
Type: Read/Write

Bit #	Name	Size (Bits)	Description
2	M_BC_LVL	1	1: Mask a change in I_BC_LVL interrupt bit
1	M_DETACH	1	1: Mask the I_DETACH interrupt bit
0	M_ATTACH	1	1: Mask a change in the I_ATTACH interrupt bit

Table 10. STATUS
Address: 11h
Reset Value: 0×XX00_0000
Type: Read

Bit #	Name	Size (Bits)	Description
7:6	Reserved	2	Do Not Use
5:4	ORIENT[1:0]	2	Status to indicate which CCx pins has the CC cable connection 11: A fault has occurred during the detection 10: Cable CC is connected through the CC2 pin 01: Cable CC is connected through the CC1 pin **00: No or unresolved connection detected.**
3	VBUSOK	1	1: Status to indicate VBUS is in the valid range
2:1	BC_LVL[1:0]	2	Thresholds that allow detection of current advertisement on CC line **00: Ra or unattached Sink** 01: Rd threshold for Sink default current advertisement 10: RD threshold for Sink 1.5 A current advertisement 11: RD threshold for Sink 3 A current advertisement
0	ATTACH	1	1: Attached to a device or accessory of a type shown in the Type register

Table 11. TYPE
Address: 12h
Reset Value: 0×XXX0_0X00
Type: Read

Bit #	Name	Size (Bits)	Description
7:5	Reserved	3	Do Not Use
4	Sink	1	1: Indicates a Sink has been detected
3	Source	1	1: Indicates a Source has been detected
2	Reserved	1	Do Not Use
1	DEBUGACC	1	1: Indicates a Debug Accessory has been detected
0	AUDIOACC	1	1: Indicates a Audio Accessory has been detected

Table 12. INTERRUPT0
Address: 13h
Reset Value: 0×XXXX_X000
Type: Write/Clear

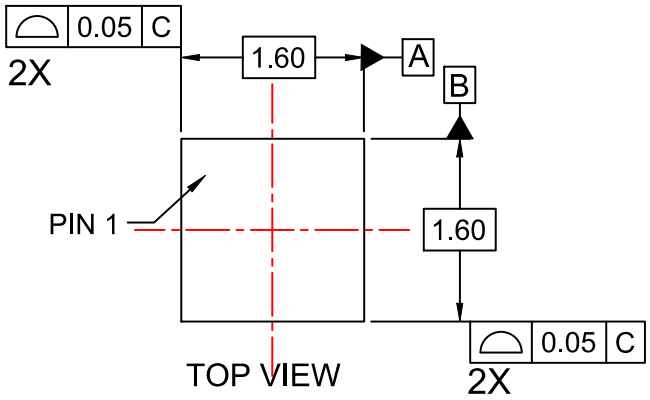
Bit #	Name	Size (Bits)	Description
7:4	Reserved	4	Do Not Use
3	I_ACC_CH	1	1: Interrupt flagged when a change from Accessory Present to Audio Accessory or Debug Accessory occurs.
2	I_BC_LVL	1	1: Interrupt flagged when a change in BC_LVL advertised current level has occurred

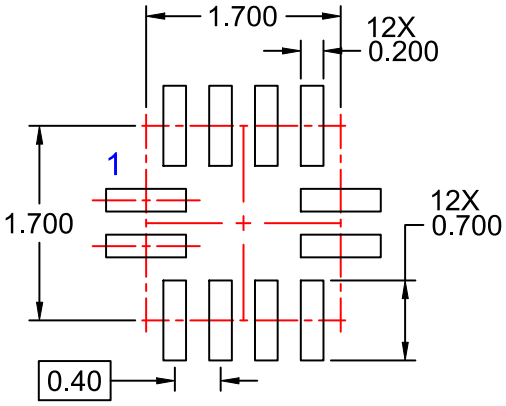
Table 12. INTERRUPT0 (continued)
Address: 13h
Reset Value: 0×XXXX_X000
Type: Write/Clear

Bit #	Name	Size (Bits)	Description
1	I_DETACH	1	1: Interrupt flagged when a device or accessory has been detached
0	I_ATTACH	1	1: Interrupt flagged when a device or accessory of type indicated in the Type register has been attached

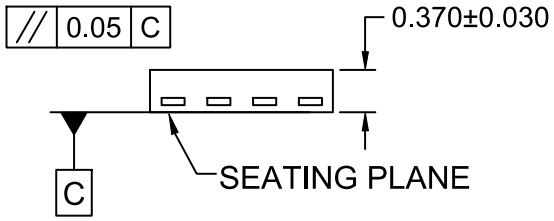
X2QFN12 1.6x1.6, 0.4P
CASE 722AD
ISSUE O

DATE 31 OCT 2016





LAND PATTERN RECOMMENDATION



SIDE VIEW

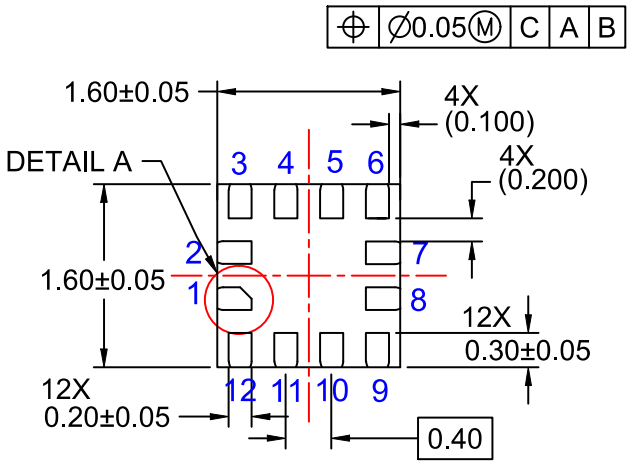
NOTES:

A. NO JEDEC REGISTRATION APPLIES.

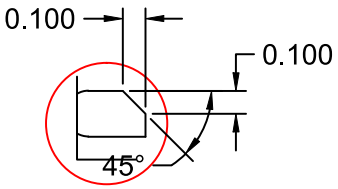
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 2009.

D. PACKAGE NOMINAL HEIGHT IS 370 MICRONS.



BOTTOM VIEW



DETAIL A 2X

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