## FAIRCHILD

## FST3244－8－Bit Bus Switch

## Features

－ $4 \Omega$ Switch Connection between Two Ports
－Minimal Propagation Delay through the Switch
－Low $\mathrm{I}_{\mathrm{Cc}}$
－Zero Bounce in Flow－through Mode
－Control Inputs Compatible with TTL Level

## Description

The FST3244 switch provides eight－bits of high－speed， CMOS，TTL－compatible bus switching in a standard＇244 pin－out．The low on resistance allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise．

The device is organized as two four－bit switches with separate／OE inputs．When／OE is LOW，the switch is ON and port A is connected to port $B$ ．When／OE is HIGH，the switch is OPEN and a high－impedance state exists between the two ports．

## Ordering Information

| Part Number | Operating <br> Temperatur <br> e Range | Package | Packing <br> Method |
| :--- | :---: | :--- | :--- | :--- |
| FST3244MTCX | -40 to $+85^{\circ} \mathrm{C}$ | 20－Lead Thin Shrink Small Outline Package（TSSOP），JEDEC MO－153， <br> 4.4 mm Wide | Tape and <br> Reel |

## Logic Diagram



Figure 1．Logic Diagram

## Pin Configurations



Figure 2. Pin Configuration

## Pin Descriptions

| Pin \# | Pin Names | Description |
| :---: | :---: | :---: |
| 1,19 | $/ \mathrm{OE}_{1}, / \mathrm{OE}_{2}$ | Bus Switch Enables |
| $2,4,6,8,11,13,15,17$ | $1 \mathrm{~A}, 2 \mathrm{~A}$ | Bus A |
| $3,5,7,9,12,14,16,18$ | $1 \mathrm{~B}, 2 \mathrm{~B}$ | Bus B |
| 20 | $\mathrm{~V}_{\mathrm{CC}}$ | Supply Voltage |
| 10 | GND | Ground |

## Truth Table

| Inputs |  | Inputs/Outputs |  |
| :---: | :---: | :---: | :---: |
| IOE1 | IOE $_{2}$ | 1A, 1B | 2A, 2B |
| LOW | LOW | $1 \mathrm{~A}=1 \mathrm{~B}$ | $2 \mathrm{~A}=2 \mathrm{~B}$ |
| LOW | HIGH | $1 \mathrm{~A}=1 \mathrm{~B}$ | High Impedance |
| HIGH | LOW | High Impedance | 2A = 2B |
| HIGH | HIGH | High Impedance | High Impedance |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Min. | Max. | Unit |
| :---: | :--- | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | -0.5 | 7.0 | V |
| $\mathrm{~V}_{\mathrm{S}}$ | DC Switch Voltage | -0.5 | 7.0 | V |
| $\mathrm{~V}_{\text {IN }}$ | DC Input VoItage ${ }^{(1)}$ | -0.5 | 7.0 | V |
| $\mathrm{I}_{\text {IK }}$ | DC Input Diode Current $\mathrm{V}_{\text {IN }}<0 \mathrm{~V}$ |  | -50 | mA |
| $\mathrm{I}_{\text {OUT }}$ | DC Output Sink Current |  | 128 | mA |
| $\mathrm{I}_{\mathrm{CC}} / \mathrm{I}_{\mathrm{GND}}$ | DC $\mathrm{V}_{\mathrm{CC}} /$ GND Current |  | $\pm 100$ | mA |
| $\mathrm{~T}_{\text {STG }}$ | Storage Temperature Range | -65 | +150 | ${ }^{\circ} \mathrm{C}$ |

Note:

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Min. | Max. | Unit |
| :---: | :--- | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Power Supply Operating | 4.0 | 5.5 | V |
| $\mathrm{~V}_{\mathrm{IN}}$ | Input Voltage | 0 | 5.5 | V |
| $\mathrm{~V}_{\mathrm{OUT}}$ | Output Voltage | 0 | 5.5 | V |
| $\mathrm{t}_{\mathrm{r}}, \mathrm{t}_{\mathrm{f}}$ | Input Rise and Fall Time | Switch Control Input ${ }^{(2)}$ | 0 | 5 |
|  |  | Switch I/O | $\mathrm{ns} / \mathrm{V}$ |  |
| $\mathrm{T}_{\mathrm{A}}$ | Operating Temperature, Free Air | 0 |  |  |

Note:
2. Unused control inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

Typical values are at $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.

| Symbol | Parameter | Conditions | $\mathrm{V}_{\mathrm{cc}}(\mathrm{V})$ | $\mathrm{T}_{\mathrm{A}}=-40$ to $+85^{\circ} \mathrm{C}$ |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min. | Typ. | Max. |  |
| $\mathrm{V}_{\mathrm{IK}}$ | Clamp Diode Voltage | $\mathrm{I}_{\mathrm{IN}}=-18 \mathrm{~mA}$ | 4.5 |  |  | -1.2 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-Level Input Voltage |  | 4.0 to 5.5 | 2.0 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low-Level Input Voltage |  | 4.0 to 5.5 |  |  | 0.8 | V |
| $\mathrm{I}_{\mathrm{IN}}$ | Input Leakage Current | $0 \leq \mathrm{V}_{\text {IN }} \leq 5.5 \mathrm{~V}$ | 5.5 |  |  | $\pm 1.0$ | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{Oz}}$ | Off-state Leakage Current | $0 \leq A, B \leq V_{c c}$ | 5.5 |  |  | $\pm 1.0$ | $\mu \mathrm{A}$ |
| $\mathrm{R}_{\text {ON }}$ | Switch On Resistance ${ }^{(3)}$ | $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}, \mathrm{I}_{\mathrm{IN}}=64 \mathrm{~mA}$ | 4.5 |  | 4 | 7 | $\Omega$ |
|  |  | $\mathrm{V}_{\text {IN }}=0 \mathrm{~V}, \mathrm{I}_{\text {IN }}=30 \mathrm{~mA}$ | 4.5 |  | 4 | 7 |  |
|  |  | $\mathrm{V}_{\mathrm{IN}}=2.4 \mathrm{~V}, \mathrm{I}_{\mathrm{IN}}=15 \mathrm{~mA}$ | 4.5 |  | 8 | 15 |  |
|  |  | $\mathrm{V}_{\mathrm{IN}}=2.4 \mathrm{~V}, \mathrm{I}_{\mathrm{IN}}=15 \mathrm{~mA}$ | 4.0 |  | 11 | 20 |  |
| $I_{\text {cc }}$ | Quiescent Supply Current | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{CC}} \text { or } \mathrm{GND}, \\ & \mathrm{l}_{\text {OUT }}=0 \end{aligned}$ | 5.5 |  |  | 3 | $\mu \mathrm{A}$ |
| $\Delta l_{\text {cc }}$ | Increase in $\mathrm{I}_{\text {cc }}$ per Input | One Input at 3.4 V , Other Inputs at $\mathrm{V}_{\mathrm{Cc}}$ or GND | 5.5 |  |  | 2.5 | mA |

## Note:

3. Measured by the voltage drop between the $A$ and $B$ pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the A or B pins.

## AC Electrical Characteristics

$\mathrm{T}_{\mathrm{A}}=-40$ to $+85^{\circ} \mathrm{C}, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$, and $\mathrm{R}_{\mathrm{U}}=\mathrm{R}_{\mathrm{D}}=500 \Omega$.

| Symbol | Parameter | Conditions | $\mathrm{V}_{\mathrm{cc}}=4.5-5.5 \mathrm{~V}$ |  | $\mathrm{V}_{\mathrm{cc}}=4.0 \mathrm{~V}$ |  | Units | Figure |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min. | Max. | Min. | Max. |  |  |
| $\mathrm{t}_{\text {PHL }}, \mathrm{t}_{\text {PLH }}$ | Propagation Delay Bus-to Bus ${ }^{(4)}$ | $\mathrm{V}_{\text {IN }}=$ Open |  | 0.25 |  | 0.25 | ns | Figure 3 Figure 4 |
| $\mathrm{t}_{\text {PZH }}, \mathrm{t}_{\text {PZL }}$ | Output Enable Time | $\begin{aligned} & \mathrm{V}_{\text {IN }}=7 \mathrm{~V} \text { for } \mathrm{t}_{\text {PZL }} \\ & \mathrm{V}_{\text {IN }}=\text { Open for } \\ & \mathrm{t}_{\text {PZH }} \end{aligned}$ | 1.0 | 5.6 |  | 6.1 | ns | Figure 3 Figure 4 |
| $\mathrm{t}_{\text {PHZ }}, \mathrm{t}_{\text {PLZ }}$ | Output Disable Time | $\begin{aligned} & V_{\text {IN }}=7 \mathrm{~V} \text { for } \mathrm{t}_{\text {PLZ }} \\ & V_{\text {IN }}=\text { Open for } \\ & t_{\text {PHZ }} \end{aligned}$ | 1.0 | 6.2 |  | 5.6 | ns | Figure 3 Figure 4 |

## Note:

4. This parameter is guaranteed by design, but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the 50 pF load capacitance when driven by an ideal voltage source (zero output impedance).

## Capacitance

$\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{f}=1 \mathrm{MHz}$. Capacitance is characterized, but not tested.

| Symbol | Parameter | Conditions | Typ. | Units |
| :---: | :--- | :--- | :---: | :---: |
| $\mathrm{C}_{1 \mathrm{~N}}$ | Control Pin Input Capacitance | $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ | 3 | pF |
| $\mathrm{C}_{/ / \mathrm{O}}$ | Input/Output Capacitance | $\mathrm{V}_{\mathrm{CC}}, / \mathrm{OE}=5.0 \mathrm{~V}$ | 5 | pF |

## AC Loadings and Waveforms



Figure 3. AC Test Circuit


Figure 4. AC Waveforms

## Physical Dimensions



LAND PATTERN RECOMMENDATION


Figure 5. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4 mm Wide

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| BitSiC'm | GreenBridge ${ }^{\text {TM }}$ | QFET ${ }^{\text {® }}$ |  |
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| CROSSVOLT ${ }^{\text {TM }}$ | GTOTM | $)^{\text {Tm }}$ | TINYOPTOTM |
| CTL ${ }^{\text {™ }}$ | IntelliMAX'm | Saving our morld, $1 \mathrm{~mW} / \mathrm{W} / \mathrm{kW}$ at a time ${ }^{\text {TM }}$ | TinyPowertm |
| Current Transfer Logic ${ }^{\text {m }}$ | ISOPLANAR ${ }^{\text {TM }}$ ( ${ }^{\text {a }}$ | SignalMise ${ }^{\text {Tm }}$ | TinyPMM ${ }^{\text {TM }}$ |
| DEUXPEED ${ }^{\text {a }}$ | Making Small Speakers Sound Louder | SmartMax ${ }^{\text {™ }}$ | Tiny ${ }^{\text {Mire }}{ }^{\text {m }}$ |
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| EfficientMax ${ }^{\text {™ }}$ | MICROCOUPLER ${ }^{\text {™ }}$ | Solutions for Your Success ${ }^{\text {TM }}$ SPM ${ }^{\text {® }}$ | TriFault Detect ${ }^{\text {TM }}$, |
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| $5^{\text {® }}$ | MicroPak'm | SuperFET ${ }^{\text {® }}$ | $\boldsymbol{H}$ |
| Fairchild ${ }^{\text {® }}$ | MicroPak2 ${ }^{\text {Tm }}$ | SuperSOTTM-3 | SerDes: |
| Fairchild Semiconductor ${ }^{(1)}$ | MilierDrive ${ }^{\text {a }}$ | SuperSOT ${ }^{\text {Tm-6 }}$ | UHC ${ }^{\text {® }}$ |
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