Low EMI Spread Spectrum Clock

Features

- Spread Spectrum Clock Generator (SSCG) with 1x Spread and 1X non-Spread Output.
- 6 to 82 MHz operating frequency range.
- Modulates external clocks including crystals, crystal oscillators and ceramic resonators.
- Programmable modulation with simple R-C external loop filter (LF)
- Provides Two Output Clocks, One Modulated and One Non-Modulated clock.
- Center Spread Modulation.
- 3 - 5 Volt power supply.
- TTL/CMOS compatible outputs.
- Low short term jitter.
- Low Power Dissipation;

  3.3 VDC = 37 mW – typical
  5.0 VDC = 115 mW - typical
- Available in 8 pin SOIC package.

Applications

- Desktop/Notebook Computers
- Printers, Copiers and MFP
- Scanners and Fax
- LCD Displays and Monitors
- CD-ROM, VCD and DVD
- Automotive and Embedded Systems
- Networking, LAN/WAN
- Digital Cameras and Camcorders
- Modems

Benefits

- Programmable EMI Reduction
- Fast Time to Market
- Lower cost of compliance
- No degradation in Rise/Fall times
- Lower component and PCB layer count

Product Description

The CYPRESS FS786/787 are Spread Spectrum Clock Generator ICs (SSCG) designed for the purpose of reducing Electro Magnetic Interference (EMI) found in today's high-speed digital systems.

The FS786/787 SSCG clocks use an Cypress proprietary technology to modulate the input clock frequency, FSOUT by modulating the frequency of the digital clock. By modulating the reference clock the measured EMI at the fundamental and harmonic frequencies of FSOUT is greatly reduced. This reduction in radiated energy can significantly reduce the cost of complying with regulatory requirements without degrading digital waveforms.

The CYPRESS FS786/787 clocks are very simple and versatile devices to use. Range selection is performed via one pin, D0. The **FS786/787** are designed to operate over a very wide range of input frequencies and provide one modulated and one non-modulated output.

The FS786/787 devices have a simple frequency selection table that allows operation from 6 MHz to 82 MHz in two separate ranges and two separate parts. The bandwidth of the frequency spread at FSOUT is determined by the values of the loop filter components. The modulation rate is determined internally by the input frequency and the selected input frequency range.

The Bandwidth of these products can be programmed from as little as 0.6% up to as much as 4.0% by selecting the proper loop filter value. Refer to the Loop Filter Selection chart on page 6 for recommended values. Due to a wide range of application requirements, an external loop filter (LF) is used on the FS786/787 products. The user can select the exact amount of frequency modulation suitable for the application. Using a fixed internal loop filter would severely limit the use of a wide range of modulation bandwidths (Spread %) to a few discrete values.

Refer to FS791/2/4 products for applications requiring 80 to 140 MHz frequency range.

Block Diagram

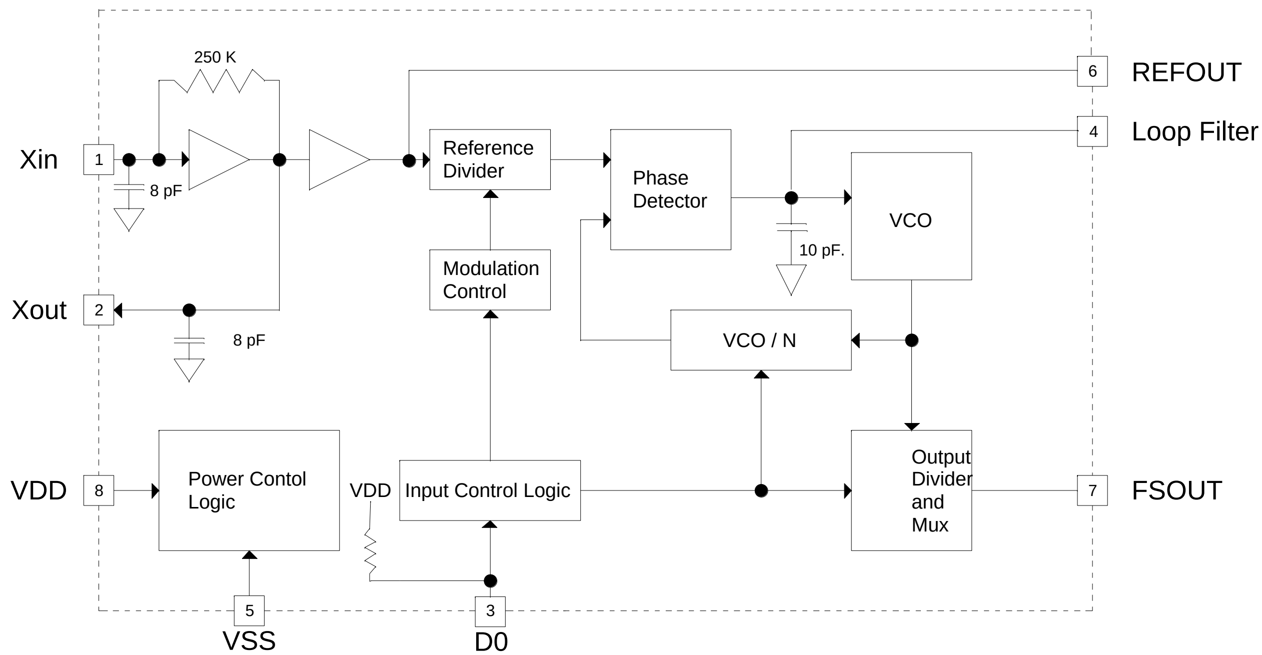


Figure 1.

Ordering Information

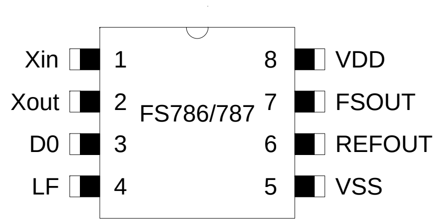
Product Number	Frequency Range	Package Type	Production Flow
FS786BZ	16 – 32 MHz, 64 – 82 MHz	8 Pin 150 mil SOIC	Commercial, 0 to 70°C
FS787BZ	6 – 14 MHz, 34 – 62 MHz	8 Pin 150 mil SOIC	Commercial, 0 to 70°C

Marking Example: Date Code
FS786BZB (FS787BZB)
Lot Number

FS786BZ

- Package
  Z = SOIC (150 Mil)
- Revision
- Device Number

Pin Configuration



Refer to page 11 for package dimensions.

Pin Description

Pin No.	Pin Name	I/O	TYPE	Description
1/2	Xin / Xout	I/O	Analog	Pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Xin may be connected to TTL/CMOS external clock source. If Xin connected to external clock other than crystal, leave Xout (pin 2) unconnected.
3	D0	I	CMOS/TTL	Input frequency range selection. Has internal pull-up resistor. FS786 → 0 = 16 – 32 MHz, 1 = 64 – 82 MHz. FS787 → 0 = 6 – 14 MHz, 1 = 34 – 62 MHz.
4	LF	I	Analog	Loop Filter. Single ended tri-state output of the phase detector. A passive RC filter is connected to the Loop Filter pin (LF).
5	VSS	P	Power	Power Supply Ground.
6	REFOUT	O	CMOS/TTL	Non-Modulated Clock Output of Reference Oscillator.
7	FSOUT	O	CMOS/TTL	Modulated Clock Output of Reference Oscillator. Frequency is center spread and 1X of reference clock.
8	VDD	P	Power	Positive Power Supply.

Table 1. Pin Description

Output Frequency Selection

Product Number	FSOUT Frequency Scaling	Description
FS786	1x	1X Modulated Clock + 1X Non-Modulated Clock
FS787	1x	1X Modulated Clock + 1X Non-Modulated Clock

Table 2. FSOUT SSCG (Modulated Output Clock) Product Selection

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of any voltage higher than the absolute maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range, VSS < (Vin or Vout) < VDD. All digital inputs are tied high or low internally. Refers to electrical specifications for operating supply range.

Absolute Maximum Ratings[1]

Item	Symbol	Min	Max	Units
Operating Voltage	VDD	3.0	6.0	VDC
Input, relative to VSS	VIRvss	-0.3	VDD +0.3	VDC
Output, relative to VSS	VORvss	-0.3	VDD +0.3	VDC
AVDD relative to DVDD	ΔVpp	-100	+100	mV
AVSS relative to DVSS	ΔVss	-100	+100	mV
Temperature, Operating	TOP	0	+ 70	^{0}C
Temperature, Storage	TST	- 65	+ 150	^{0}C

Table 3

Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Units
Input Low Voltage	VIL	-	-	0.3 * VDD	VDC
Input High Voltage	VIH	0.7 * VDD	-	-	VDC
Input Low Current	IIL	-	-	100	µA
Input High Current	IIH	-	-	100	µA
Output Low Voltage IOL= 10mA, VDD = 5V	VOL	-	-	0.4	VDC
Output High Voltage IOH = 10mA, VDD = 5V	VOH	VDD-1.0	-	-	VDC
Output Low Voltage IOL= 6mA, VDD = 3.3V	VOL	-	-	0.4	VDC
Output High Voltage IOH = 5mA,VDD = 3.3V	VOH	2.4	-	-	VDC
Resistor, Pull Up (Pin-3)	Rpu	60K	125K	200K	Ohms
Input Capacitance (Pin-1)	C_{in1}	-	8	-	pF
Output Capacitance (Pin-2)	C_{in2}	-	8	-	pF
5 Volt Dynamic Supply Current (CL = No Load)	ICC	-	38	-	mA
3.3 Volt Dynamic Supply Current (CL = No Load)	ICC	-	20	-	mA
Short Circuit Current (FSOUT)	ISC	-	25	-	mA
Test measurements performed at VDD = 3.3V and 5.0V ±10%, Xin = 48 MHz, Ta = 0°C to 70°C					

Table 4

[1] **Single Power Supply:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up.

Timing Characteristics

Characteristic	Symbol	Min.	Typ.	Max.	Units
FSOUT Rise Time @ 10 - 90% at 5 VDC	tTLH	2.0	2.2	2.5	ns
FSOUT Fall Time @ 10 - 90% at 5 VDC	tTHL	1.7	2.0	2.2	ns
FSOUT Rise Time @ 0.8 - 2.0V at 5 VDC	tTLH	0.50	0.65	0.75	ns
FSOUT Fall Time @ 0.8 - 2.0V at 5 VDC	tTHL	0.50	0.65	0.75	ns
FSOUT Rise Time @ 10 - 90% at 3.3 VDC	tTLH	2.6	2.65	2.9	ns
FSOUT Fall Time @ 10 - 90% at 3.3 VDC	tTHL	2.0	2.1	2.2	ns
FSOUT Rise Time @ 0.8 - 2.0V at 3.3 VDC	tTLH	0.8	0.95	1.1	ns
FSOUT Fall Time @ 0.8 - 2.0V at 3.3 VDC	tTHL	0.78	0.85	0.9	ns
FSOUT Duty Cycle @ 50% of VDD	TsymF1	45	50	55	%
FSOUT, Cycle to Cycle Jitter, 48 MHz @ 3.30 VDC	CCJ	-	320	370	ps
FSOUT, Cycle to Cycle Jitter, 48 MHz @ 5.00 VDC	CCJ	-	310	360	ps
FSOUT, Cycle to Cycle Jitter, 72 MHz @ 3.30 VDC	CCJ	-	270	325	ps
FSOUT, Cycle to Cycle Jitter, 72 MHz @ 5.00 VDC	CCJ	-	390	440	ps
REFOUT Rise Time @ 10 – 90% at 5 VDC	tTLH	4.2	4.5	4.9	ns
REFOUT Fall Time @ 10 – 90% at 5 VDC	tTHL	2.5	2.65	2.8	ns
REFOUT Rise Time @ 0.8 – 2.0 V at 5 VDC	tTLH	0.74	0.80	0.86	ns
REFOUT Fall Time @ 0.8 – 2.0 V at 5 VDC	tTHL	0.76	0.85	0.93	ns
REFOUT Rise Time @ 10 – 90% at 3.3 VDC	tTLH	4.6	4.95	5.3	ns
REFOUT Fall Time @ 10 – 90% at 3.3 VDC	tTHL	2.5	2.65	2.8	ns
REFOUT Rise Time @ 0.8 – 2.0 V at 3.3 VDC	tTLH	1.4	1.5	1.6	ns
REFOUT Fall Time @ 0.8 – 2.0 V at 3.3 VDC	tTHL	1.00	1.1	1.2	ns
Unless otherwise indicated, measurements performed at VDD = 3.3 and 5.0V ± 10%, Ta = 0°C to 70°C, CL = 15pF, Xin = 48 MHz.					

Table 5

Application Selection Table

Select the row containing the frequency for the intended application. Read the device number and D0 programming in cells to the right of Fin. The Modulation Rate is also given below.

Fin (MHz) (pin 1/2)	D0 (pin 3)	Modulation Rate	Device to Use
6 – 14	0	Fin/120	FS787BZB
16 – 32	0	Fin/240	FS786BZB
34 - 62	1	Fin/480	FS787BZB
64 - 82	1	Fin/720	FS786BZB

Table 6

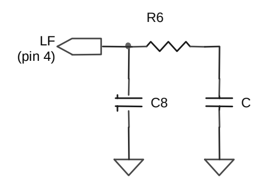
FS786 Loop Filter Selection Chart

The following table provides a list of recommended loop filter values for the FS786. The FS786 is divided into 2 ranges and operates at both 3.3 and 5.0 VDC. The loop filter at the right is representative of the loop filter components in the table below.

FS786 Recommended Loop Filter Values.								
		C7 (pF.) @ +3.3 VDC +/- 5% (R6 = 3.3K)						
Input (MHz)	**D0 (pin 3)**	**BW = 1.0% (note 2)**	**BW = 1.5% (note 2)**	**BW = 2.0% (note 2)**	**BW = 2.5% (note 2)**	**BW = 3.0% (note 2)**	**BW = 3.5% (note 2)**	**BW = 4.0% (note 2)**
16	0	10000	980	760	580	470	410	385
18	0	1200	750	580	470	415	370	300
20	0	1000	730	470	390	320	220	190
22	0	960	640	410	270	230	200	180
24	0	920	400	250	210	180	160	150
26	0	660	300	220	180	150	140	120
28	0	470	230	180	150	130	100	70
30	0	470	180	140	120	100	80	60
32	0	330	170	120	100	82	68	47
64	1	1180	860	560	410	340	290	230
65	1	1180	850	540	400	330	280	220
66	1	1180	760	560	350	260	220	210
68	1	1180	750	500	320	260	230	210
70	1	1120	740	470	370	300	240	170
72	1	1160	780	470	300	250	220	190
74	1	1110	770	470	280	230	210	190
76	1	1000	720	440	240	210	190	170
78	1	910	670	270	210	190	170	160
80	1	900	620	260	210	190	170	156
82	1	900	540	250	210	190	170	150
		C7 (pF.) @ +5.0 VDC +/- 5% (R6 = 3.3K)						
Input (MHz)	**D0**	**BW = 1.0% (note 2)**	**BW = 1.5% (note 2)**	**BW = 2.0% (note 2)**	**BW = 2.5% (note 2)**	**BW = 3.0% (note 2)**	**BW = 3.5% (note 2)**	**BW = 4.0% (note 2)**
16	0	2200	860	640	520	420	375	330
18	0	2200	770	575	450	375	325	275
20	0	1200	600	425	325	250	170	220
22	0	870	490	290	230	200	180	170
24	0	720	320	220	180	160	140	130
26	0	465	235	185	150	130	100	75
28	0	380	205	160	130	100	90	80
30	0	220	178	135	95	85	80	72
62	1	Note 4.	800	580	430	330	250	180
64	1	Note 4.	720	490	375	285	200	140
66	1	Note 4.	630	400	320	240	150	100
68	1	Note 4.	690	365	285	225	170	140
70	1	Note 4.	650	330	250	210	~~190~~	180
72	1	Note 4.	575	340	250	210	190	170
74	1	Note 4.	500	355	245	205	180	165
76	1	Note 4.	550	330	230	200	175	160
78	1	Note 4.	600	290	220	190	170	155
80	1	Note 4.	570	240	210	185	165	150
82	1	Note 4.	540	250	200	180	160	140

Notes:
1. If the value selected from the above chart is not a standard value, use the next available larger value.
2. All bandwidths indicated are total peak-to-peak spread. 1% = +0.5% to –0.5%. 4% = +2.0% to –2.0%.
3. If C8 is not listed in the chart for a particular BW and Freq., it is not used in the loop filter.
4. Contact Factory for these Loop Filter values and bandwidths less than 1.0%.

Table 7.



FS787 Loop Filter Selection Chart

The following table provides a list of recommended loop filter values for the FS787. The FS787 is divided into 2 ranges and operates at both 3.3 and 5.0 VDC. Refer to the Loop Filter schematic on previous page for component references.

FS787 Recommended Loop Filter Values.

		C7 (pF.) @ +3.3 VDC +/- 5% (R6 = 3.3K)						
Input (MHz)	**D0**	**BW = 1.0% (note 2)**	**BW = 1.5% (note 2)**	**BW = 2.0% (note 2)**	**BW = 2.5% (note 2)**	**BW = 3.0% (note 2)**	**BW = 3.5% (note 2)**	**BW = 4.0% (note 2)**
6	0	10,000/1000	1500	880	750	680	620	540
8	0	10,000/330	960	790	620	500	430	390
10	0	1000	660	440	350	290	230	200
12	0	800	410	290	215	195	180	160
14	0	560	220	190	150	130	100	75
34	1	10000	860	640	520	430	380	330
36	1	2200	820	620	470	400	330	290
38	1	1500	690	520	410	340	290	240
40	1	960	600	420	340	280	220	160
42	1	940	620	380	275	230	210	180
44	1	950	680	400	250	210	190	170
46	1	900	580	270	220	190	180	165
48	1	790	440	260	210	180	160	140
50	1	660	360	250	190	170	150	140
52	1	470	325	220	185	155	135	120
54	1	470	270	200	170	140	130	100
56	1	445	250	185	150	120	85	47
58	1	430	210	165	130	100	65	33
60	1	295	185	150	120	100	90	82
62	1	270	220	150	120	100	82	68
		C7 (pF.) @ +5.0 VDC +/- 5% (R6 = 3.3K)						
Input (MHz)	**D0**	**BW = 1.0% (note 2)**	**BW = 1.5% (note 2)**	**BW = 2.0% (note 2)**	**BW = 2.5% (note 2)**	**BW = 3.0% (note 2)**	**BW = 3.5% (note 2)**	**BW = 4.0% (note 2)**
6	0	1110	1000	900	800	690	590	490
8	0	1130	940	720	550	450	390	270
10	0	1000	640	420	340	270	200	130
12	0	740	330	220	190	170	150	130
14	0	440	230	170	135	100	70	47
32	1	Note 4.	900	670	510	420	370	330
34	1	Note 4.	890	635	470	380	325	270
36	1	Note 4.	870	600	430	340	280	210
38	1	Note 4.	795	500	345	276	242	202
40	1	Note 4.	720	410	260	212	204	194
42	1	930	610	320	230	196	184	172
44	1	710	500	230	200	180	170	150
46	1	1000	375	255	185	165	150	130
48	1	1000	250	180	170	150	130	110
50	1	750	300	180	160	140	120	100
52	1	500	310	185	155	130	110	85
54	1	460	250	165	130	100	97	82
56	1	420	190	145	110	90	85	80
58	1	405	200	225	95	80	75	70
60	1	385	220	110	80	75	70	60

Notes:

1. If the value selected from the above chart is not a standard value, use the next available larger value.
2. All bandwidths indicated are total peak-to-peak spread. 1% = +0.5% to –0.5%. 4% = +2.0% to –2.0%.
3. If C8 is not listed in the chart for a particular BW and Freq., it is not used in the loop filter.
4. Contact Factory for these Loop Filter values and bandwidths less than 1.0%.

Table 8.

SSCG Modulation Profile

The digital control input D0 determines the modulation frequency of the FS786 and FS787 products. The modulation frequency is determined by dividing the input frequency by a constant divisor. One of 4 divisor numbers are used, depending on the device and setting of D0. The modulation frequency of the FS786/787 can be determined from Table 8. Select the device and input frequency on Table 8 and read the Modulation Divider. Then, divide the input frequency by the Modulation Divider.

Device	D0	Input Frequency Range (MHz)	Modulation Divider Number
FS787	0	6 to 14	120
FS786	0	16 to 32	240
FS787	1	32 to 62	480
FS786	1	64 to 82	720

Table 11

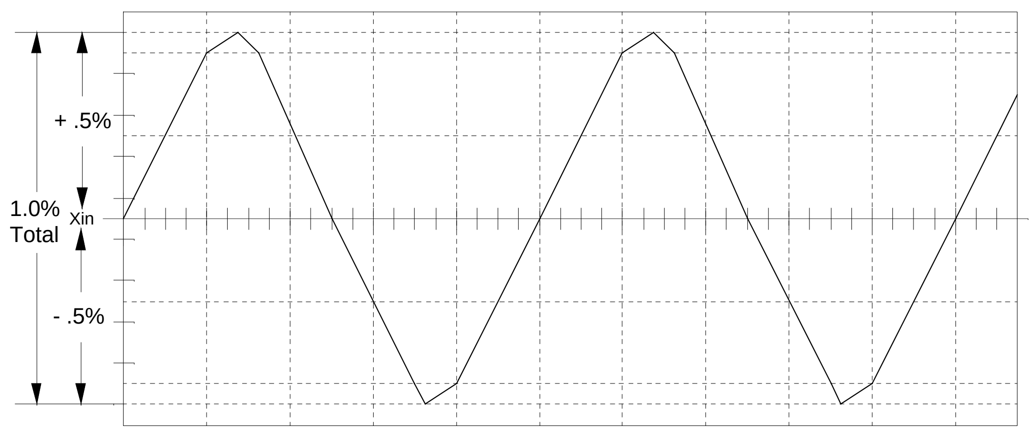
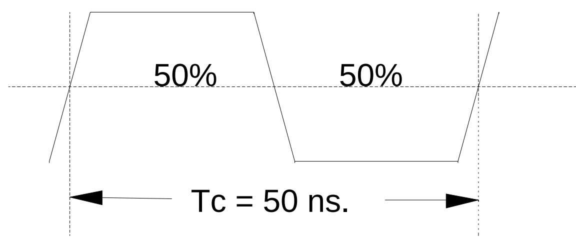


Figure 5. Frequency Profile in Time Domain

With the correct loop filter connected to pin 4, the profile in figure 5 above will provide the best EMI reduction. This profile can be seen on a Time Domain Analyzer.

Theory of Operation

The FS786/787 devices are Phase Lock Loop (PLL) type clock generators using Direct Digital Synthesis (DDS). By precisely controlling the bandwidth of the output clock, the FS786/787 products become a Low EMI clock generator. The theory and detailed operation of these products will be discussed in the following sections.



EMI

All clocks generate unwanted energy in their harmonics. Conventional digital clocks are square waves with a duty cycle that is very close to 50 %. Because of the 50/50 duty cycle, digital clocks generate most of their harmonic energy in the odd harmonics, i.e.; 3rd, 5th, 7th etc. It is possible to reduce the amount of energy contained in the fundamental and harmonics by increasing the bandwidth of the fundamental clock frequency. Conventional digital clocks have a very high Q factor, which means that all of the energy at that frequency is concentrated in a very narrow bandwidth, consequently, higher energy peaks. Regulatory agencies test electronic equipment by the amount of peak energy radiated from the equipment. By reducing the peak energy at the fundamental and harmonic frequencies, the equipment under test is able to satisfy agency requirements for Electro-Magnetic Interference (EMI). Conventional methods of reducing EMI have been to use shielding, filtering, multi-layer PCB's etc. The FS786 and 787 use the approach of reducing the peak energy in the clock by increasing the clock bandwidth, and lowering the Q of the clock.

SSCG

The FS786/787 products use a unique method of modulating the clock over a very narrow bandwidth and controlled rate of change, both peak to peak and cycle to cycle. The FS78x products take a narrow band digital reference clock in the range 6 - 82 MHz and produce a clock that sweeps between a controlled start and stop frequency and precise rate of change. To understand what happens to an SSCG clock, consider that we have a 20 MHz clock with a 50 % duty cycle. From a 20 MHz clock we know the following;

Clock Frequency = Fc = 20 MHz.
Clock Period = Tc = 1/20 MHz=50 ns

Consider that this 20 MHz clock is applied to the Xin input of the FS78x, either as an externally driven clock or as the result of a parallel resonant crystal connected to pins 1 and 2 of the FS78x. Also consider that the products are operating from a 5-volt DC power supply and the loop filter is set for a total bandwidth spread of 2%. Refer to table 6 on page 6.
From the above parameters, the output clock at FSOUT will be sweeping symmetrically around a center frequency of 20 MHz.
The minimum and maximum extremes of this clock will be +200 kHz and -200 kHz. So, we have a clock that is sweeping from 19.8 MHz to 20.2 MHz and back again. If we were to look at this clock on a spectrum analyzer we would see the picture in figure 7. Keep in mind that this is a drawing of a perfect clock with no noise.

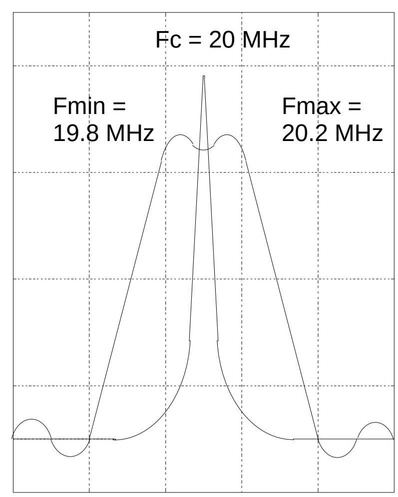


Figure 7.

We see that the original 20 MHz reference clock is at the center Frequency, Cf, and the minimum and maximum extremes are positioned symmetrically about the center frequency. This type of modulation is called **Center-Spread**. Figure 8 shows a 20 MHz clock, as it would be seen on an oscilloscope. The top trace is the non-modulated reference clock,. The bottom trace is the modulated clock at pin 6. From this comparison chart you can see that the frequency is decreasing and the period of each successive clock is increasing. The Tc measurements on the left and right of the bottom trace indicate the max. and min. extremes of the clock. Intermediate clock changes are small and accumulate to achieve the total period deviation. The reverse of this figure would show the clock going from min. extreme back to the high extreme.

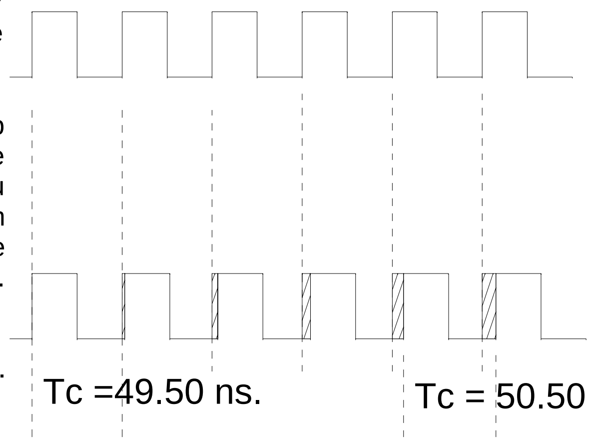


Figure 8. Period Comparison Chart

Looking at figure 7, you will note that the peak amplitude of the 20 MHz non-modulated clock is higher than the wideband modulated clock. This difference in peak amplitudes between modulated and unmodulated clocks is the reason why SSCG clocks are so effective in digital systems. This figure refers to the fundamental frequency of a clock. A very important characteristic of the SSCG clock is that the bandwidth of the fundamental frequency is multiplied by the harmonic number. In other words, if the bandwidth of a 20 MHz clock is 200 kHz, the bandwidth of the 3rd harmonic will be 3 times 200, or 600 kHz. The amount of bandwidth is relative to the amount of energy in the clock. Consequently, the wider the bandwidth, the greater the energy reduction of the clock.

Most applications will not have a problem meeting agency specifications at the fundamental frequency. It is the higher harmonics that usually cause the most problems. With an SSCG clock, the bandwidth and peak energy reduction increases with the harmonic number. Consider that the 11th harmonic of a 20 MHz clock is 220 MHz. With a total spread of 200 kHz at 20 MHz, the spread at the 11th harmonic would be 2.20 MHz which greatly reduces the peak energy content. It is typical to see as much as 12 to 18 dB. reduction at the higher harmonics, due to a modulated clock.

The difference in the peak energy of the modulated clock and the non-modulated clock in typical applications will see a 2 - 3 dB. reduction at the fundamental and as much as 8 - 10 dB. reduction at the intermediate harmonics, 3rd, 5th, 7th etc. At the higher harmonics, it is quite possible to reduce the peak harmonic energy, compared to the unmodulated clock, by as much as 12 to 18 dB.

Application Notes and Schematic

The schematic at the right is configured for the following parameters;

Package selected = FS786

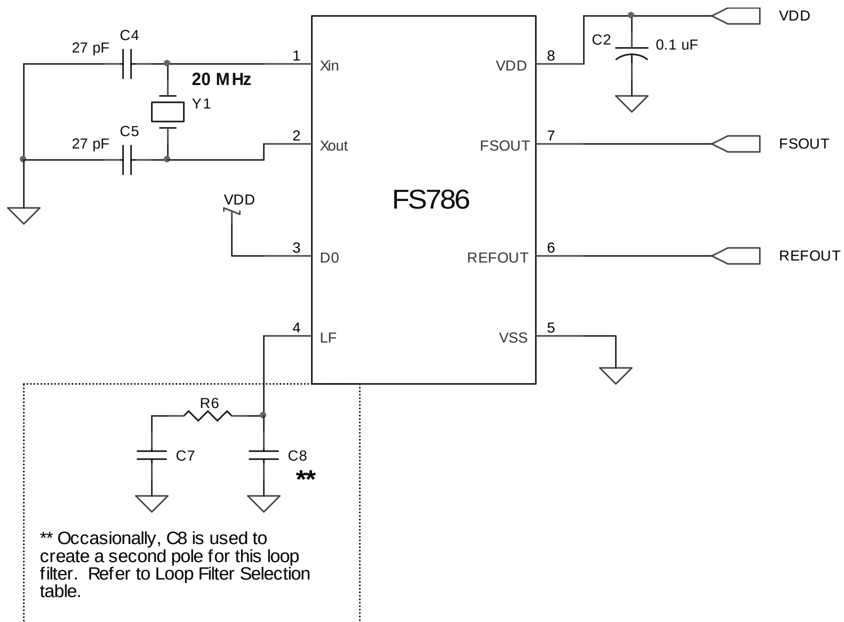
Crystal is a 20 MHz, Fundamental, with 18 pF load capacitance.

If Crystal load capacitance is different than 18 pF, C1 and C2 must be re-calculated.

For third overtone crystals, a parallel or series resonant trap is required.

Mount loop filter components as close to LF pin as possible.

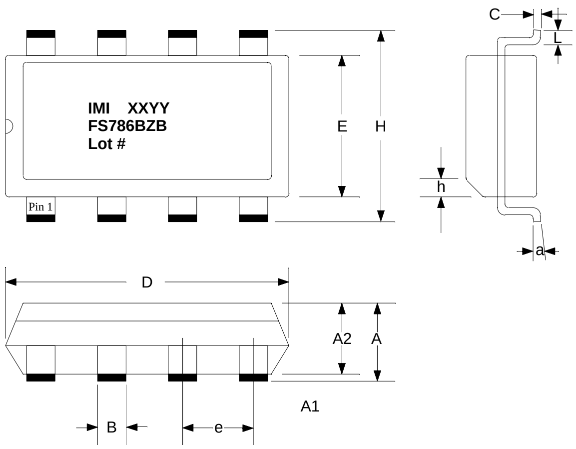
Bandwidth is determined by the value of the Loop Filter components connected to pin 4.



By selecting the FS786 or the FS787 and selecting D0 low or high, any input frequency from 6 to 82 MHz can be modulated. In addition to providing a modulated Low EMI clock, the FS786 and FS787 also provide a non-modulated clock which is a buffered copy of the reference oscillator.

Package Drawing and Dimensions

8 Pin SOIC Outline Dimensions



	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.061	0.064	0.068	1.55	1.63	1.73
A_1	0.004	0.006	0.0098	0.127	0.150	0.250
A_2	0.055	0.058	0.061	1.40	1.47	1.55
B	0.0138	0.016	0.0192	0.35	0.41	0.49
C	0.0075	0.008	0.0098	0.19	0.20	0.25
D	0.189	0.194	0.196	4.80	4.93	4.98
E	0.150	0.155	0.157	3.81	3.94	3.99
e	0.050 BSC			1.270 BSC		
H	.230	.236	.244	5.84	5.99	6.20
h	0.010	0.013	0.016	0.25	0.33	0.41
a	0°	5°	8°	0°	5°	8°
L	0.016	0.025	0.035	0.41	0.64	0.89

Document Title: FS786/787 Low EMI Spread Spectrum Clock **Document Number:** 38-07031				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106959	06/11/01	IKA	Convert from IMI to Cypress
*A	122680	12/14/02	RBI	Added power up requirements to Absolute Maximum Ratings information.