National Semiconductor

May 2002

FPD33684A/ FPD33684B Low Power, Low EMI, TFT-LCD Column Driver with RSDS™ Inputs, 64 Grayshades, and 384 Outputs for XGA/SXGA Applications

General Description

The FPD33684 Column Driver is a direct drive, 64 gray level, 384 output, TFT-LCD column driver with an RSDS™ data interface. It provides the capability to display 262,144 colors (18-bit color) with a large dynamic output range for twisted nematic applications. When used in a bank with other FPD33684 column drivers, the FPD33684 can support both XGA (8 drivers) or SXGA (10 drivers) applications. Output voltages are programmably gamma corrected to provide a direct mapping between digital video and LCD panel brightness.

An RSDS™ (Reduced Swing Differential Signaling) interface is used between the timing controller and the column driver to minimize EMI and reduce power.

The FPD33684 offers a low power, low EMI column driver solution with direct-drive dynamic range and dot-inversion addressing.

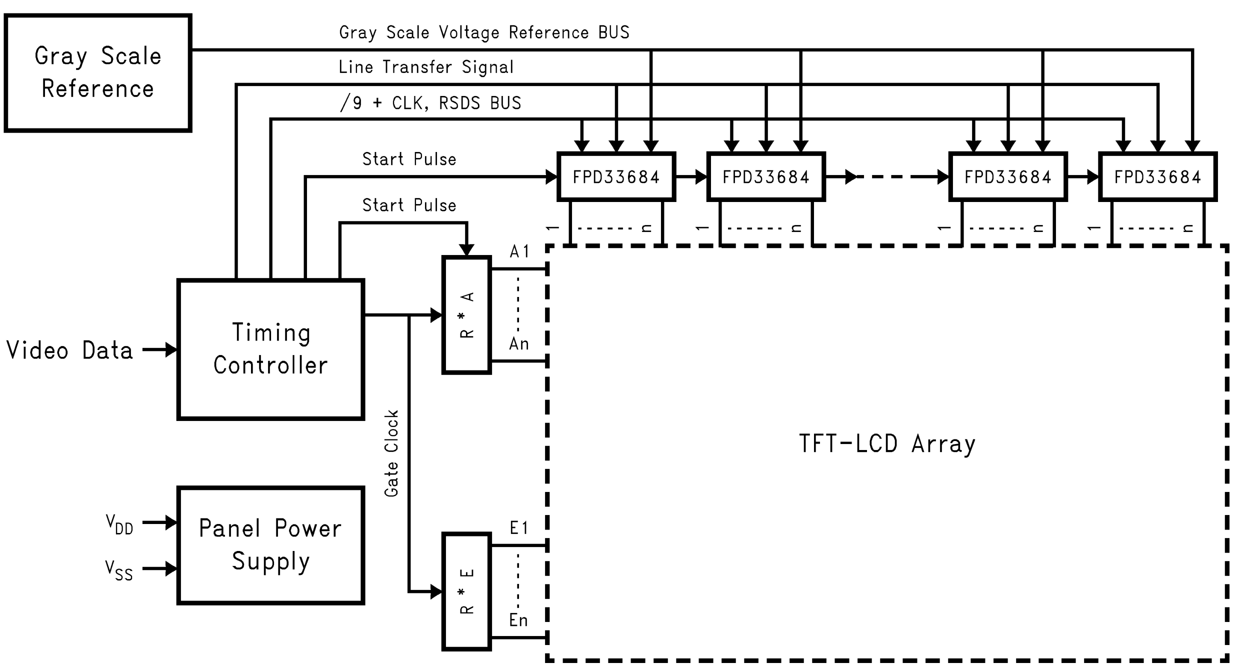
Features

- RSDS™ (Reduced Swing Differential Signaling) data bus for low power, reduced EMI and small PCB foot print
- Up to 85MHz clock
- Supports both XGA and SXGA timing
- Supports notebook and monitor applications
- Smart Charge Conservation for low power consumption
- 64 Gray levels per color (18-bit color)
- Supports both Dot and N-Line inversion
- Externally programmable gamma characteristic
- Very low offsets for artifact-free images
- High voltage outputs for high contrast in a large range of display panel applications
- Optional, high current, repair line buffers
- Available in 2 common gamma reference curves

Ordering Information			
Part Number	Gamma Curve	Custom TCP #	Package Suffix
FPD33684	A or B	XX(Note 1)	CT

Note 1: Custom TCP # is assigned by National Semiconductor for each custom TCP design

System Diagram



DS200113-1

 DS200113

Absolute Maximum Ratings (Note 2)

Analog Supply, (V_{DD2}) (Note 3)	−0.3V to +11.5V
Logic Supply, (V_{DD1}) (Note 3)	−0.3V to +5.0V
High Bias Supply, (V_{HBIAS}) (Note 3)	−0.3V to +13.0V
Low-Polarity RDAC Reference Voltages, (V_{GMA6} to V_{GMA10}) (Note 3)	−0.3V to 0.5V_{DD2}
High-Polarity RDAC Reference Voltages, (V_{GMA1} to V_{GMA5}) (Note 3)	0.5V_{DD2} − 1.0V to V_{DD2} + 0.3V
RDAC Current (All Gamma Voltage Taps), (I_{GMA} to I_{GMA10})	−2.5mA to 2.5mA
Input Voltage (Digital Logic), (V_{IN}) (Note 3)	−0.3V to V_{DD1} + 0.3V
Output Voltage, (V_{OUT}) (Note 3)	−0.3V to V_{DD2} + 0.3V
Output Current (Analog), (I_{OUT})	−7mA to +7mA
Storage Temperature Range, (T_S)	−55˚C to +125˚C

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 3: Absolute voltages referenced to V_{SS1} = V_{SS2} = 0.0V.

Recommended Operating Conditions

	Min	Typ	Max	Units
Logic Supply Voltage (V_{DD1})	2.7	3.3	3.6	V
Supply Voltage (V_{DD2})	7.5		10.5	V
Supply Voltage (V_{HBIAS})	V_{DD2}		V_{DD2}+1.5	V
Operating Temperature (T_A)	−10	+25	+70	˚C

DC Electrical Characteristics

Digital Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logic Input High Voltage		0.7 V_{DD1}			V
V_{IL}	Logic Input Low Voltage				0.3 V_{DD1}	V
V_{OH}	Logic Output High Voltage	I_{OH} = −0.5mA	V_{DD1} − 0.5			V
V_{OL}	Logic Output Low Voltage	I_{OL} = 0.5mA			0.5	V
I_{DD1}	Logic Current	(Note 4)		3.0	8.0	mA
I_{IH}	Input Leakage	V_{DD1} = 3.6V, V_{IN} = 3.6V	-1		1	µA
I_{IL}	Input Leakage	V_{DD1} = 3.6V, V_{IN} = 0V	-1		1	µA
C_{IN}	Input Capacitance	All logic pins		2		pF

Note 4: CLK frequency = 32.5 MHz, V_{DD1} = 3.3V, V_{SS1} = V_{SS2} = 0.0V, charge share time = 1.5µs, line time = 22µs.

RSDS Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIH_{RSDS}	RSDS™ High Input Voltage	VCM_{RSDS} = 1.2V (Note 5) see *Figure 1*	100	200		mV
VIL_{RSDS}	RSDS™ Low Input Voltage	VCM_{RSDS} = 1.2V (Note 5) see *Figure 1*		−200	−100	mV
VCM_{RSDS}	RSDS™ Common Mode Input Voltage Range	VIH_{RSDS} = +100mV, VIL_{RSDS} = −100mV (Note 6) see *Figure 1*	V_{SS1} + 0.1		V_{DD1} − 1.3	V
IDL	RSDS™ Input Leakage Current	DxxP, DxxN, CLKP, CLKN	−10		10	µA

Note 5: VCM_{RSDS} = (VCLKP + VCLKN)/2 or (VDxxP + VDxxN)/2.

Note 6: Positive means that DxxP (or CLKP) is higher than RSDS ground DxxN (or CLKN). Negative means that DxxP (or CLKP) is lower than RSDS ground DxxN (or CLKN).

RSDS Characteristics (Continued)

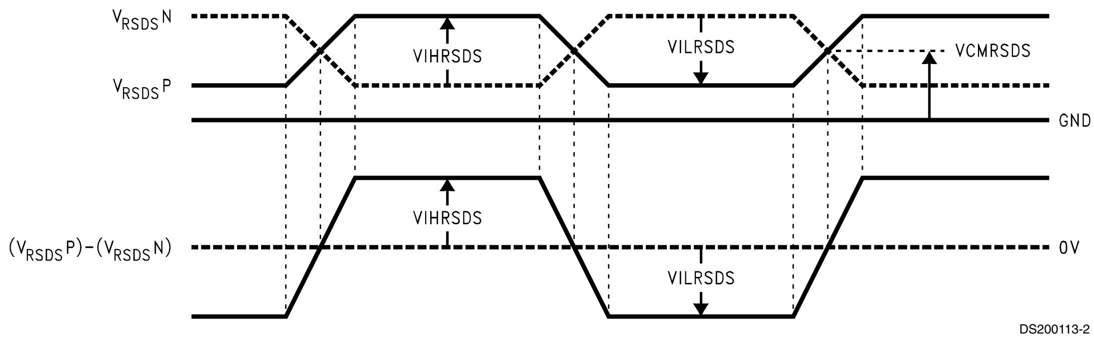


FIGURE 1. RSDS™ Signal Definition

Analog Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD2}	Supply Current Consumption	(Note 7)		3.0	8.0	mA
I_{HBIAS}	Current Consumption through HBIAS pin			1.25		mA
PD	Power Dissipation	(Note 7)		45		mW
V_{GMA1}	Upper RDAC High Side Input	(Note 8)	$V_{DD2}/2 + 0.2$		$V_{DD2} - 0.2$	V
V_{GMA5}	Upper RDAC Low Side Input	(Note 8)	$V_{DD2}/2 + 0.2$		$V_{DD2} - 0.2$	V
V_{GMA6}	Lower RDAC High Side Input	(Note 8)	0.2		$V_{DD2}/2 - 0.2$	V
V_{GMA10}	Lower RDAC Low Side Input	(Note 8)	0.2		$V_{DD2}/2 - 0.2$	V
V_{CS}	Charge Share Voltage		The Greater of V_{DD1} or V_{GMA6}		V_{GMA5}	V
C_{LOAD}	Output Capacitive Load		30		150	pF
V_{OUT}	Output Voltage Range		V_{SS2} + 0.2		$V_{DD2} - 0.2$	V
R_{DAC}	RDAC References (V_{GMA1} to V_{GMA5} and V_{GMA6} to V_{GMA10})	each	12.0	15.0	18.0	kΩ
V_{pperr}	Output Peak to Peak Error (gray levels 0 through 58)	$V_{GMA1} = V_{DD2} - 0.2V$ $V_{GMA10} = V_{SS2} + 0.2V$ (Note 9)		±3	±12	mV
	Output Peak to Peak Error (gray levels 59 through 63)			±5	±25	mV
$V_{parterr}$	Output Part to Part Error	(Note 10)			±5	mV
$I_{OUT\ RP}$	Repair Buffer Output Current	(Note 11)	±2	±3		mA

Note 7: V_{DD2} = 10.5V, V_{HBIAS} = 10.5V, V_{DD1} = 3.3V, DCLK = 65 MHz, R_{LOAD} = 5 kΩ, C_{LOAD} = 50 pF, charge share time = 1.5 µs, all other swinging between V_{GMA1} (= 8.0V) and V_{GMA10} (= 0.5V) with a line time = 22 µs.

Note 8: The following relationship must be maintained between the reference voltages: $V_{DD2} > V_{GMA1} > V_{GMA2} > V_{GMA3} > V_{GMA4} > V_{GMA5} > V_{GMA6} > V_{GMA7} > V_{GMA8} > V_{GMA9} > V_{GMA10} > V_{SS2}$

Note 9: V_{pperr} is defined as the error in peak-to-peak output voltage for each gray level when the output swings from the gray level high value (VHxx) to the gray level low value (VLxx). This parameter applies to every output on the die. The typical value represents one standard deviation from ideal based on final test data.

Note 10: $V_{parterr}$ is meant to guarantee the part to part output variation. The average of all outputs at gray level 32 is compared to a nominal gray level 32 value.

Note 11: Current into device pins is defined as positive. Current out of device pins is defined as negative. $|V_{OUT} - V_{IN}|$ > 500mV.

AC Electrical Characteristics

Digital AC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PW_{CLK}	Clock Period		11.7			ns
$PW_{CLK(L)}$	Low Clock Pulse Width		5			ns
$PW_{CLK(H)}$	High Clock Pulse Width		5			ns
t_{setup1}	RSDS Data Setup Time		2			ns
t_{hold1}	RSDS Data Hold Time		0			ns
t_{setup2}	ENIOx Setup Time		2			ns
t_{hold2}	ENIOx Hold Time		4			ns
t_{PLH1}	Start Pulse Fall Delay	C_{LINE} = 15 pF			8	ns
PW_{DIO}	ENIOx Pulse Width		1		2	T_{CLK}
PW_{CLK1}	LOAD Pulse Width		5 T_{CLK}		5µs	
t_{LDT}	Last Clock to LOAD Delay		5			T_{CLK}
t_{DENSU}	LOAD to First ENIO Setup		2			T_{CLK}
tPOL−CLK1	POL−CLK1 Time		14			ns

Analog AC Characteristics

Supplies: V_{SS1} = V_{SS2} = 0.0V, V_{DD1} = 3.3V, V_{DD2} = +9.5V, V_{HBIAS} = 11.0V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{settle\ 90\%}$	Output Settling Time to 90% of Final Value	*Figure 2* (Note 12)			6	µs
$t_{6\text{-bit accy}}$	Output Settling Time to 6-bit accuracy	*Figure 2* (Note 12)			10	µs
$t_{RP\ 90\%}$	Repair Line Output Settling Time to 90% of Final Value	C_{LOAD} = 150 pF, (Note 12)			6	µs
$t_{RP\ 6\text{-bit accy}}$	Repair Line Output Settling Time to 6-bit accuracy	C_{LOAD} = 150 pF, (Note 12)			10	µs

Note 12: Charge Share Time = 800ns, V_{GMA1} = 10.3V, V_{GMA10} = 0.2V, V_{GMA5} = 5.45V, V_{GMA6} = 5.05V.

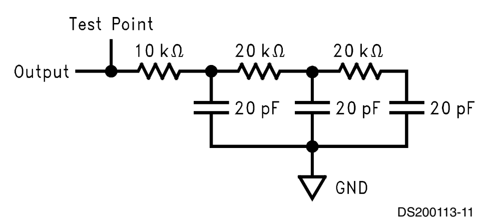
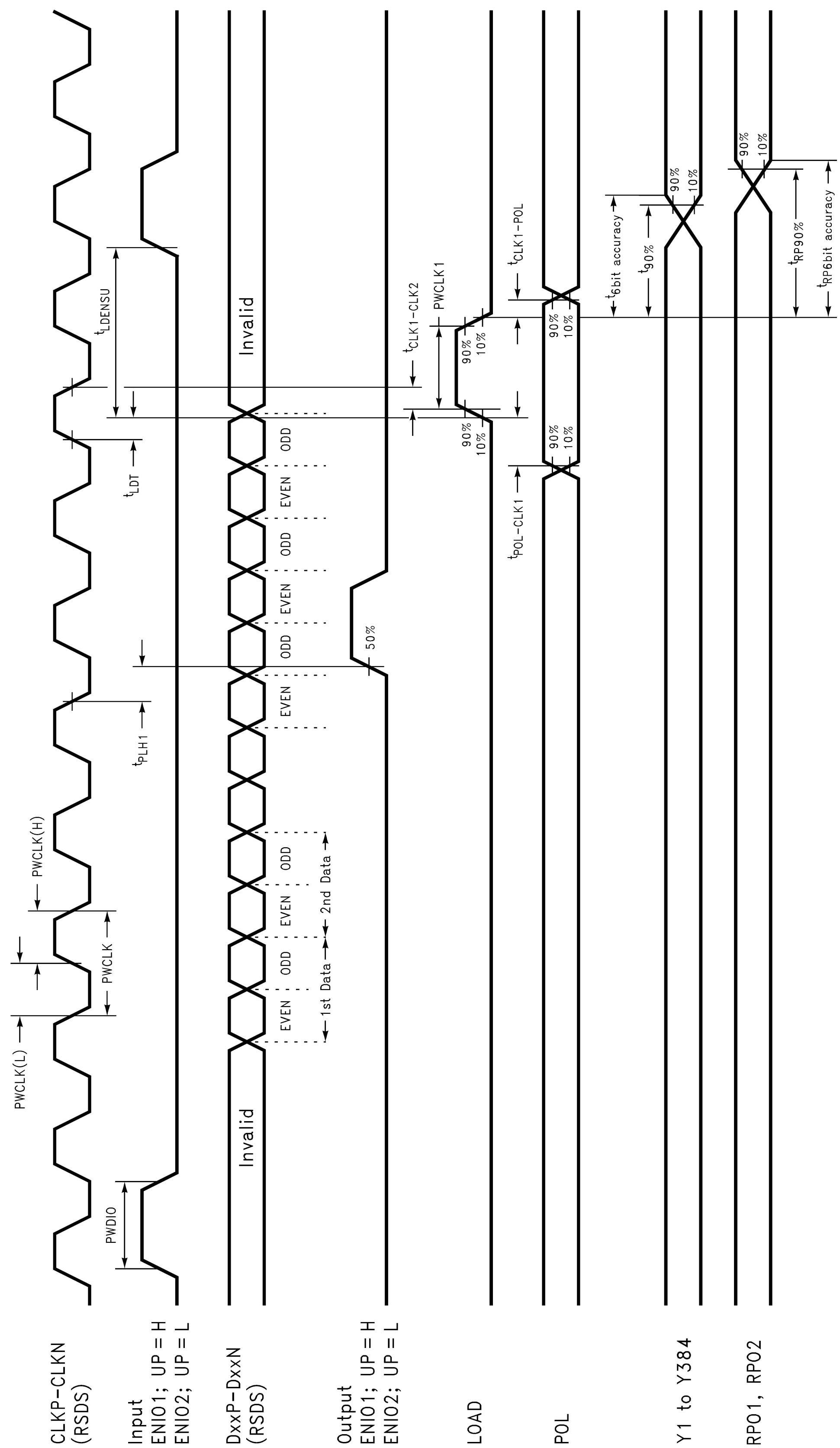


FIGURE 2. Test Circuit for Output Settling Time Measurements

Timing Diagrams



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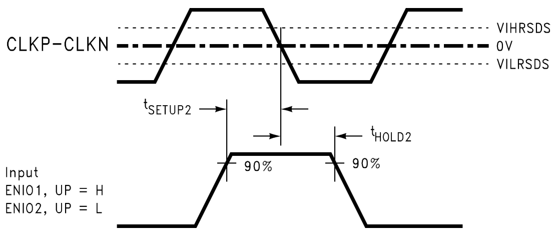
Timing Diagrams (Continued)



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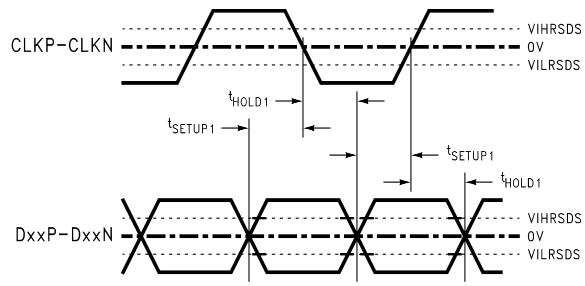

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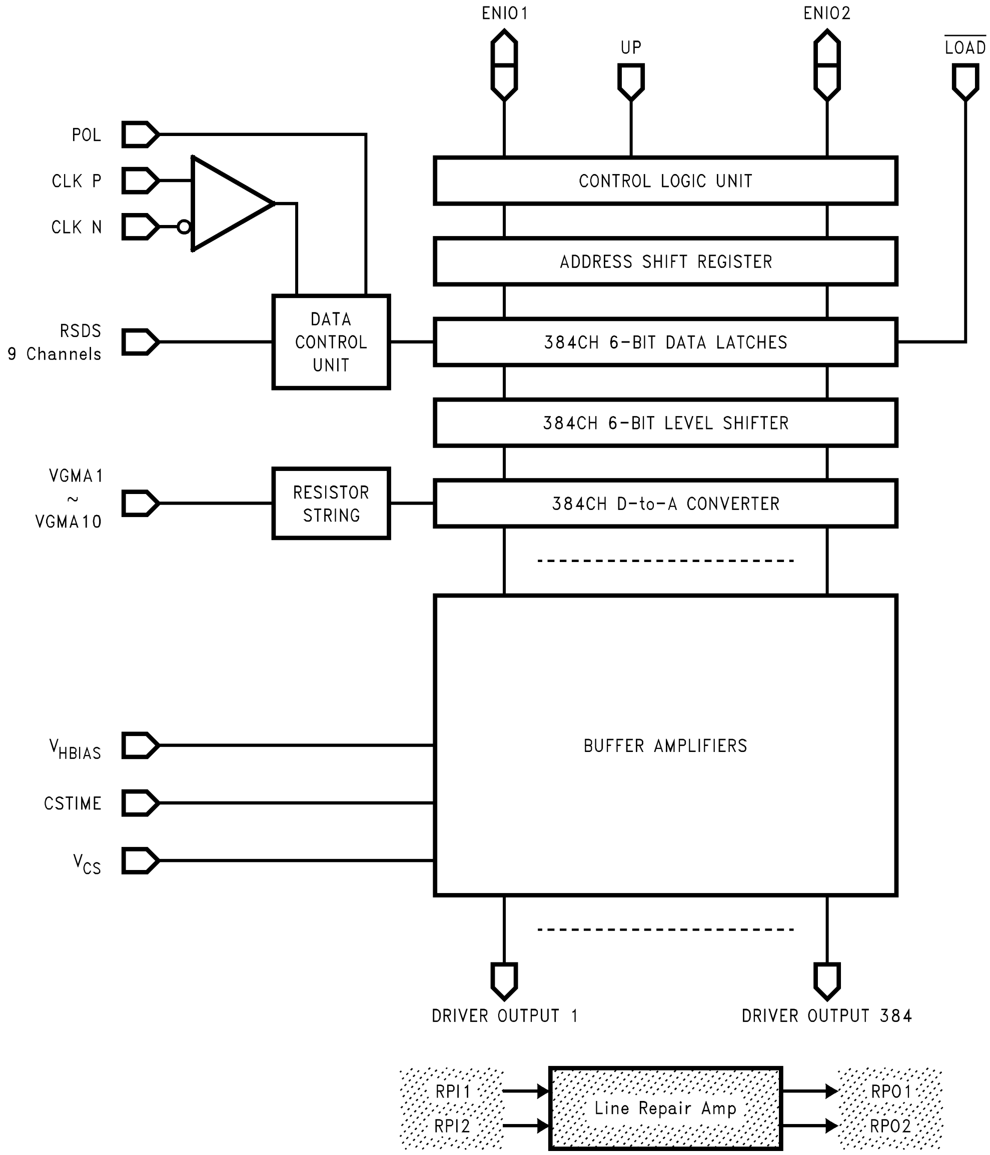
Block Diagram



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Functional Description

GENERAL OVERVIEW

The FPD33684 is a low power, low EMI, 384 output column driver with 64 gray level capability (6-bit). It provides direct drive for TFT-LCD displays, eliminating the need for V_{com} modulation. Direct drive significantly reduces system power consumption and also reduces component count while providing superior image quality and cross-talk margin. The FPD33684 utilizes National's *Charge Conservation Technology* that recovers energy stored in the capacitance of the column lines to reduce power consumption further.

The FPD33684 is designed for use in systems using dot inversion as the method of polarity inversion. Column inversion and N-line inversion are also supported. Other modes of polarity inversion including line inversion and frame inversion are not supported.

Digital video data inputs to the FPD33684 are received via a low power, low EMI Reduced Swing Differential Signaling (RSDS™) bus. The RSDS™ digital video commands one of 64 gray level voltages on each output. Output voltages are driven with individual high drive, low offset operational amplifiers. Data loading and line buffering is accomplished by means of an internal, bi-directional shift register.

GAMMA CORRECTION

The FPD33684 is designed to offer compatibility with a wide range of panel gamma characteristics. The output voltage is controlled by the digital data on the RSDS™ bus. Two identical R-DACs are used to program the output voltages. One R-DAC provides the high-polarity output voltages (voltages higher than V_{com}) and the other provides the low-polarity output voltages (voltages lower than V_{com}).

The FPD33684 is available with two R-DAC resistance curve options, both of which have been carefully designed to accurately match the natural, inverse gamma of a twisted nematic (TN) display with a 2.2 gamma transfer characteristic. A typical TN display, when operated with the FPD33684 drivers will produce a luminance with grayscale characteristics typical of CRT monitors. The R-DAC resistance values for the FPD33684A are shown in *Figure 3* and *Figure 4*. The

Functional Description (Continued)

R-DAC resistance values for the FPD33684B (designed to match the gamma curve of the Samsung S6C0666) are shown in *Figure 5* and *Figure 6*. Most applications will only need to provide references for each of the two ends of the two R-DACs (GMA1, GMA5, GMA6, and GMA10). Six additional, intemediate R-DAC tap points are available for further customization.

CHARGE CONSERVATION TECHNOLOGY

National Semiconductor's proprietary charge conservation technology significantly reduces power consumption. Charge conservation works by briefly switching all of the columns at the start of each line to a common node. This has the effect of redistributing the charge stored in the capacitance of the panel columns. Because half the columns are at voltages more positive than V_{com} and half are more negative, this redistribution of charge or "charge-sharing" has the effect of pulling all of the columns to a neutral voltage near the middle of the driver's dynamic range. Thus, the voltages on all the columns are driven approximately halfway toward their next value with no power expended. This dramatically reduces panel power dissipation (up to a theoretical limit of 50%) compared to conventional drivers which must drive each column through the entire voltage swing every time polarity is reversed.

'Smart' charge sharing is used to further optimize this feature. Data inversion is monitored and charge shared only across data ranges (when output polarity changes between adjacent lines). This is useful during n-line inversion when polarity changes do not occur at every line transition.

Charge sharing enables the FPD33684 to have faster output rise and fall times than drivers with convential amplifiers. This is due to the fact that the instantaneous currents supplied by the energy stored in the panel are much higher than the maximum output current of conventional drivers.

CSTIME — *CHARGE SHARE TIME*

The CSTIME pin allows the user to set the duration of charge-sharing mode based on the panel capacitance and resistance. The length of charge-sharing is important because it must be long enough to allow all of the columns to equalize to the same value in order to achieve optimum power performance. The length of charge-mode is user programmable. There are two common methods to drive the CSTIME pin.

The first method is to actively drive the CSTIME input with a control signal. This may be achieved by connecting the LOAD signal to the CSTIME input.The width of the LOAD/CSTIME signal determines the amount of time spent in charge-sharing. This width may be optimized for a particular panel load. A 'typical' width is 800ns. If desired, the CSTIME pin may be driven independently, however, this will require an additional output from the timing controller.

At the rising edge of the CSTIME/LOAD input signal, the outputs enter charge-sharing mode. Outputs remain in charge-mode until the falling edge of the CSTIME/LOAD signal.

A second method for setting charge-time is to connect a resistor (R_{CSTIME}) and capacitor (C_{CSTIME}) in parallel between the CSTIME pin and ground. Only one resistor and capacitor is required for the entire display. At the rising edge of the LOAD signal, the CSTIME pin is internally pulled to V_{DD1} and then released (i.e. floated). At this time the outputs enter charge-sharing mode. The voltage on the CSTIME pin, V_{CSTIME},will then decay toward GND at a rate determined by the R_{CSTIME} and C_{CSTIME} time constant. When V_{CSTIME} reaches $V_{DD1}/2$ the output mode switches from charge sharing to conventional amplifier drive mode. The charge-share mode time can be calculated using the following equation:

$t_{charge\text{-}share} = 0.69 \times R_{CSTIME} \times C_{CSTIME}$

RSDS™ DATA CHANNEL

The RSDS™ data bus is comprised of nine differential data pairs and a differential clock. The nine channels are organized as three busses of three channels each. Each three channel bus corresponds on one of the three video colors, red, green and blue. Because the clocking is dual edged, the even fields of the 6-bit word are transmitted-received on a first clock and are followed by the odd fields. One full pixel (red, green, and blue subpixels) is transmitted every full pixelclock cycle.

OPTIONAL LINE BUFFERS

The FPD33684 provides two general purpose, unity gain output buffers, one located at each end of the input bank of the die. These buffers may be used to repair an open column line. The drive signal from the output of the faulted line can be stitched to the input of the repair buffer during the repair process. The output of the repair buffer is then routed to the other side of the column line making it possible to maintain fast rise and fall times on both ends of the afflicted column line.

PIN DESCRIPTIONS

The pin order configuration for the FPD33684 is shown in *Figure 7*. Optional pins do not need to be carried off a custom TCP or COF package but may require a connection to a neighboring pad on the die by a tie on the tape.

CLKP and CLKN — *DATA CLOCK (INPUT)*

Differential clock input for RSDS™ data loading.

D00P–D22N — *RSDS™ DATA BUS (INPUT)*

D0xP–D0xN — Data for OUTPUTS 1,4,7...382 (red)

D1xP–D1xN — Data for OUTPUTS 2,5,8...383 (green)

D2xP–D2xN — Data for OUTPUTS 3,6,9...384 (blue)

Where x = 0 (LSB), 1 or 2 (MSB).

ENIO1/ENIO2 — *DATA LOADING ENABLE 1 AND 2 (I/O)*

The ENIO1/ ENIO2 pins are used to daisy chain the FPD33684 together with other FPD33684s. The first input in the chain is normally connected to the SP signal (or it's equivalent) on the timing controller. If UP = H, then the ENIO1 pin is configured as an input and the ENIO2 pin is configured as an output. If UP = L, then the ENIO2 pin is configured as an input and the ENIO1 pin is configured as an output.

INVERT — *DIGITAL DATA INVERT (INPUT)*

When INVERT = H, RSDS data is inverted. The INVERT pin can be tied either high or low through connection to a neighboring pin, eliminating the need to bring the pin off the package.

LOAD — *DATA LOAD* (INPUT)

The rising edge of LOAD copies the digital video buffered by the shift register into a second latch for conversion to analog. The outputs are forced into charge share mode while load is high. When CSTIME = LOAD the falling edge ends the charge share time and the newly converted analog voltages are driven by the outputs.

POL — *POLARITY (INPUT)*

Functional Description (Continued)

When POL = L, odd numbered outputs (1, 3, 5, ...383) are controlled by VGMA6 through VGMA10 and even numbered outputs are controlled by VGMA1 through VGMA5. When POL = H, odd numbered outputs are controlled by VGMA1 through VGMA5 and even numbered outputs are controlled by VGMA6 through VGMA10.

RPI1/ RPI2 — *REPAIR INPUT 1 AND 2 (INPUT)*

The input signal for the repair line buffers. These buffers are optional and when not used, the input should be tied to ground. The pin can be tied to ground through a local pin on the TCP, eliminating the need to bring the repair amp inputs or outputs off the TCP.

RPO1/ RPO2 — *REPAIR OUTPUT 1 AND 2 (OUTPUT)*

The output of the repair line buffers. These outputs are current buffered copies of their respective inputs.

UP — *DATA SHIFT DIRECTION — UP OR DOWN (INPUT)*

The UP pin controls the data shift direction. If UP is high then data is shifted “up” from output 1 to output 384, ENIO1 is configured as an input, and ENIO2 is an output. If UP is low then data is shifted “down” from output 384 to output 1, ENIO2 is an input, and ENIO1 is an output. The UP pin can be tied either high or low through connection to a neighboring pin, eliminating the need to bring the pin off the package.

CSTIME — *CHARGE SHARE TIME*

The CSTIME pin allows the user to set the duration of charge-sharing mode based on the panel capacitance and resistance.

V_{DD1} — *DIGITAL VOLTAGE SUPPLY*

Positive supply voltage for the digital logic functions of the driver.

V_{DD2} — *ANALOG VOLTAGE SUPPLY*

Positive supply voltage for the analog functions of the driver.

V_{GMA1}–V_{GMA10} — *RDAC REFERENCES (INPUTS)*

The reference voltages to the upper and lower RDACs used to control the inverse gamma transfer function of the driver.

Option - Any or all of the inputs V_{GMA2} through V_{GMA4} and V_{GMA7} through V_{GMA9} can be left undriven (floating).

V_{HBIAS} — *HIGH BIAS CURRENT VOLTAGE SUPPLY*

Optional positive supply voltage that provides a constant bias current to the output amplifiers to extend dynamic range. When separately provided, V_{HBIAS} must be 1.5V greater than V_{GMA1}. When not separately provided, V_{HBIAS} must be tied to V_{DD2}. In this configuration, V_{GMA1} must be held at or below V_{DD2} –1.5V.

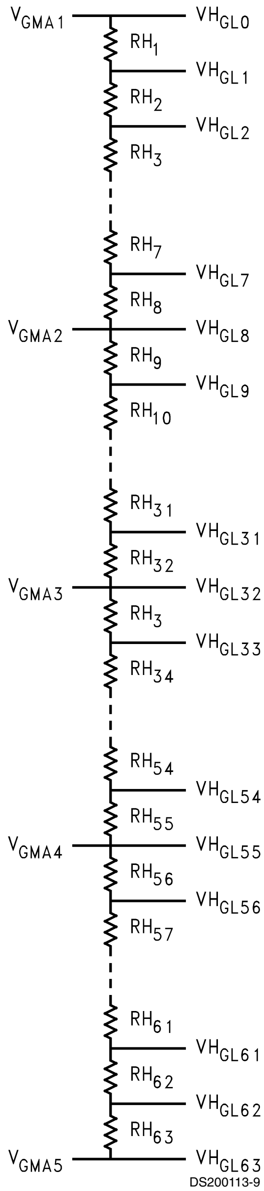
V_{SS1} — *DIGITAL GROUND*

Digital ground reference voltage.

V_{SS2} — *ANALOG GROUND*

Analog ground reference voltage.

Functional Description (Continued)



RH1	RDAC x 123/1008
RH2	RDAC x 69/1008
RH3	RDAC x 49/1008
RH4	RDAC x 42/1008
RH5	RDAC x 35/1008
RH6	RDAC x 28/1008
RH7	RDAC x 28/1008
RH8	RDAC x 21/1008
RH9	RDAC x 21/1008
RH10	RDAC x 14/1008
RH11	RDAC x 14/1008
RH12	RDAC x 10/1008
RH13	RDAC x 10/1008
RH14	RDAC x 9/1008
RH15	RDAC x 9/1008
RH16	RDAC x 8/1008
RH17	RDAC x 8/1008
RH18	RDAC x 8/1008
RH19	RDAC x 8/1008
RH20	RDAC x 8/1008
RH21	RDAC x 7/1008
RH22	RDAC x 7/1008
RH23	RDAC x 7/1008
RH24	RDAC x 7/1008
RH25	RDAC x 7/1008
RH26	RDAC x 7/1008
RH27	RDAC x 7/1008
RH28	RDAC x 7/1008
RH29	RDAC x 7/1008
RH30	RDAC x 7/1008
RH31	RDAC x 7/1008

RH32	RDAC x 7/1008
RH33	RDAC x 7/1008
RH34	RDAC x 7/1008
RH35	RDAC x 7/1008
RH36	RDAC x 7/1008
RH37	RDAC x 7/1008
RH38	RDAC x 7/1008
RH39	RDAC x 7/1008
RH40	RDAC x 7/1008
RH41	RDAC x 7/1008
RH42	RDAC x 7/1008
RH43	RDAC x 7/1008
RH44	RDAC x 8/1008
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RH46	RDAC x 8/1008
RH47	RDAC x 8/1008
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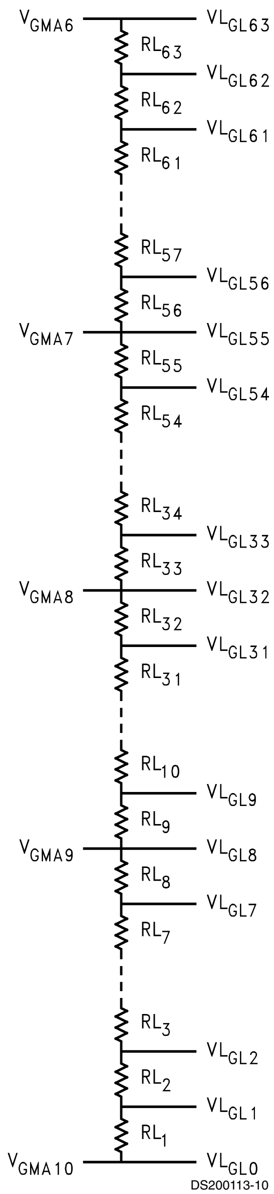
RH50	RDAC x 8/1008
RH51	RDAC x 9/1008
RH52	RDAC x 9/1008
RH53	RDAC x 10/1008
RH54	RDAC x 10/1008
RH55	RDAC x 10/1008
RH56	RDAC x 10/1008
RH57	RDAC x 13/1008
RH58	RDAC x 15/1008
RH59	RDAC x 17/1008
RH60	RDAC x 21/1008
RH61	RDAC x 35/1008
RH62	RDAC x 48/1008
RH63	RDAC x 62/1008

FIGURE 3. FPD33684A R-DAC Transfer Characteristic (continued in next figure)

Functional Description (Continued)



RL1	RDAC x 123/1008
RL2	RDAC x 69/1008
RL3	RDAC x 49/1008
RL4	RDAC x 42/1008
RL5	RDAC x 35/1008
RL6	RDAC x 28/1008
RL7	RDAC x 28/1008
RL8	RDAC x 21/1008
RL9	RDAC x 21/1008
RL10	RDAC x 14/1008
RL11	RDAC x 14/1008
RL12	RDAC x 10/1008
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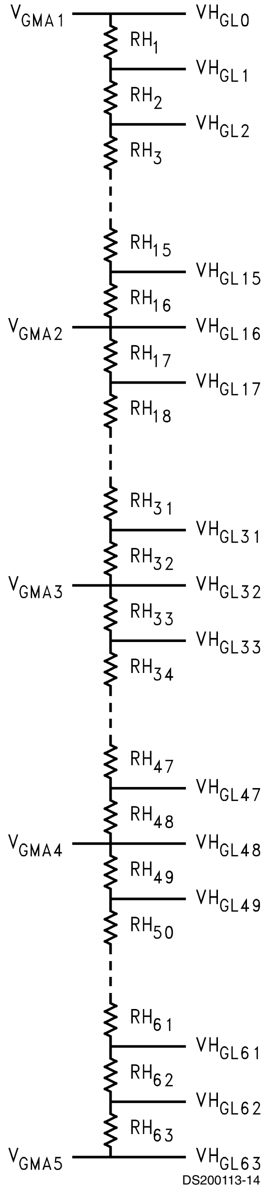
RL24	RDAC x 7/1008
RL25	RDAC x 7/1008
RL26	RDAC x 7/1008
RL27	RDAC x 7/1008
RL28	RDAC x 7/1008
RL29	RDAC x 7/1008
RL30	RDAC x 7/1008
RL31	RDAC x 7/1008

RL32	RDAC x 7/1008
RL33	RDAC x 7/1008
RL34	RDAC x 7/1008
RL35	RDAC x 7/1008
RL36	RDAC x 7/1008
RL37	RDAC x 7/1008
RL38	RDAC x 7/1008
RL39	RDAC x 7/1008
RL40	RDAC x 7/1008
RL41	RDAC x 7/1008
RL42	RDAC 7/1008
RL43	RDAC x 7/1008
RL44	RDAC x 8/1008
RL45	RDAC x 8/1008
RL46	RDAC x 8/1008
RL47	RDAC x 8/1008
RL48	RDAC x 8/1008
RL49	RDAC x 8/1008
RL50	RDAC x 8/1008
RL51	RDAC x 9/1008
RL52	RDAC x 9/1008
RL53	RDAC x 10/1008
RL54	RDAC x 10/1008
RL55	RDAC x 10/1008
RL56	RDAC x 10/1008
RL57	RDAC x 13/1008
RL58	RDAC x 15/1008
RL59	RDAC x 17/1008
RL60	RDAC x 21/1008
RL61	RDAC x 35/1008
RL62	RDAC x 48/1008
RL63	RDAC x 62/1008

FIGURE 4. FPD33684A R-DAC Transfer Characteristic (continued from prior figure)

Functional Description (Continued)

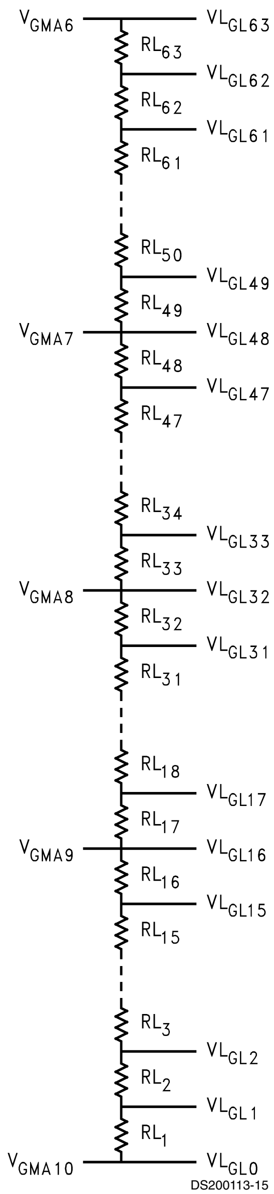


RH1	RDAC x 27/1008
RH2	RDAC x 27/1008
RH3	RDAC x 27/1008
RH4	RDAC x 27/1008
RH5	RDAC x 27/1008
RH6	RDAC x 27/1008
RH7	RDAC x 27/1008
RH8	RDAC x 27/1008
RH9	RDAC x 27/1008
RH10	RDAC x 27/1008
RH11	RDAC x 27/1008
RH12	RDAC x 27/1008
RH13	RDAC x 24/1008
RH14	RDAC x 24/1008
RH15	RDAC x 21/1008
RH16	RDAC x 20/1008
RH17	RDAC x 18/1008
RH18	RDAC x 18/1008
RH19	RDAC x 18/1008
RH20	RDAC x 17/1008
RH21	RDAC x 16/1008
RH22	RDAC x 15/1008
RH23	RDAC x 14/1008
RH24	RDAC x 14/1008
RH25	RDAC x 13/10078
RH26	RDAC x 13/1008
RH27	RDAC x 12/1008
RH28	RDAC x 12008
RH29	RDAC x 11/1008
RH30	RDAC x 11/1008
RH31	RDAC x 10/1008

RH32	RDAC x 10/1008
RH33	RDAC x 9/1008
RH34	RDAC x 9/1008
RH35	RDAC x 9/1008
RH36	RDAC x 9/1008
RH37	RDAC x 9/1008
RH38	RDAC x 9/1008
RH39	RDAC x 9/1008
RH40	RDAC x 9/1008
RH41	RDAC x 9/1008
RH42	RDAC x 9/1008
RH43	RDAC x 9/1008
RH44	RDAC x 9/1008
RH45	RDAC x 9/1008
RH46	RDAC x 9/1008
RH47	RDAC x 10/1008
RH48	RDAC x 10/1008
RH49	RDAC x 11/1008
RH50	RDAC x 12/1008
RH51	RDAC x 12/1008
RH52	RDAC x 13/1008
RH53	RDAC x 13/1008
RH54	RDAC x 14/1008
RH55	RDAC x 14/1008
RH56	RDAC x 16/1008
RH57	RDAC x 16/1008
RH58	RDAC x 17/1008
RH59	RDAC x 17/1008
RH60	RDAC x 18/1008
RH61	RDAC x 18/1008
RH62	RDAC x 18/1008
RH63	RDAC x 18/1008

FIGURE 5. FPD33684B R-DAC Transfer Characteristic (matches Samsung S6C0666) (continued in next figure)

Functional Description (Continued)

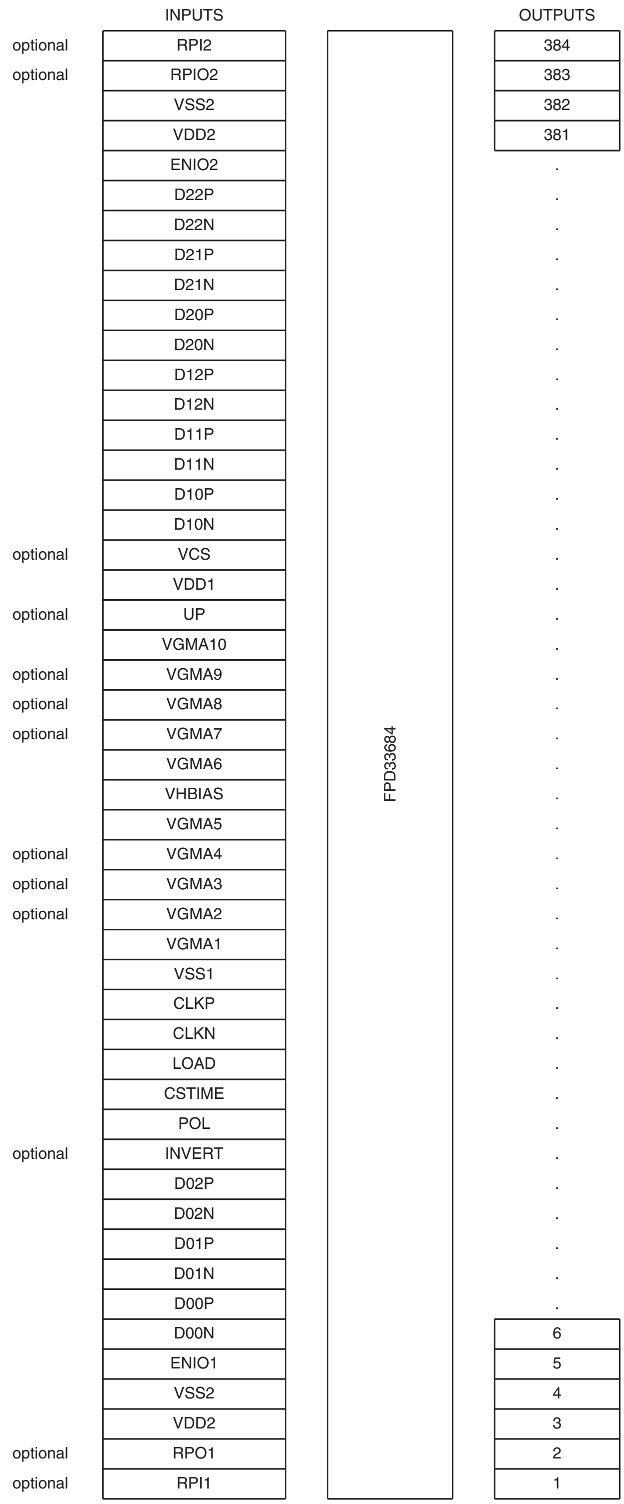


RL1	RDAC x 27/1008
RL2	RDAC x 27/1008
RL3	RDAC x 27/1008
RL4	RDAC x 27/1008
RL5	RDAC x 27/1008
RL6	RDAC x 27/1008
RL7	RDAC x 27/1008
RL8	RDAC x 27/1008
RL9	RDAC x 27/1008
RL10	RDAC x 27/1008
RL11	RDAC x 27/1008
RL12	RDAC x 27/1008
RL13	RDAC x 24/1008
RL14	RDAC x 24/1008
RL15	RDAC x 21/1008
RL16	RDAC x 20/1008
RL17	RDAC x 18/1008
RL18	RDAC x 18/1008
RL19	RDAC x 18/1008
RL20	RDAC x 17/1008
RL21	RDAC x 16/1008
RL22	RDAC x 15/1008
RL23	RDAC x 14/1008
RL24	RDAC x 14/1008
RL25	RDAC x 13/1008
RL26	RDAC x 13/1008
RL27	RDAC x 12/1008
RL28	RDAC x 12/1008
RL29	RDAC x 11/1008
RL30	RDAC x 11/1008
RL31	RDAC x 10/1008

RL32	RDAC x 10/1008
RL33	RDAC x 9/1008
RL34	RDAC x 9/1008
RL35	RDAC x 9/1008
RL36	RDAC x 9/1008
RL37	RDAC x 9/1008
RL38	RDAC x 9/1008
RL39	RDAC x 9/1008
RL40	RDAC x 9/1008
RL41	RDAC x 9/1008
RL42	RDAC x 9/1008
RL43	RDAC x 9/1008
RL44	RDAC x 9/1008
RL45	RDAC x 9/1008
RL46	RDAC x 9/1008
RL47	RDAC x 10/1008
RL48	RDAC x 10/1008
RL49	RDAC x 11/1008
RL50	RDAC x 12/1008
RL51	RDAC x 12/1008
RL52	RDAC x 13/1008
RL53	RDAC x 13/1008
RL54	RDAC x 14/1008
RL55	RDAC x 14/1008
RL56	RDAC x 16/1008
RL57	RDAC x 16/1008
RL58	RDAC x 17/1008
RL59	RDAC x 17/1008
RL60	RDAC x 18/1008
RL61	RDAC x 18/1008
RL62	RDAC x 18/1008
RL63	RDAC x 18/1008

FIGURE 6. FPD33684B R-DAC Transfer Characteristic (matches Samsung S6C0666) (conitnued from previous figure)

Functional Description (Continued)



Note: This figure represents a FPD33684 die oriented pad side up.

FIGURE 7. FPD33684 I/O Configuration

Packaging

The FPD33684 is available in TCP or as singulated die.

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