

## FPD33680 Low Power, Low EMI, TFT-LCD Column Driver with RSDS Inputs, 64 Grayshades, and 480 Outputs for SXGA/UXGA Applications

Check for Samples: [FPD33680](#)

### FEATURES

- **RSDS (Reduced Swing Differential Signaling) data bus for low power, reduced EMI and small PCB foot print**
- **85MHz maximum operating frequency at  $V_{DD1}=3.0V$**
- **RSDS pin location and RSDS Switch feature simplify PCB layout and improve EMI**
- **Ideal for UXGA notebook applications**
- **Smart Charge Conservation for low power consumption**
- **64 Gray levels per color (18-bit color)**
- **Supports both Dot and N-Line inversion**
- **Four externally programmable gamma curves**
- **Very low offsets for artifact free images**
- **Optional, high current, repair amplifiers**

### DESCRIPTION

The FPD33680 is a direct drive, 64 gray level, 480 output, TFT-LCD column driver with an RSDS™ data interface. It provides the capability to display 262,144 colors (18-bit color) with a large dynamic output range for twisted nematic applications. It is targeted to support SXGA applications up to a 75Hz refresh rate and UXGA applications up to a 60Hz refresh rate. Output voltages are gamma corrected to provide a direct mapping between digital video and LCD panel brightness.

An RSDS™ (Reduced Swing Differential Signaling) interface is used between the timing controller and the column driver to minimize EMI and reduce power.

The column driver with its interface offers a low power, low EMI column driver solution with direct-drive dynamic range and dot-inversion addressing.

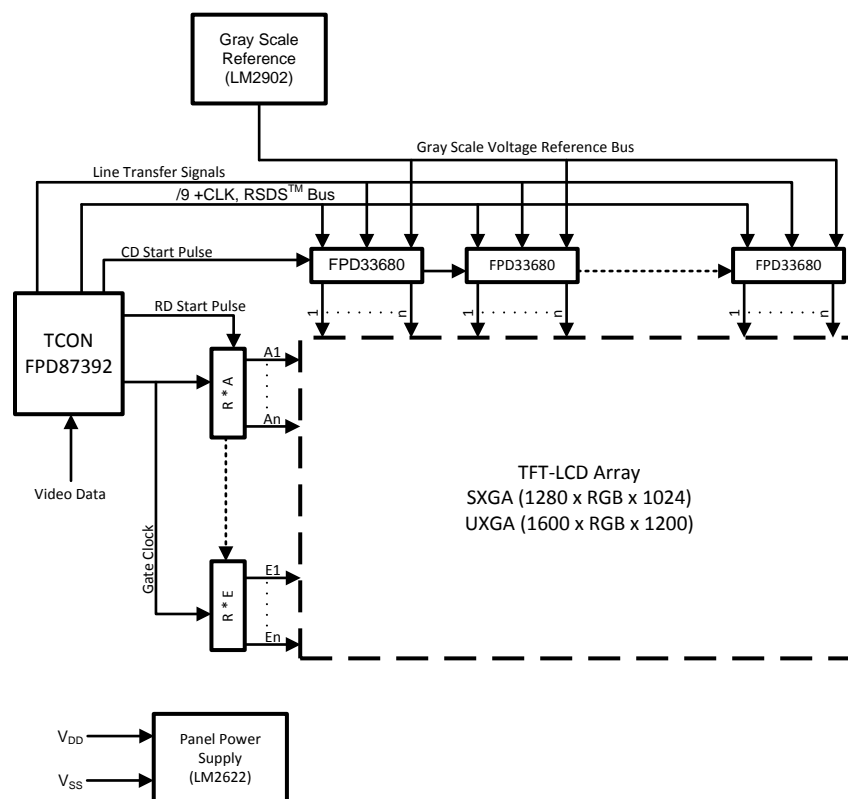


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## System Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings <sup>(1)</sup>

Analog Supply, ( $V_{DD2}$ ) <sup>(2)</sup>	-0.3V to +11.5V
Logic Supply, ( $V_{DD1}$ ) <sup>(2)</sup>	-0.3V to +5.0V
Low-Polarity RDAC Reference Voltages, ( $V_{GMA6}$ to $V_{GMA10}$ ) <sup>(2)</sup>	-0.3V to $0.5V_{DD2}$
High-Polarity RDAC Reference Voltages, ( $V_{GMA1}$ to $V_{GMA5}$ ) <sup>(2)</sup>	$0.5V_{DD2} - 1.0V$ to $V_{DD2} + 0.3V$
RDAC Current (All Gamma Voltage Taps), ( $I_{GMA}$ to $I_{GMA10}$ )	-2.5mA to 2.5mA
Input Voltage (Digital Logic), ( $V_{IN}$ ) <sup>(2)</sup>	-0.3V to $V_{DD1} + 0.3V$
Output Voltage, ( $V_{OUT}$ ) <sup>(2)</sup>	-0.3V to $V_{DD2} + 0.3V$
Output Current (Analog), ( $I_{OUT}$ )	-7mA to +7mA
Storage Temperature Range, ( $T_S$ )	-55°C to +125°C

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

(2) Absolute voltages referenced to  $V_{SS1} = V_{SS2} = 0.0V$ .

### Recommended Operating Conditions

	Min	Typ	Max	Units
Logic Supply Voltage ( $V_{DD1}$ )	3.0	3.3	3.6	V
Supply Voltage ( $V_{DD2}$ )	7.5		10.5	V
Operating Temperature				

**Recommended Operating Conditions (continued)**

	Min	Typ	Max	Units
(T <sub>A</sub> )	-10	+25	+70	°C

**DC Electrical Characteristics**  
**Digital Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IH}$	Logic Input High Voltage		$0.7 V_{DD1}$			V
$V_{IL}$	Logic Input Low Voltage				$0.3 V_{DD1}$	V
$V_{OH}$	Logic Output High Voltage	$I_{OH} = -0.5\text{mA}$	$V_{DD1} - 0.5$			V
$V_{OL}$	Logic Output Low Voltage	$I_{OL} = 0.5\text{mA}$			0.5	V
$I_{DD1}$	Logic Current	<sup>(1)</sup>		10.0	15.0	mA
$I_{IH}$	Input Leakage	$V_{DD1} = 3.6\text{V}, V_{IN} = 3.6\text{V}$	-1		1	$\mu\text{A}$
$I_{IL}$	Input Leakage	$V_{DD1} = 3.6\text{V}, V_{IN} = 0\text{V}$	-1		1	$\mu\text{A}$
$C_{IN}$	Input Capacitance	All logic pins		2		pF

(1) CLK frequency = 81MHz,  $V_{DD1} = 3.3\text{V}$ ,  $V_{SS1} = V_{SS2} = 0.0\text{V}$ , line time = 13.3 $\mu\text{s}$ , data = all 1's for 4 lines followed by all 0's for 4 lines.

### RSDS™ Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IH_{RSDS}}$	RSDS High Input Voltage	$V_{CM_{RSDS}} = 1.2V$ <sup>(1)</sup> see <a href="#">Figure 1</a>	100	200		mV
$V_{IL_{RSDS}}$	RSDS Low Input Voltage	$V_{CM_{RSDS}} = 1.2V$ <sup>(1)</sup> see <a href="#">Figure 1</a>		-200	-100	mV
$V_{CM_{RSDS}}$	RSDS Common Mode Input Voltage Range	$V_{IH_{RSDS}} = +100mV$ , $V_{IL_{RSDS}} = -100mV$ <sup>(2)</sup> see <a href="#">Figure 1</a>	$V_{SS1} + 0.1$		$V_{DD1} - 1.3$	V
IDL	RSDS Input Leakage Current	DxxP, DxxN, CLKP, CLKN	-10		10	$\mu A$

(1)  $V_{CM_{RSDS}} = (V_{CLKP} + V_{CLKN})/2$  or  $(V_{DxxP} + V_{DxxN})/2$ .

(2)  $V_{IH_{RSDS}}$  and  $V_{IL_{RSDS}}$  are referenced to  $V_{CM_{RSDS}}$

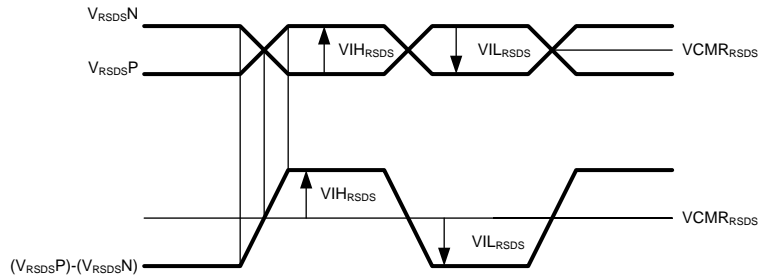


Figure 1. RSDS™ Signal Definition

## Analog Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{DD2}$	Supply Current Consumption	(1)		8.0	15.0	mA
$V_{GMA1}$	Upper RDAC High Side Input	(2)	$V_{DD2}/2 + 0.2$		$V_{DD2} - 0.2$	V
$V_{GMA5}$	Upper RDAC Low Side Input	(2)	$V_{DD2}/2 + 0.2$		$V_{DD2} - 0.2$	V
$V_{GMA6}$	Lower RDAC High Side Input	(2)	0.2		$V_{DD2}/2 - 0.2$	V
$V_{GMA10}$	Lower RDAC Low Side Input	(2)	0.2		$V_{DD2}/2 - 0.2$	V
$C_{LOAD}$	Output Capacitive Load		30		150	pF
$V_{OUT}$	Output Voltage Range		$V_{SS2} + 0.2$		$V_{DD2} - 0.2$	V
$R_{DAC}$	RDAC References ( $V_{GMA1}$ to $V_{GMA5}$ and $V_{GMA6}$ to $V_{GMA10}$ )	each	12.0	15.0	18.0	k $\Omega$
$V_{pperr}$	Output Peak to Peak Error (gray levels 0 through 58)	$V_{GMA1} = V_{DD2} - TBDV$ $V_{GMA10} = V_{SS2} + TBDV$ (3)		$\pm 3$	$\pm 10$	mV
	Output Peak to Peak Error (gray levels 59 through 63)			$\pm 5$	$\pm 15$	mV
$V_{parterr}$	Output Part to Part Error	(4)			$\pm 5$	mV
$I_{OUT RP}$	Repair Buffer Output Current	(5)	$\pm 2$	$\pm 3$		mA

- (1)  $V_{DD2} = 10V$ ,  $V_{DD1} = 3.3V$ ,  $f_{CLK} = 81MHz$ , line time = 13.3 $\mu$ sec, data = maximum output swing (GMA1 to GMA10), [TIME1, TIME0] = [0,1] (charge sharing of 32 clock cycles)
- (2) The following relationship must be maintained between the reference voltages:  $V_{DD2} > V_{GMA1} > V_{GMA2} > V_{GMA3} > V_{GMA4} > V_{GMA5} > V_{GMA6} > V_{GMA7} > V_{GMA8} > V_{GMA9} > V_{GMA10} > V_{SS2}$
- (3)  $V_{pperr}$  is meant to reflect the error in peak-to-peak output voltage for each gray level when the output swings from the high value  $V_{Hxx}$  to the low value  $V_{Lxx}$ . This parameter applies to every output on the die. The typical value represents one standard deviation from ideal based on tester data. The maximum value is a constraint of the test environment, not the performance of the part.
- (4)  $V_{parterr}$  is meant to guarantee the part-to-part output variation. The average of all outputs at gray level 32 is compared to a nominal gray level 32 value. The difference is  $V_{parterr}$
- (5) Current into device pins is defined as positive. Current out of device pins is defined as negative.  $|V_{OUT} - V_{IN}| > 500mV$ .

**AC Electrical Characteristics  
AC Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$PW_{CLK}$	Clock Period	$V_{DD1} = 3.0$ to $3.6V$	11.7			ns
$PW_{CLK(L)}$	Low Clock Pulse Width		40%		60%	$PW_{CLK}$
$PW_{CLK(H)}$	High Clock Pulse Width		40%		60%	$PW_{CLK}$
$t_{setup1}$	RSDS Data Setup Time		2			ns
$t_{hold1}$	RSDS Data Hold Time		0			ns
$t_{setup2}$	ENIOx Setup Time		2			ns
$t_{hold2}$	ENIOx Hold Time		4			ns
$t_{PLH1}$	Start Pulse Fall Delay	$C_{LINE} = 15$ pF			8	ns
$PW_{DIO}$	ENIOx Pulse Width		1		2	$PW_{CLK}$
$PW_{CLK1}$	LOAD Pulse Width		$5 T_{CLK}$		$5\mu s$	
$t_{LDT}$	Last Clock to LOAD Delay		1			$PW_{CLK}$
$t_{DENSU}$	LOAD to First ENIO Setup		2			$PW_{CLK}$
$t_{POL-CLK1}$	POL-CLK1 Time		14			ns

## Analog AC Characteristics

Supplies:  $V_{SS1} = V_{SS2} = 0.0V$ ,  $V_{DD1} = 3.3V$ ,  $V_{DD2} = +10.0V$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{\text{settle } 90\%}$	Output Settling Time to 90% of Final Value	Figure 2 <sup>(1)</sup>			6	$\mu\text{s}$
$t_{6\text{-bit accy}}$	Output Settling Time to 6-bit accuracy	Figure 2 <sup>(1)</sup>			10	$\mu\text{s}$
$t_{\text{RP } 90\%}$	Repair Line Output Settling Time to 90% of Final Value	$C_{\text{LOAD}} = 150 \text{ pF}$ , (1)			6	$\mu\text{s}$
$t_{\text{RP } 6\text{-bit accy}}$	Repair Line Output Settling Time to 6-bit accuracy	$C_{\text{LOAD}} = 150 \text{ pF}$ , (1)			10	$\mu\text{s}$

(1)  $V_{\text{GMA1}} = 9.8V$ ,  $V_{\text{GMA10}} = 0.2V$ ,  $V_{\text{GMA5}} = 5.2V$ ,  $V_{\text{GMA6}} = 4.8V$ ,  $[\text{TIME0}, \text{TIME1}] = [0, 1]$ .

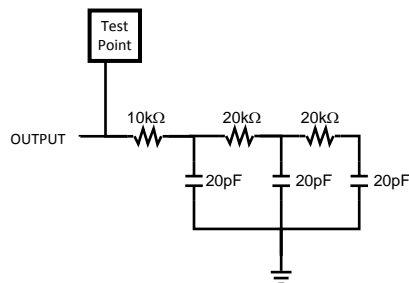
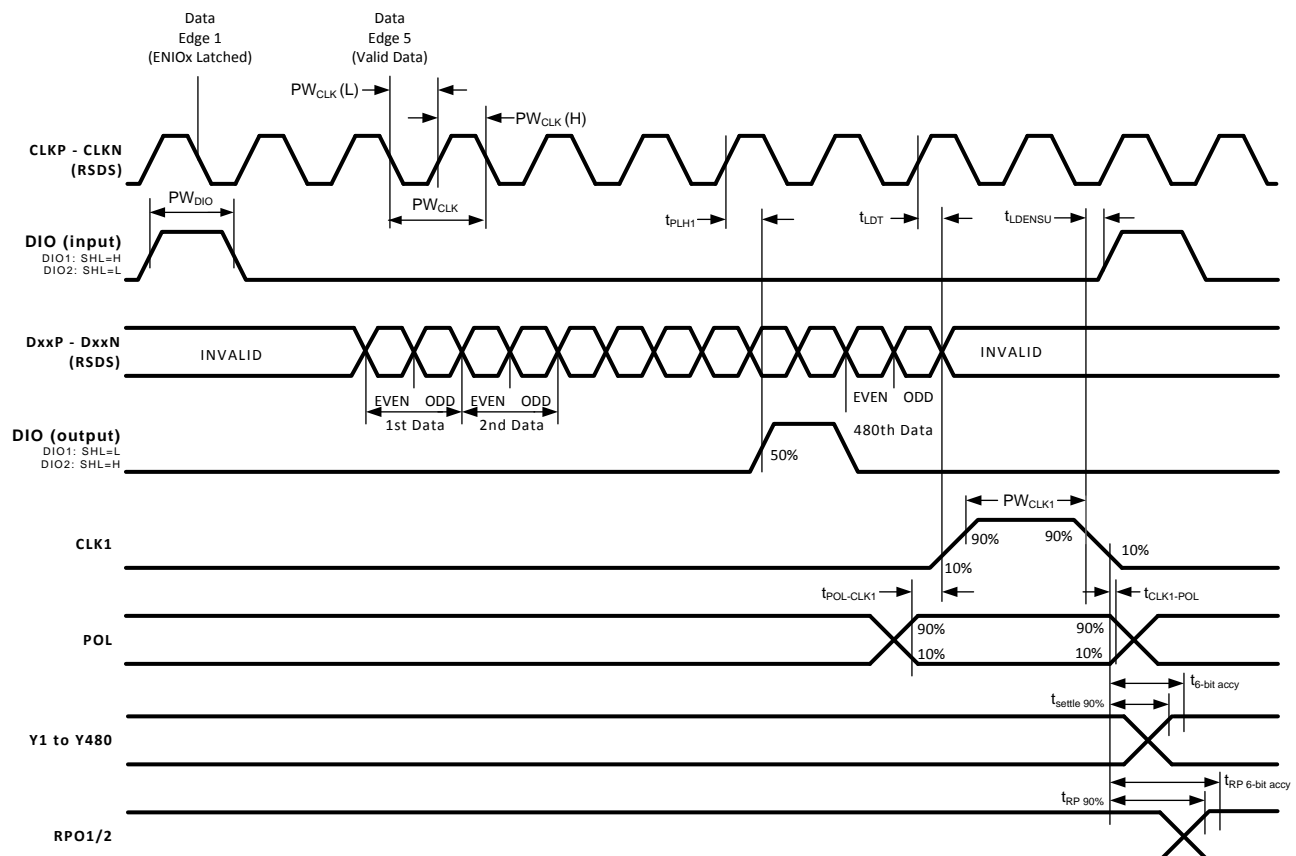
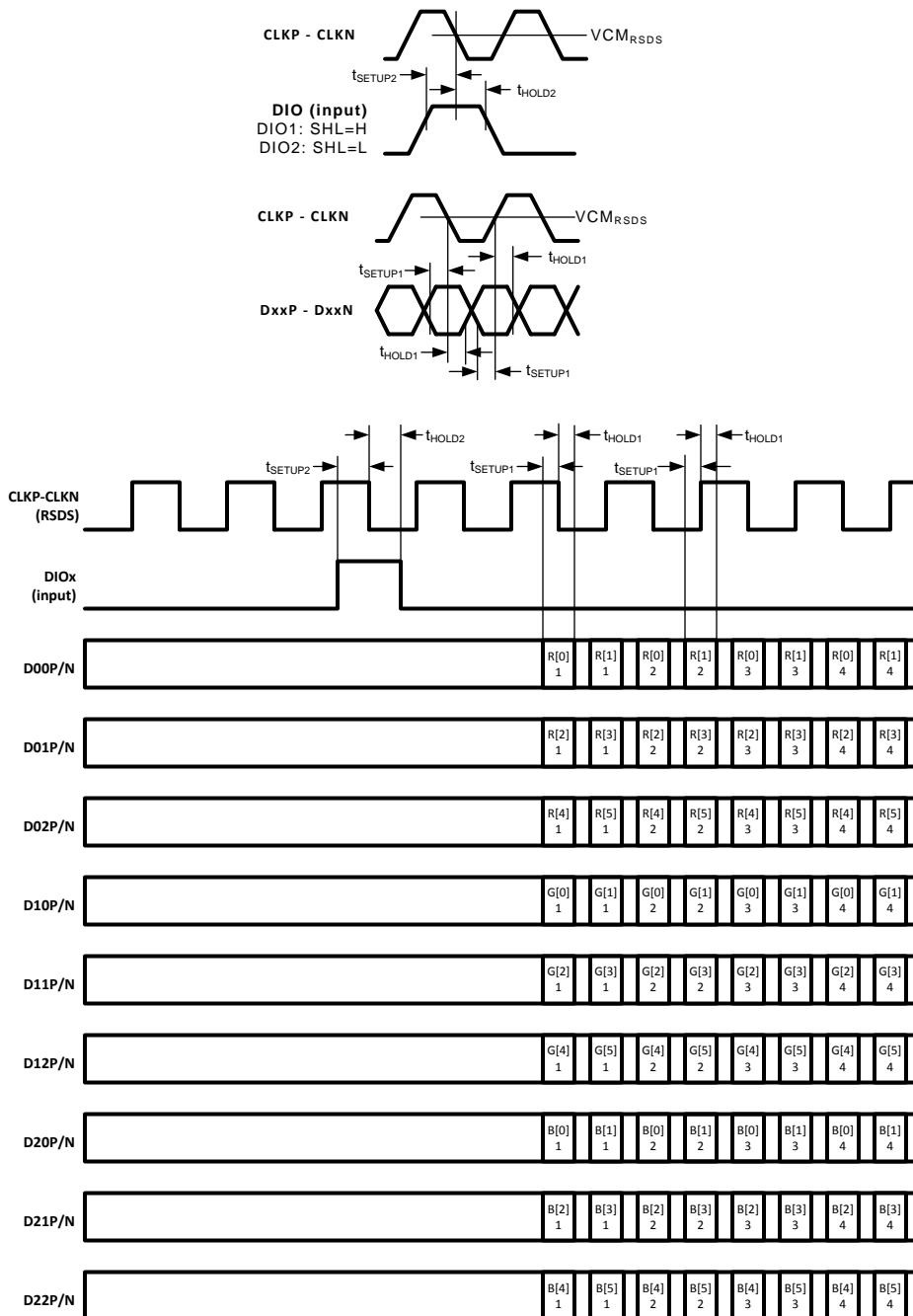


Figure 2. Test Circuit for Output Settling Time Measurements

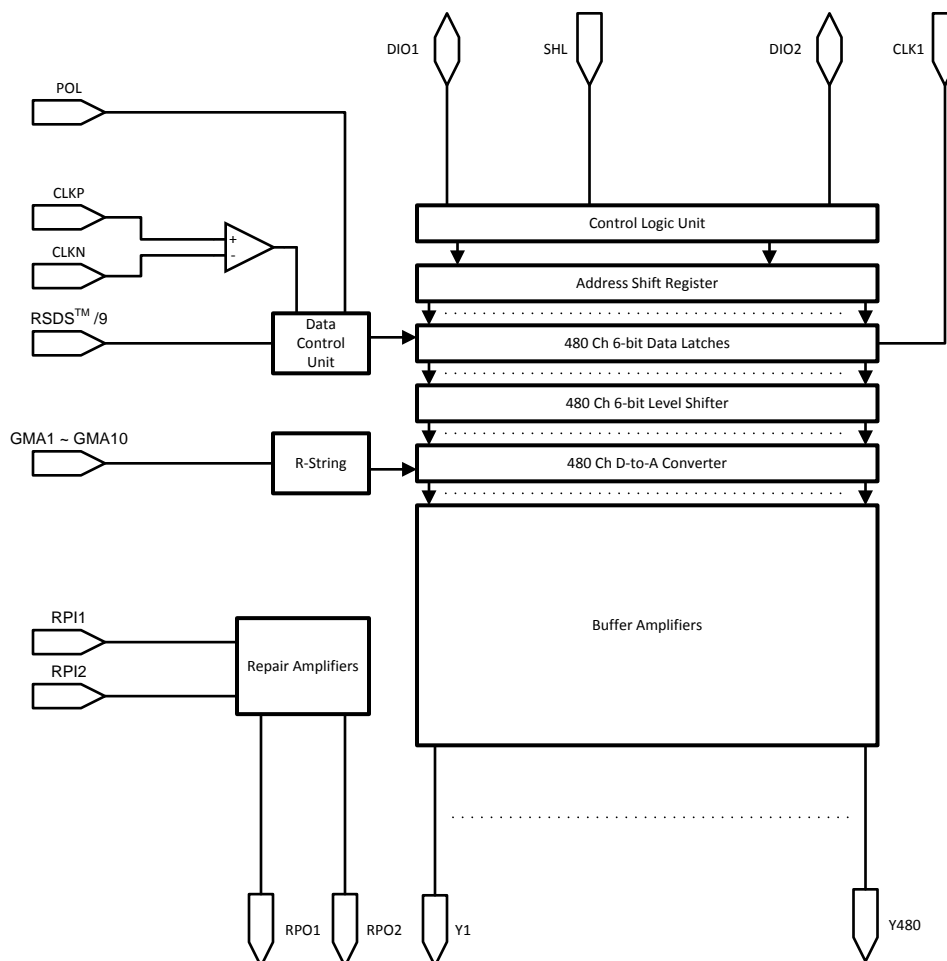
## Timing Diagrams







## Block Diagram



## Functional Description

### GENERAL OVERVIEW

The FPD33680 is a low power, low EMI, 480 output column driver with 64 gray level capability (6-bit). It provides direct drive for TFT-LCD displays, eliminating the need for  $V_{COM}$  modulation. Direct drive significantly reduces system power consumption and also reduces component count while providing superior image quality and cross-talk margin. The FPD33680 utilizes National's *Charge Conservation Technology* that recovers energy stored in the capacitance of the column lines to reduce power consumption further.

The FPD33680 is designed for use in systems using dot inversion. Column inversion and N-line inversion are also supported. Other modes of polarity inversion including line inversion and frame inversion are not supported.

Digital video data inputs to the FPD33680 are received using Reduced Swing Differential Signaling (RSDS™) receiver circuitry integrated into the column driver IC. The RSDS™ digital video commands one of 64 gray level voltages on each output. Output voltages are driven with individual high drive, low offset, operational amplifiers. Data loading and line buffering is accomplished by means of an internal, bi-directional shift register.

### GAMMA CORRECTION

The FPD33680 is designed to offer compatibility with a wide range of panel gamma characteristics. The output voltage levels corresponding to each of the 64 gray level commands can be externally adjusted to match the desired gamma characteristics of the display by means of two internal resistor-string DACs (RDACs). One RDAC provides the high-polarity output voltages (voltages higher than  $V_{com}$ ) and the other provides the low-polarity output voltages (voltages lower than  $V_{com}$ ).

The FPD33680 R-DAC resistance curve has been carefully designed to accurately match the natural, inverse gamma of a twisted nematic (TN) display with a 2.2 gamma transfer characteristic. Additional, custom gamma curves can be requested through your National Semiconductor representative. A typical TN display, when operated with the FPD33680 drivers will produce a luminance with grayscale characteristic typical of CRT monitors. The resistor values for the R-DAC are shown in Table 5. The individual R-DAC characteristics can be found in Figure 4, Table 3, and Table 4.

Most applications will only need to provide references for each of the two ends of the two R-DACs (GMA1, GMA5, GMA6, and GMA10). Six additional, intermediate R-DAC tap points are available for further customization.

**CHARGE CONSERVATION TECHNOLOGY**

National Semiconductor's proprietary charge conservation technology significantly reduces power consumption. Charge conservation works by briefly switching all of the columns to a common node at the start of each line. This has the effect of redistributing the charge stored in the capacitance of the panel columns. Because half the columns are at voltages more positive than  $V_{com}$  and half are more negative, this redistribution of charge or "charge-sharing" has the effect of pulling all of the columns to a neutral voltage near the middle of the driver's dynamic range. Thus, the voltages on all the columns are driven approximately halfway toward their next value with no power expended. This dramatically reduces panel power dissipation (up to a theoretical limit of 50%) compared to conventional drivers which must drive each column through the entire voltage swing every time polarity is reversed.

'Smart' charge sharing is used to further optimize this feature. Data inversion is monitored and charge shared only across data ranges (i.e. when output polarity changes between adjacent lines). This is useful during n-line inversion when polarity changes do not occur at every line transition.

As shown in Figure 3, charge sharing begins at the falling edge of CLK1 and continues for the number of RSDS clock cycles shown in Table 1. For more information on National's proprietary Smart Charge Sharing technology, please see application note AN1235 Using Smart Charge Sharing to Reduce Power and Boost Column Driver Performance, which is available on the National Semiconductor website or through your National Semiconductor representative.

The amount of charge share time is determined by 2 pins: TIME0 and TIME1. Both TIME0 and TIME1 pins default to a low state, so if both pins are left floating, the charge share time will be 16 RSDS clock cycles. The average panel should set charge sharing at either 32 RSDS clocks or 64 RSDS clocks, depending on the data rate and the panel load. Panels with much larger RC loads may need to increase the charge share time to get the maximum benefit and panels with a smaller load can realize power savings with a shorter charge share time. Please contact National Semiconductor if you need further assistance in selecting a charge share time.

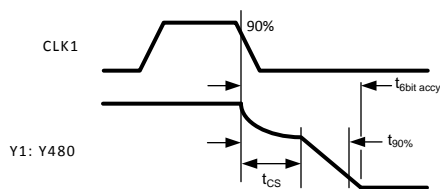


Figure 3. FPD33680 Charge Share Timing

Table 1. Charge Sharing Definition

TIME0	TIME1	Charge Share Time
0	0	16 RSDS CLKs (approx. 250ns @ 65MHz)
0	1	32 RSDS CLKs (approx. 500ns @ 65MHz)
1	0	64 RSDS CLKs (approx. 1µs @ 65MHz)
1	1	128 RSDS CLKs (approx. 2µs @ 65MHz)

## ***RSDS DATA CHANNEL***

The RSDS data bus is comprised of nine channels and a common clock. Each channel consists of a two wire differential pair. The nine channels carry digital video data organized as three busses of three channels. Each three channel bus corresponds on one of the three video colors, red, green and blue. The three video busses are comprised of a most, middle and least significant bit. The six bit video word is carried on the three wires of each video bus in two consecutive half words. The even fields of the word are transmitted-received on a first clock and are followed by the odd fields on the following clock transition. Clocking is dual edge and the clock signal is also carried on a two wire, differential pair.

## ***PIN SWAP AND PIN ORDER***

The FPD33680 comes with advanced features to simplify the PCB routing and reduce EMI. The first improvement is the organization of the input pins. In the industry standard RSDS pinout, the RSDS bus is split into 3 sections across the inputs and is interrupted by power and ground signals as well as TTL level signals. The FPD33680 groups all of the RSDS signals together. The power and gamma inputs are grouped together and the low speed TTL signals are grouped together. This makes PCB routing easier. The second feature is the RSDS Swap. This allows the number of corners in the RSDS bus to be cut in half. From one column driver to the next, the order of the RSDS input pins is reversed, allowing the RSDS bus to be routed more efficiently. The pin definitions are shown in [Table 2](#).

## ***OPTIONAL REPAIR AMPLIFIERS***

The FPD33680 provides two general purpose, unity gain output buffers, one located at each end of the input bank of the die. These buffers may be used to repair an open in a column line. The drive signal from the output of the faulted line can be stitched to the input of the repair buffer during the repair process. The output of the repair buffer is then routed to the other side of the column line making it possible to maintain fast rise and fall times on both ends of the afflicted column line.

## ***PIN DESCRIPTIONS***

The pin order configuration for the FPD33680 is shown in [Table 6](#).

### **CLKP and CLKN—Data Clock (input)**

Differential clock input for RSDS™ data loading. Note that when RSDS\_SW is tied to  $V_{SS1}$ , the polarity of CLKP and CLKN is reversed (i.e. the CLKP input should be connected to the TCON CLKN output and the CLKN input should be connected to the TCON CLKP output).

### **RSDS\_SW—RSDS Swap (Input)**

The RSDS\_SW pin controls the definition of the RSDS data input pins to provide for optimal PCB routing. When tied to  $V_{DD1}$  or left floating, the RSDS input pins are in their default state. When the RSDS\_SW pin is tied to  $V_{SS2}$ , the input pins are in their alternate configuration as shown in [Table 2](#)

### **DxxP/N—RSDS Data Bus (input)**

RSDS™ data input pins. The definitions are controlled by the state of the RSDS\_SW pin as shown in [Table 2](#). Note that the polarity of the RSDS signals also reverses (i.e. CLKP—CLKN).

**Table 2. RSDS Input Pin Configuration**

RSDS™ Input	RSDS_SW = NC or $V_{DD1}$	RSDS_SW = $V_{SS}$
RSDS0P	BLUE[2]P	NC
RSDS0N	BLUE[2]N	NC
RSDS1P	BLUE[1]P	NC
RSDS1N	BLUE[1]N	NC
RSDS2P	BLUE[0]P	NC
RSDS2N	BLUE[0]N	NC
RSDS3P	GREEN[2]P	RED[0]N
RSDS3N	GREEN[2]N	RED[0]P
RSDS4P	GREEN[1]P	RED[1]N

**Table 2. RSDS Input Pin Configuration (continued)**

RSDS4N	GREEN[1]N	RED[1]P
RSDS5P	GREEN[0]P	RED[2]N
RSDS5N	GREEN[0]N	RED[2]P
CLKP	CLKP	CLKN
CLKN	CLKN	CLKP
RSDS6P	RED[2]P	GREEN[0]N
RSDS6N	RED[2]N	GREEN[0]P
RSDS7P	RED[1]P	GREEN[1]N
RSDS7N	RED[1]N	GREEN[1]P
RSDS8P	RED[0]P	GREEN[2]N
RSDS8N	RED[0]N	GREEN[2]P
RSDS9P	NC	BLUE[0]N
RSDS9N	NC	BLUE[0]P
RSDS10P	NC	BLUE[1]N
RSDS10N	NC	BLUE[1]P
RSDS11P	NC	BLUE[2]N
RSDS11N	NC	BLUE[2]P

**CLK1—Data Load (input)**

The rising edge of CLK1 copies the digital video buffered by the shift register into a second latch for conversion to analog. The falling edge of CLK1 begins charge sharing.

**POL—Polarity (input)**

When POL is low, odd numbered outputs (1, 3, 5, . . . 383) are controlled by VGMA6 through VGMA10 and even numbered outputs are controlled by VGMA1 through VGMA5. When POL is high, odd numbered outputs are controlled by VGMA1 through VGMA5 and even numbered outputs are controlled by VGMA6 through VGMA10. The POL signal for line #n is sampled at the rising edge of CLK1 on line # n-1.

**DIO1/DIO2—Data Loading Enable 1 and 2 (I/O)**

The DIO1 and DIO2 pins allow several FPD33680 column drivers to be daisy chained together. The start pulse (SP or STH) from the timing controller is connected to the input DIOx pin on the first column driver in the chain. The input DIO for the remaining column drivers in the chain are connected to the output DIO from the preceding column driver. The SHL pin controls whether DIO1 or DIO2 is configured as the input.

If SHL is high, then the DIO1 pin is configured as an input and the DIO2 pin as an output. If SHL is low, the DIO2 pin is configured as an input and the DIO1 pin as an output.

The input DIOx pin is latched on the falling edge of the CLKP signal.

**DATPOL—Digital Data Invert (input)**

When DATPOL is high, RSDS data is inverted. The DATPOL pin can be tied either high or low through connection to a neighboring pin on a custom package eliminating the need to connect the pin to the PCB.

**SHL—Data Shift Direction (input)**

The SHL pin controls the data load direction. When SHL is high, the data is loaded from output 1 to output 480, DIO1 is configured as an input, and DIO2 is configured as an output. When SHL is low, the data is loaded from output 480 to output 1, DIO2 is configured as an input, and DIO1 is configured as an output. The SHL pin can be tied off in the custom package, eliminating the need to connect it to the PCB.

**RPI1/ RPI2—Repair Amp Input 1 and 2 (input)**

The input signal for the repair line buffers. These buffers are optional and when not used, the input should be tied to ground. RPI1 and RPI2 can be tied to ground with a connection in the package, eliminating the need to connect them to the PCB.

**RPO1/ RPO2—Repair Amp Output 1 and 2 (output)**

The output of the repair line buffers. These outputs are current buffered copies of their respective inputs. When not in use, RPO1 and RPO2 can be left unconnected.

**TIME0/ TIME1**—*Charge Share Time Select Pins (input)*

The TIME0 and TIME1 pins define the length of charge share time. [Table 1](#) lists the charge share time options defined by TIME0 and TIME1. Both of these pins have internal pull-down resistors and default to a logic low state. They can also be tied high in the package, eliminating the need to connect them to the PCB.

**V<sub>GMA1</sub>–V<sub>GMA10</sub>**—*RDAC References (input)*

The reference voltages to the upper and lower RDACs used to control the inverse gamma transfer function of the driver.

Option - Any or all of the inputs V<sub>GMA2</sub> through V<sub>GMA4</sub> and V<sub>GMA7</sub> through V<sub>GMA9</sub> can be left undriven (floating).

**V<sub>DD1</sub>**—*Digital Voltage Supply (power)*

Positive supply voltage for the digital logic functions of the driver. Nominally 3.3V.

**V<sub>DD2</sub>**—*Analog Voltage Supply (power)*

Positive supply voltage for the analog functions of the driver. Nominally between 8.0 and 10.0V

**V<sub>SS1</sub>**—*Digital Ground (power)*

Digital ground reference voltage. Typically tied to V<sub>SS2</sub> on the PCB.

**V<sub>SS2</sub>**—*Analog Ground (power)*

Analog ground reference voltage. Typically tied to V<sub>SS1</sub> on the PCB

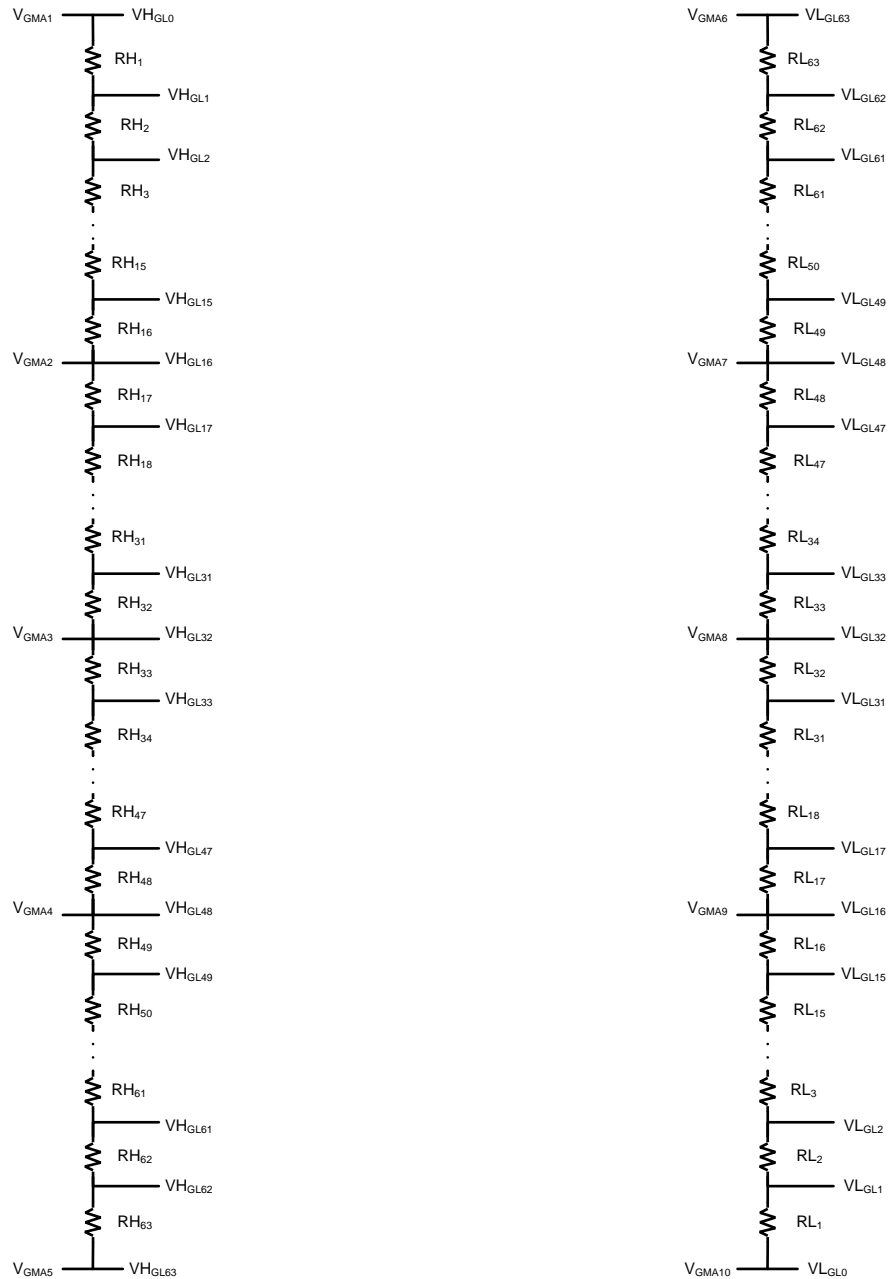


Figure 4. FPD33680F R-DAC Configuration

Table 3. FPD33680F Lower Gamma Voltages

Data	Output Voltage (gamma F)			Data	Output Voltage (gamma F)		
00 <sub>H</sub>	VL0	VGMA10		20 <sub>H</sub>	VL32	VGMA8	
01 <sub>H</sub>	VL1	VGMA9-(VGM A9-VGMA10) <sub>x</sub>	5536/6459	21 <sub>H</sub>	VL33	VGMA7-(VGM A7-VGMA8) <sub>x</sub>	1710/1829
02 <sub>H</sub>	VL2	VGMA9-(VGM A9-VGMA10) <sub>x</sub>	4762/6459	22 <sub>H</sub>	VL34	VGMA7-(VGM A7-VGMA8) <sub>x</sub>	1591/1829
03 <sub>H</sub>	VL3	VGMA9-(VGM A9-VGMA10) <sub>x</sub>	4152/6459	23 <sub>H</sub>	VL35	VGMA7-(VGM A7-VGMA8) <sub>x</sub>	1472/1829

**Table 3. FPD33680F Lower Gamma Voltages (continued)**

<b>04<sub>H</sub></b>	VL4	VGMA9-(VGM A9-VGMA10)x	3542/6459	<b>24<sub>H</sub></b>	VL36	VGMA7-(VGM A7-VGMA8)x	1353/1829
<b>05<sub>H</sub></b>	VL5	VGMA9-(VGM A9-VGMA10)x	3081/6459	<b>25<sub>H</sub></b>	VL37	VGMA7-(VGM A7-VGMA8)x	1249/1829
<b>06<sub>H</sub></b>	VL6	VGMA9-(VGM A9-VGMA10)x	2620/6459	<b>26<sub>H</sub></b>	VL38	VGMA7-(VGM A7-VGMA8)x	1145/1829
<b>07<sub>H</sub></b>	VL7	VGMA9-(VGM A9-VGMA10)x	2159/6459	<b>27<sub>H</sub></b>	VL39	VGMA7-(VGM A7-VGMA8)x	1041/1829
<b>08<sub>H</sub></b>	VL8	VGMA9-(VGM A9-VGMA10)x	1846/6459	<b>28<sub>H</sub></b>	VL40	VGMA7-(VGM A7-VGMA8)x	937/1829
<b>09<sub>H</sub></b>	VL9	VGMA9-(VGM A9-VGMA10)x	1533/6459	<b>29<sub>H</sub></b>	VL41	VGMA7-(VGM A7-VGMA8)x	833/1829
<b>0A<sub>H</sub></b>	VL10	VGMA9-(VGM A9-VGMA10)x	1265/6459	<b>2A<sub>H</sub></b>	VL42	VGMA7-(VGM A7-VGMA8)x	714/1829
<b>0B<sub>H</sub></b>	VL11	VGMA9-(VGM A9-VGMA10)x	997/6459	<b>2B<sub>H</sub></b>	VL43	VGMA7-(VGM A7-VGMA8)x	595/1829
<b>0C<sub>H</sub></b>	VL12	VGMA9-(VGM A9-VGMA10)x	774/6459	<b>2C<sub>H</sub></b>	VL44	VGMA7-(VGM A7-VGMA8)x	476/1829
<b>0D<sub>H</sub></b>	VL13	VGMA9-(VGM A9-VGMA10)x	551/6459	<b>2D<sub>H</sub></b>	VL45	VGMA7-(VGM A7-VGMA8)x	357/1829
<b>0E<sub>H</sub></b>	VL14	VGMA9-(VGM A9-VGMA10)x	358/6459	<b>2E<sub>H</sub></b>	VL46	VGMA7-(VGM A7-VGMA8)x	238/1829
<b>0F<sub>H</sub></b>	VL15	VGMA9-(VGM A9-VGMA10)x	179/6459	<b>2F<sub>H</sub></b>	VL47	VGMA7-(VGM A7-VGMA8)x	119/1829
<b>10<sub>H</sub></b>	VL16	VGMA9		<b>30<sub>H</sub></b>	VL48	VGMA7	
<b>11<sub>H</sub></b>	VL17	VGMA8-(VGM A8-VGMA9)x	1950/2114	<b>31<sub>H</sub></b>	VL49	VGMA6-(VGM A6-VGMA7)x	4481/4600
<b>12<sub>H</sub></b>	VL18	VGMA8-(VGM A8-VGMA9)x	1801/2114	<b>32<sub>H</sub></b>	VL50	VGMA6-(VGM A6-VGMA7)x	4347/4600
<b>13<sub>H</sub></b>	VL19	VGMA8-(VGM A8-VGMA9)x	1652/2114	<b>33<sub>H</sub></b>	VL51	VGMA6-(VGM A6-VGMA7)x	4198/4600
<b>14<sub>H</sub></b>	VL20	VGMA8-(VGM A8-VGMA9)x	1503/2114	<b>34<sub>H</sub></b>	VL52	VGMA6-(VGM A6-VGMA7)x	4049/4600
<b>15<sub>H</sub></b>	VL21	VGMA8-(VGM A8-VGMA9)x	1369/2114	<b>35<sub>H</sub></b>	VL53	VGMA6-(VGM A6-VGMA7)x	3885/4600
<b>16<sub>H</sub></b>	VL22	VGMA8-(VGM A8-VGMA9)x	1235/2114	<b>36<sub>H</sub></b>	VL54	VGMA6-(VGM A6-VGMA7)x	3706/4600
<b>17<sub>H</sub></b>	VL23	VGMA8-(VGM A8-VGMA9)x	1101/2114	<b>37<sub>H</sub></b>	VL55	VGMA6-(VGM A6-VGMA7)x	3527/4600
<b>18<sub>H</sub></b>	VL24	VGMA8-(VGM A8-VGMA9)x	967/2114	<b>38<sub>H</sub></b>	VL56	VGMA6-(VGM A6-VGMA7)x	3348/4600
<b>19<sub>H</sub></b>	VL25	VGMA8-(VGM A8-VGMA9)x	833/2114	<b>39<sub>H</sub></b>	VL57	VGMA6-(VGM A6-VGMA7)x	3125/4600
<b>1A<sub>H</sub></b>	VL26	VGMA8-(VGM A8-VGMA9)x	714/2114	<b>3A<sub>H</sub></b>	VL58	VGMA6-(VGM A6-VGMA7)x	2887/4600
<b>1B<sub>H</sub></b>	VL27	VGMA8-(VGM A8-VGMA9)x	595/2114	<b>3B<sub>H</sub></b>	VL59	VGMA6-(VGM A6-VGMA7)x	2619/4600
<b>1C<sub>H</sub></b>	VL28	VGMA8-(VGM A8-VGMA9)x	476/2114	<b>3C<sub>H</sub></b>	VL60	VGMA6-(VGM A6-VGMA7)x	2306/4600
<b>1D<sub>H</sub></b>	VL29	VGMA8-(VGM A8-VGMA9)x	357/2114	<b>3D<sub>H</sub></b>	VL61	VGMA6-(VGM A6-VGMA7)x	1845/2600
<b>1E<sub>H</sub></b>	VL30	VGMA8-(VGM A8-VGMA9)x	238/2114	<b>3E<sub>H</sub></b>	VL62	VGMA6-(VGM A6-VGMA7)x	1235/4600
<b>1F<sub>H</sub></b>	VL31	VGMA8-(VGM A8-VGMA9)x	119/2114	<b>3F<sub>H</sub></b>	VL63	VGMA6	



**Table 4. FPD33680F Upper Gamma Voltages**

Data			Output Voltage (gamma F)			Data			Output Voltage (gamma F)		
<b>00<sub>H</sub></b>	VH0	VGMA1		<b>20<sub>H</sub></b>	VH32	VGMA3					
<b>01<sub>H</sub></b>	VH1	VGMA2+(VGM A1-VGMA2)x	5536/6459	<b>21<sub>H</sub></b>	VH33	VGMA4+(VGM A3-VGMA4)x	1710/1829				
<b>02<sub>H</sub></b>	VH2	VGMA2+(VGM A1-VGMA2)x	4762/6459	<b>22<sub>H</sub></b>	VH34	VGMA4+(VGM A3-VGMA4)x	1591/1829				
<b>03<sub>H</sub></b>	VH3	VGMA2+(VGM A1-VGMA2)x	4152/6459	<b>23<sub>H</sub></b>	VH35	VGMA4+(VGM A3-VGMA4)x	1472/1829				
<b>04<sub>H</sub></b>	VH4	VGMA2+(VGM A1-VGMA2)x	3542/6459	<b>24<sub>H</sub></b>	VH36	VGMA4+(VGM A3-VGMA4)x	1353/1829				
<b>05<sub>H</sub></b>	VH5	VGMA2+(VGM A1-VGMA2)x	3081/6459	<b>25<sub>H</sub></b>	VH37	VGMA4+(VGM A3-VGMA4)x	1249/1829				
<b>06<sub>H</sub></b>	VH6	VGMA2+(VGM A1-VGMA2)x	2620/6459	<b>26<sub>H</sub></b>	VH38	VGMA4+(VGM A3-VGMA4)x	1145/1829				
<b>07<sub>H</sub></b>	VH7	VGMA2+(VGM A1-VGMA2)x	2159/6459	<b>27<sub>H</sub></b>	VH39	VGMA4+(VGM A3-VGMA4)x	1041/1829				
<b>08<sub>H</sub></b>	VH8	VGMA2+(VGM A1-VGMA2)x	1846/6459	<b>28<sub>H</sub></b>	VH40	VGMA4+(VGM A3-VGMA4)x	937/1829				
<b>09<sub>H</sub></b>	VH9	VGMA2+(VGM A1-VGMA2)x	1533/6459	<b>29<sub>H</sub></b>	VH41	VGMA4+(VGM A3-VGMA4)x	833/1829				
<b>0A<sub>H</sub></b>	VH10	VGMA2+(VGM A1-VGMA2)x	1265/6459	<b>2A<sub>H</sub></b>	VH42	VGMA4+(VGM A3-VGMA4)x	714/1829				
<b>0B<sub>H</sub></b>	VH11	VGMA2+(VGM A1-VGMA2)x	997/6459	<b>2B<sub>H</sub></b>	VH43	VGMA4+(VGM A3-VGMA4)x	595/1829				
<b>0C<sub>H</sub></b>	VH12	VGMA2+(VGM A1-VGMA2)x	774/6459	<b>2C<sub>H</sub></b>	VH44	VGMA4+(VGM A3-VGMA4)x	476/1829				
<b>0D<sub>H</sub></b>	VH13	VGMA2+(VGM A1-VGMA2)x	551/6459	<b>2D<sub>H</sub></b>	VH45	VGMA4+(VGM A3-VGMA4)x	357/1829				
<b>0E<sub>H</sub></b>	VH14	VGMA2+(VGM A1-VGMA2)x	358/6459	<b>2E<sub>H</sub></b>	VH46	VGMA4+(VGM A3-VGMA4)x	238/1829				
<b>0F<sub>H</sub></b>	VH15	VGMA2+(VGM A1-VGMA2)x	179/6459	<b>2F<sub>H</sub></b>	VH47	VGMA4+(VGM A3-VGMA4)x	119/1829				
<b>10<sub>H</sub></b>	VH16	VGMA2		<b>30<sub>H</sub></b>	VH48	VGMA4					
<b>11<sub>H</sub></b>	VH17	VGMA3+(VGM A2-VGMA3)x	1950/2114	<b>31<sub>H</sub></b>	VH49	VGMA5+(VGM A4-VGMA5)x	4481/4600				
<b>12<sub>H</sub></b>	VH18	VGMA3+(VGM A2-VGMA3)x	1801/2114	<b>32<sub>H</sub></b>	VH50	VGMA5+(VGM A4-VGMA5)x	4347/4600				
<b>13<sub>H</sub></b>	VH19	VGMA3+(VGM A2-VGMA3)x	1652/2114	<b>33<sub>H</sub></b>	VH51	VGMA5+(VGM A4-VGMA5)x	4198/4600				
<b>14<sub>H</sub></b>	VH20	VGMA3+(VGM A2-VGMA3)x	1503/2114	<b>34<sub>H</sub></b>	VH52	VGMA5+(VGM A4-VGMA5)x	4049/4600				
<b>15<sub>H</sub></b>	VH21	VGMA3+(VGM A2-VGMA3)x	1369/2114	<b>35<sub>H</sub></b>	VH53	VGMA5+(VGM A4-VGMA5)x	3885/4600				
<b>16<sub>H</sub></b>	VH22	VGMA3+(VGM A2-VGMA3)x	1235/2114	<b>36<sub>H</sub></b>	VH54	VGMA5+(VGM A4-VGMA5)x	3706/4600				
<b>17<sub>H</sub></b>	VH23	VGMA3+(VGM A2-VGMA3)x	1101/2114	<b>37<sub>H</sub></b>	VH55	VGMA5+(VGM A4-VGMA5)x	3527/4600				
<b>18<sub>H</sub></b>	VH24	VGMA3+(VGM A2-VGMA3)x	967/2114	<b>38<sub>H</sub></b>	VH56	VGMA5+(VGM A4-VGMA5)x	3348/4600				
<b>19<sub>H</sub></b>	VH25	VGMA3+(VGM A2-VGMA3)x	833/2114	<b>39<sub>H</sub></b>	VH57	VGMA5+(VGM A4-VGMA5)x	3125/4600				
<b>1A<sub>H</sub></b>	VH26	VGMA3+(VGM A2-VGMA3)x	714/2114	<b>3A<sub>H</sub></b>	VH58	VGMA5+(VGM A4-VGMA5)x	2887/4600				
<b>1B<sub>H</sub></b>	VH27	VGMA3+(VGM A2-VGMA3)x	595/2114	<b>3B<sub>H</sub></b>	VH59	VGMA5+(VGM A4-VGMA5)x	2619/4600				
<b>1C<sub>H</sub></b>	VH28	VGMA3+(VGM A2-VGMA3)x	476/2114	<b>3C<sub>H</sub></b>	VH60	VGMA5+(VGM A4-VGMA5)x	2306/4600				

**Table 4. FPD33680F Upper Gamma Voltages (continued)**

<b>1D<sub>H</sub></b>	VH29	VGMA3+(VGM A2-VGMA3)x	357/2114	<b>3D<sub>H</sub></b>	VH61	VGMA5+(VGM A4-VGMA5)x	1845/4600
<b>1E<sub>H</sub></b>	VH30	VGMA3+(VGM A2-VGMA3)x	238/2114	<b>3E<sub>H</sub></b>	VH62	VGMA5+(VGM A4-VGMA5)x	1235/4600
<b>1F<sub>H</sub></b>	VH31	VGMA3+(VGM A2-VGMA3)x	119/2114	<b>3F<sub>H</sub></b>	VH63	VGMA5	

**Table 5. FPD33680 R-DAC Resistance Values**

<b>R</b>	<b>F (Ω)</b>	<b>R</b>	<b>F (Ω)</b>
<b>Rx1</b>	923	<b>Rx33</b>	119
<b>Rx2</b>	774	<b>Rx34</b>	119
<b>Rx3</b>	610	<b>Rx35</b>	119
<b>Rx4</b>	610	<b>Rx36</b>	119
<b>Rx5</b>	461	<b>Rx37</b>	104
<b>Rx6</b>	461	<b>Rx38</b>	104
<b>Rx7</b>	461	<b>Rx39</b>	104
<b>Rx8</b>	313	<b>Rx40</b>	104
<b>Rx9</b>	313	<b>Rx41</b>	104
<b>Rx10</b>	268	<b>Rx42</b>	119
<b>Rx11</b>	268	<b>Rx43</b>	119
<b>Rx12</b>	223	<b>Rx44</b>	119
<b>Rx13</b>	223	<b>Rx45</b>	119
<b>Rx14</b>	193	<b>Rx46</b>	119
<b>Rx15</b>	179	<b>Rx47</b>	119
<b>Rx16</b>	179	<b>Rx48</b>	119
<b>Rx17</b>	164	<b>Rx49</b>	119
<b>Rx18</b>	149	<b>Rx50</b>	134
<b>Rx19</b>	149	<b>Rx51</b>	149
<b>Rx20</b>	149	<b>Rx52</b>	149
<b>Rx21</b>	134	<b>Rx53</b>	164
<b>Rx22</b>	134	<b>Rx54</b>	179
<b>Rx23</b>	134	<b>Rx55</b>	179
<b>Rx24</b>	134	<b>Rx56</b>	179
<b>Rx25</b>	134	<b>Rx57</b>	223
<b>Rx26</b>	119	<b>Rx58</b>	238
<b>Rx27</b>	119	<b>Rx59</b>	268
<b>Rx28</b>	119	<b>Rx60</b>	313
<b>Rx29</b>	119	<b>Rx61</b>	461
<b>Rx30</b>	119	<b>Rx62</b>	610
<b>Rx31</b>	119	<b>Rx63</b>	1235
<b>Rx32</b>	119	<b>R<sup>total</sup></b>	15000


**Table 6. FPD33680 I/O Configuration<sup>(1)</sup>**

	INPUTS				OUTPUTS	
--	--------	--	--	--	---------	--

(1) **Note:** This figure represents a FPD33680 die oriented pad side up.

**Table 6. FPD33680 I/O Configuration<sup>(1)</sup> (continued)**

optional	RPI2	Y480
optional	RPIO2	Y479
	VDD2	Y478
	VSS2	
	DIO2	
	RSDS0P	
	RSDS0N	.
	RSDS1P	.
	RSDS1N	.
	RSDS2P	.
	RSDS2N	.
	RSDS3P	.
	RSDS3N	.
	RSDS4P	.
	RSDS4N	.
	RSDS5P	.
	RSDS5N	.
	CLKP	.
	CLKN	.
	RSDS6P	.
	RSDS6N	.
	RSDS7P	.
	RSDS7N	.
	RSDS8P	.
	RSDS8N	.
	RSDS9P	.
	RSDS9N	FPD33680
	RSDS10P	.
	RSDS10N	.
	RSDS11P	.
	RSDS11N	.
	GMA10	.
optional	GMA9	.
optional	GMA8	.
optional	GMA7	.
	GMA6	.
	GMA5	.
optional	GMA4	.
optional	GMA3	.
optional	GMA2	.
	GMA1	.
	VSS1	.
	VDD1	
	CLK1	
	POL	
optional	RSDS_SW	
optional	SHL	
optional	DATPOL	

		<i>OBSOLETE</i>			
 <b>TEXAS INSTRUMENTS</b>				<b>FPD33680</b>	
<a href="http://www.ti.com">www.ti.com</a>				SNOSA70 – MAY 2004	
<b>Table 6. FPD33680 I/O Configuration<sup>(1)</sup> (continued)</b>					
		DIO1			
		VDD2			
		VSS2			.
	optional	RPO1			Y3
	optional	RPI1			Y2
					Y1

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