FAIRCHILD SEMICONDUCTOR®

July 2008

FDZ1905PZ

Common Drain P-Channel 1.5V PowerTrench® WL-CSP MOSFET
–20V, –3A, 123mΩ

Features

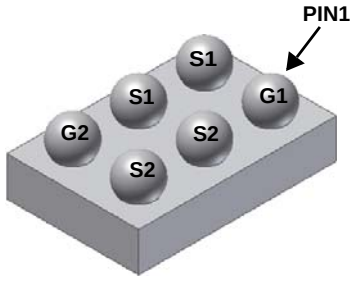
- Max $r_{S1S2(on)}$ = 126mΩ at V_{GS} = –4.5V, I_{S1S2} = –1A
- Max $r_{S1S2(on)}$ = 141mΩ at V_{GS} = –2.5V, I_{S1S2} = –1A
- Max $r_{S1S2(on)}$ = 198mΩ at V_{GS} = –1.8V, I_{S1S2} = –1A
- Max $r_{S1S2(on)}$ = 303mΩ at V_{GS} = –1.5V, I_{S1S2} = –1A
- Occupies only 1.5 mm^2 of PCB area, less than 50% of the area of 2 x 2 BGA
- Ultra-thin package: less than 0.65 mm height when mounted to PCB
- High power and current handling capability
- HBM ESD protection level > 4kV (Note 3)
- RoHS Compliant

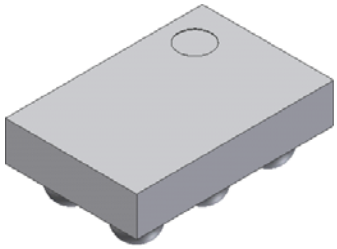
General Description

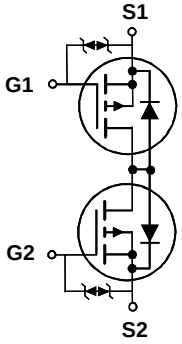
This device is designed specifically as a single package solution for the battery charge switch in cellular handset and other ultra-portable applications. It features two common drain P-channel MOSFETs, which enables bidirectional current flow, on Fairchild's advanced 1.5V PowerTrench® process with state of the art "low pitch" WL-CSP packaging process, the FDZ1905PZ minimizes both PCB space and $r_{S1S2(on)}$. This advanced WL-CSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra-low profile packaging, low gate charge, and low $r_{S1S2(on)}$.

Applications

- Battery management
- Load switch
- Battery protection







MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{S1S2}	Source1 to Source2 Voltage			–20	V
V_{GS}	Gate to Source Voltage			±8	V
I_{S1S2}	Source1 to Source2 Current -Continuous	T_A = 25°C	(Note 1a)	–3	A
	-Pulsed			–15	
P_D	Power Dissipation (Steady State)	T_A = 25°C	(Note 1a)	1.5	W
	Power Dissipation	T_A = 25°C	(Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	83	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	140	

Package Marking and Ordering Information

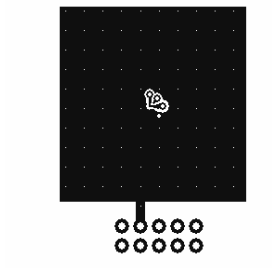
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
5	FDZ1905PZ	WL-CSP 1.0X1.5	7"	8mm	5000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

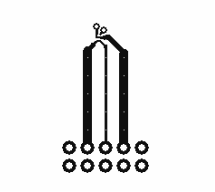
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
I_{S1S2}	Zero Gate Voltage Source1 to Source2 Current	V_{S1S2} = –16V, V_{GS} = 0V			–1	μA
I_{GSS}	Gate Body Leakage Current	V_{GS} = ±8V, V_{S1S2} = 0V			±10	uA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{S1S2}, I_{S1S2} = -250μA	–0.4	–0.7	–1.0	V
$r_{S1S2(on)}$	Static Source1 to Source2 On Resistance	V_{GS} = –4.5V, I_{S1S2} = –1A		99	126	mΩ
		V_{GS} = –2.5V, I_{S1S2} = –1A		112	141	
		V_{GS} = –1.8V, I_{S1S2} = –1A		132	198	
		V_{GS} = –1.5V, I_{S1S2} = –1A		164	303	
		V_{GS} = –4.5V, I_{S1S2} = –1A, T_J = 125°C		135	195	
g_{FS}	Forward Transconductance	V_{S1S2} = –5V, I_{S1S2} = –1A		8		S
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	V_{S1S2} = –10V, I_{S1S2} = –1A, V_{GS} = –4.5V, R_{GEN} = 6Ω		12	22	ns
t_r	Rise Time			36	58	ns
$t_{d(off)}$	Turn-Off Delay Time			143	229	ns
t_f	Fall Time			182	291	ns

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 83°C/W when mounted on a 1 in^2 pad of 2 oz copper



b.140°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300ms, Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics T_J = 25°C unless otherwise noted

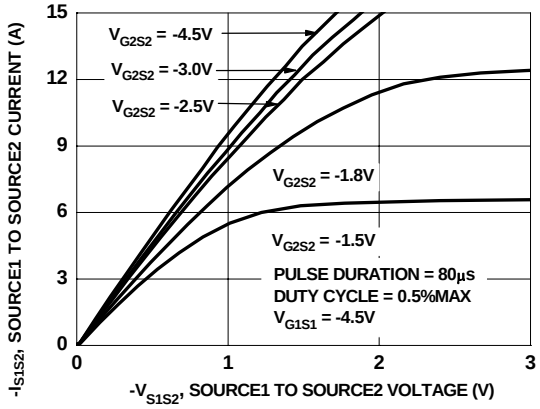


Figure 1. On Region Characteristics

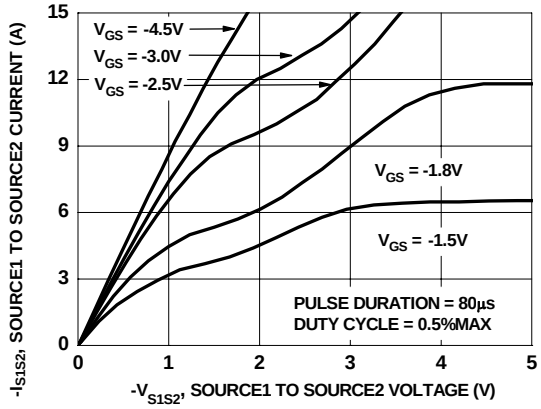


Figure 2. On Region Characteristics

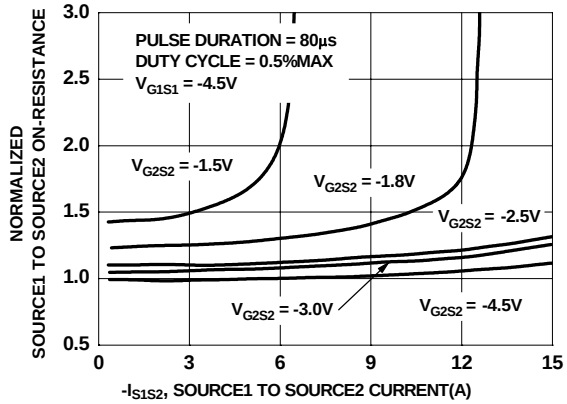


Figure 3. Normalized On-Resistance vs Drain Current and Gate Voltage

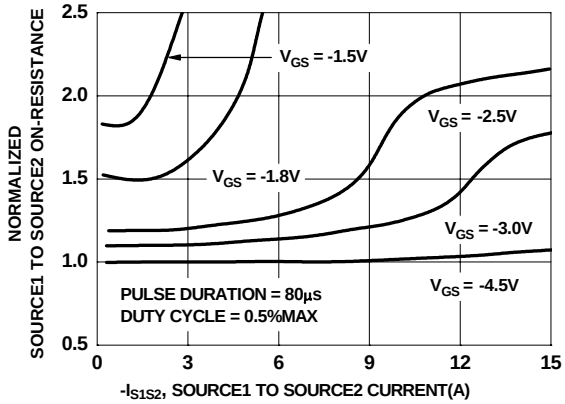


Figure 4. Normalized On-Resistance vs Drain Current and Gate Voltage

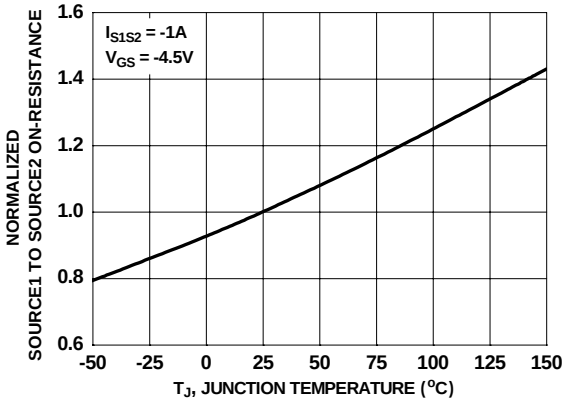


Figure 5. Normalized On Resistance vs Junction Temperature

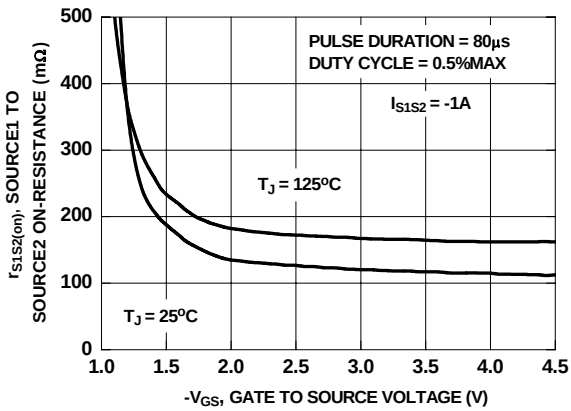


Figure 6. On-Resistance vs Gate to Source Voltage

Typical Characteristics T_J = 25°C unless otherwise noted

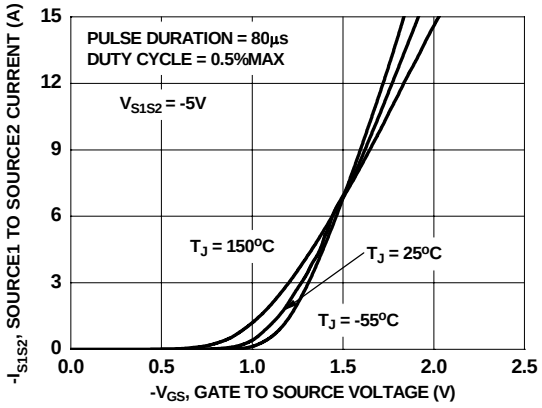


Figure 7. Transfer Characteristics

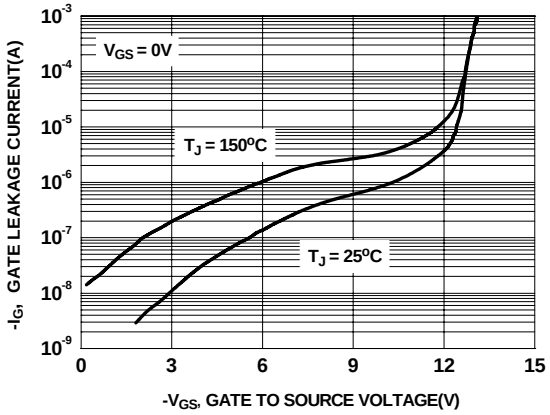


Figure 8. Gate Leakage vs Gate to Source Voltage

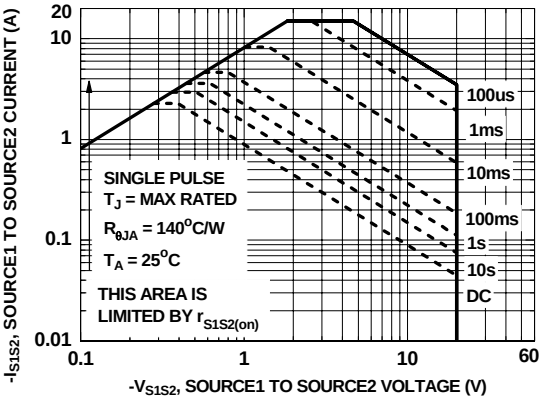


Figure 9. Forward Bias Safe Operating Area

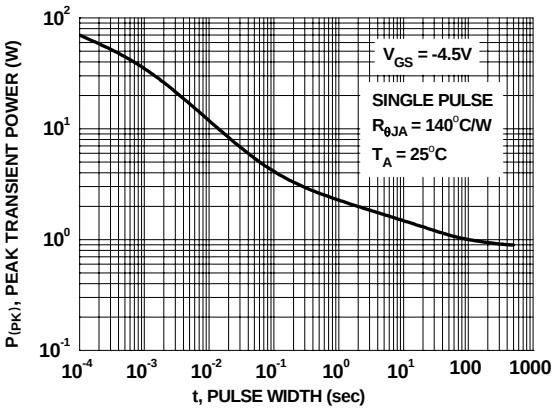


Figure 10. Single Pulse Maximum Power Dissipation

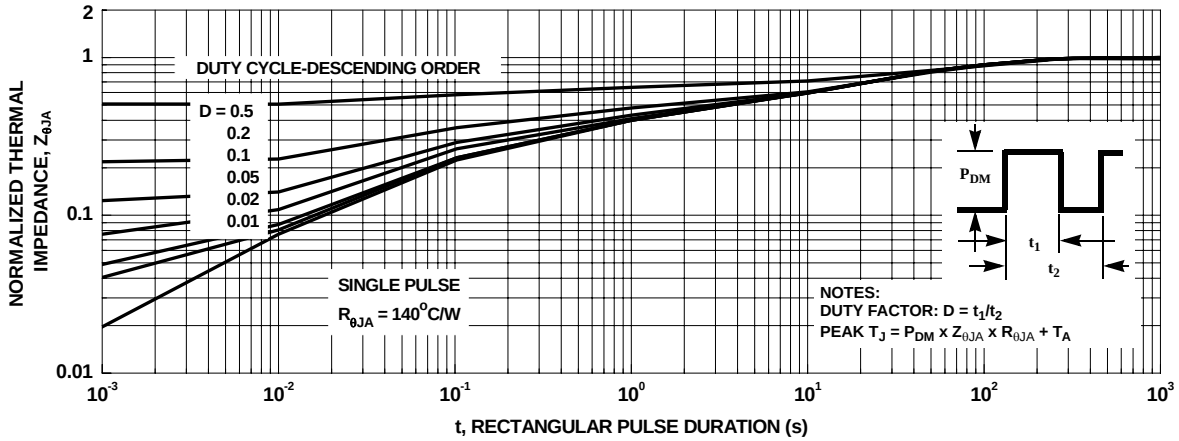
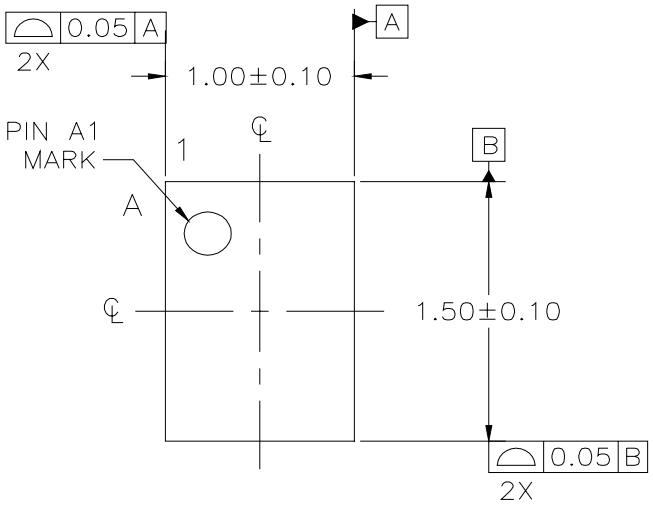
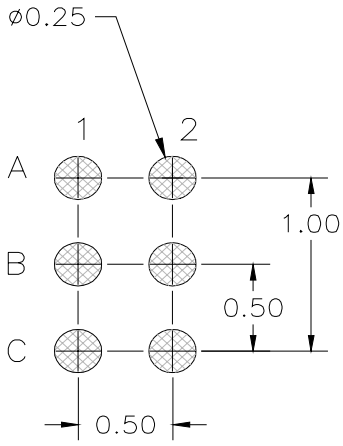
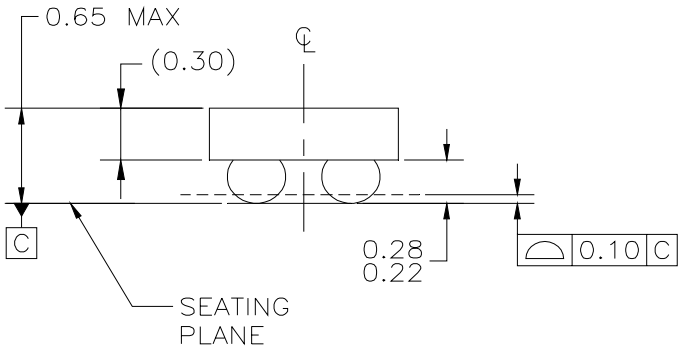


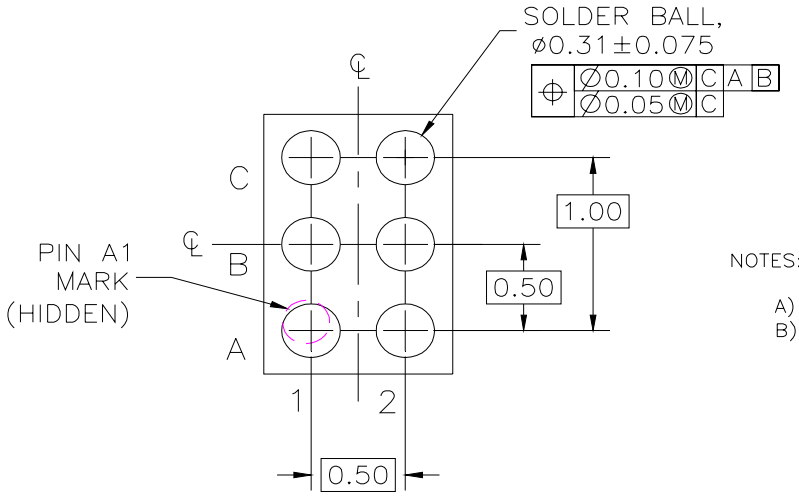
Figure 11. Transient Thermal Response Curve





LAND PATTERN
RECOMMENDATION





NOTES: UNLESS OTHERWISE SPECIFIED

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B) NO JEDEC REGISTRATION REFERENCE AS OF OCTOBER 2005.

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