January 2006

FDY301NZ

Single N-Channel 2.5V Specified PowerTrench® MOSFET

General Description

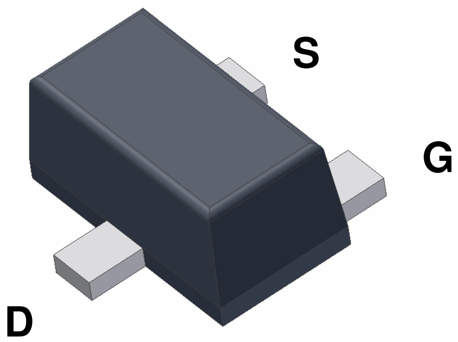
This Single N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced Power Trench process to optimize the $R_{DS(ON)}$ @ V_{GS} = 2.5v.

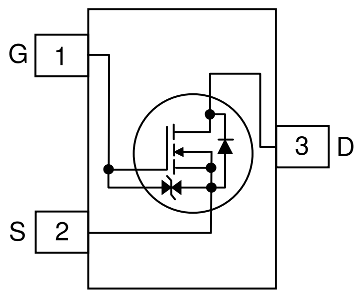
Applications

- Li-Ion Battery Pack

Features

- 200 mA, 20 V $R_{DS(ON)}$ = 5 Ω @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 7 Ω @ V_{GS} = 2.5 V
- ESD protection diode (note 3)
- RoHS Compliant





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		± 12	V
I_D	Drain Current – Continuous	(Note 1a)	200	mA
	– Pulsed		1000	
P_D	Power Dissipation (Steady State)	(Note 1a)	625	mW
		(Note 1b)	446	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	200	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	280	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
D	FDY301NZ	7''	8 mm	3000units

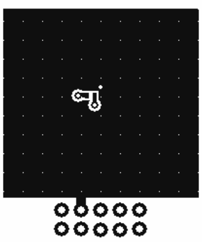
Electrical Characteristics

$T_A = 25°C$ unless otherwise noted

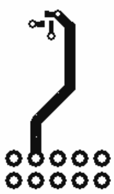
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ µA	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250$ µA, Referenced to 25°C		14		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16$ V, $V_{GS} = 0$ V			1	µA
I_{GSS}	Gate–Body Leakage,	$V_{GS} = \pm 12$ V, $V_{DS} = 0$ V			± 10	µA
		$V_{GS} = \pm 4.5$ V, $V_{DS} = 0$ V			± 1	µA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ µA	0.6	-	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250$ µA, Referenced to 25 C		2.8		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5$ V, $I_D = 200$ mA $V_{GS} = 2.5$ V, $I_D = 175$ mA $V_{GS} = 1.8$ V, $I_D = 150$ mA $V_{GS} = 1.5$ V, $I_D = 20$ mA $V_{GS} = 4.5$ V, I_D=200mA, $T_J = 125°C$			5 7 9 10 7	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 5$ V, $I_D = 200$ mA		1.1		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 10$ V, $V_{GS} = 0$ V, f = 1.0 MHz		60		pF
C_{oss}	Output Capacitance			20		pF
C_{rss}	Reverse Transfer Capacitance			10		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 10$ V, $I_D = 1$ A, $V_{GS} = 4.5$ V, $R_{GEN} = 6$ Ω		6	12	ns
t_r	Turn–On Rise Time			8	16	ns
$t_{d(off)}$	Turn–Off Delay Time			8	16	ns
t_f	Turn–Off Fall Time			2.4	4.8	ns
Q_g	Total Gate Charge	$V_{DS} = 10$ V, $I_D = 200$ mA, $V_{GS} = 4.5$ V		0.8	1.1	nC
Q_{gs}	Gate–Source Charge			0.16		nC
Q_{gd}	Gate–Drain Charge			0.26		nC
Drain–Source Diode Characteristics and Maximum Ratings						
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 150$ mA (Note 2)		0.7	1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = 200$ mA, $dI_F/dt = 100$ A/µs		12		nS
Q_{rr}	Diode Reverse Recovery Charge			3		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 200°C/W when mounted on a 1in^2 pad of 2 oz copper



b) 280°C/W when mounted on a minimum pad of 2 oz copper
Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection againts ESD. No gate overvoltage rating is implied.

Typical Characteristics

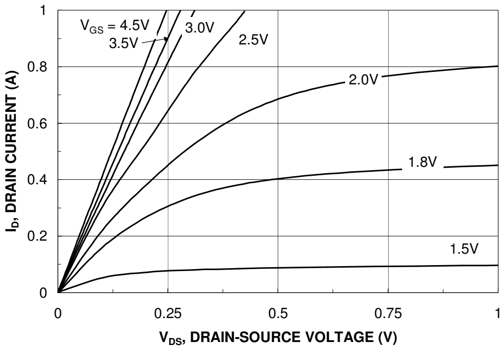


Figure 1. On-Region Characteristics.

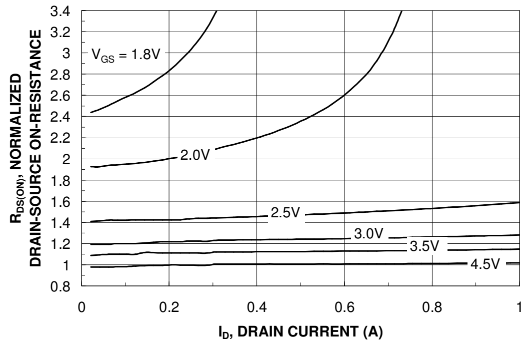


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

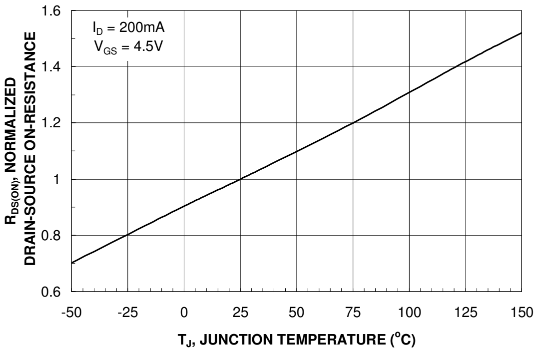


Figure 3. On-Resistance Variation with Temperature.

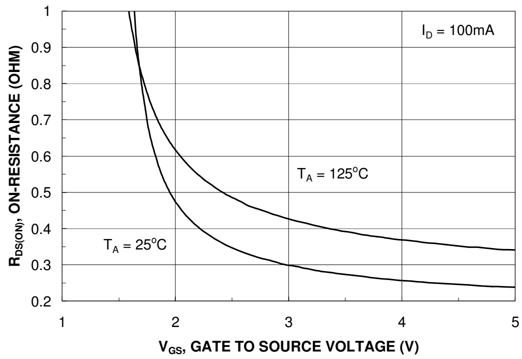


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

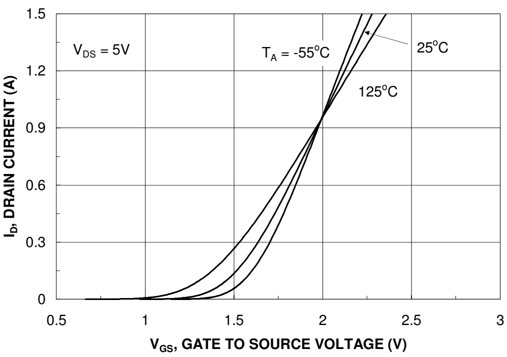


Figure 5. Transfer Characteristics.

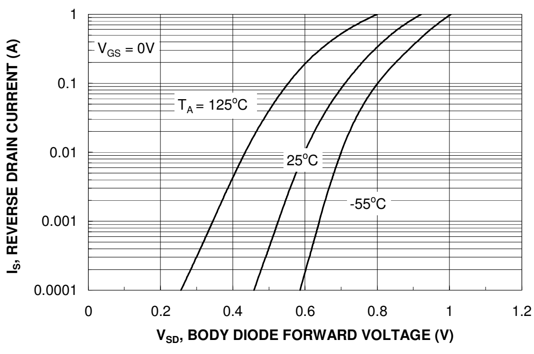


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

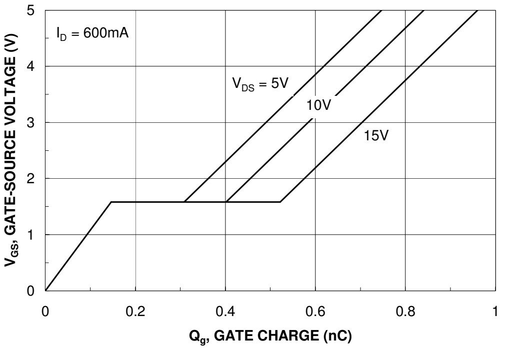


Figure 7. Gate Charge Characteristics.

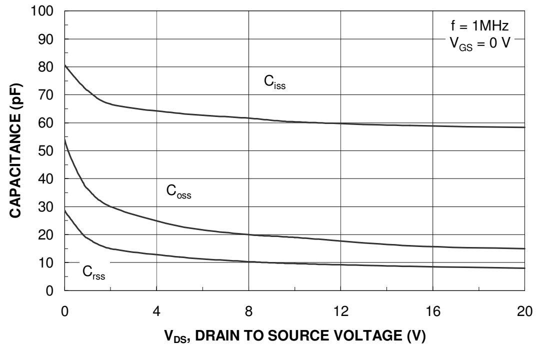


Figure 8. Capacitance Characteristics.

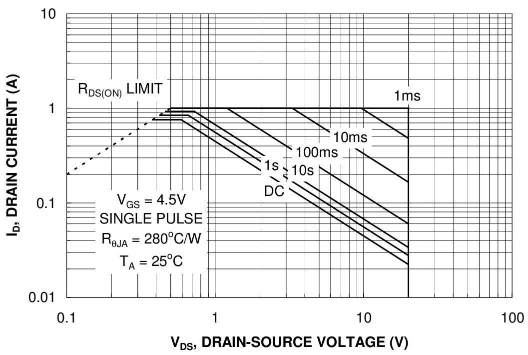


Figure 9. Maximum Safe Operating Area.

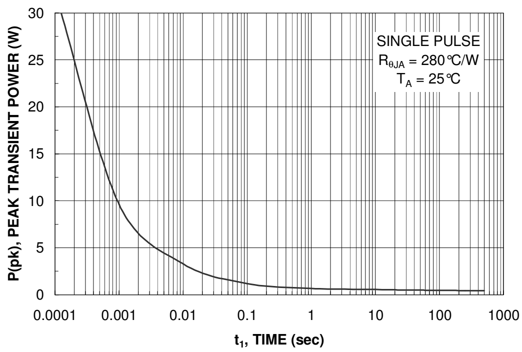


Figure 10. Single Pulse Maximum Power Dissipation.

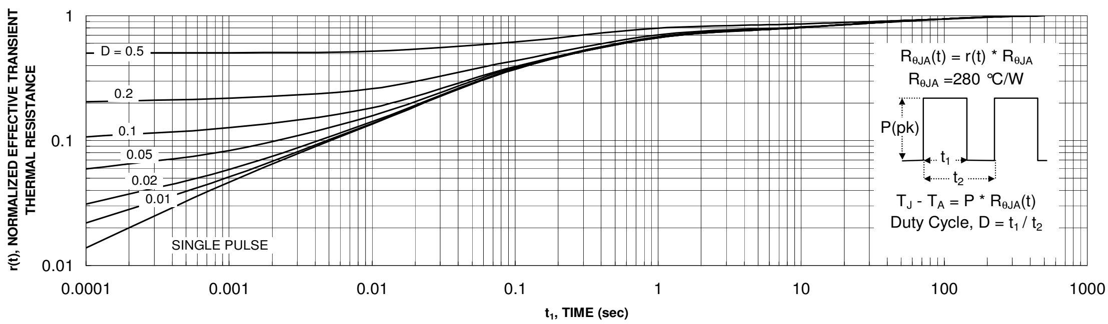
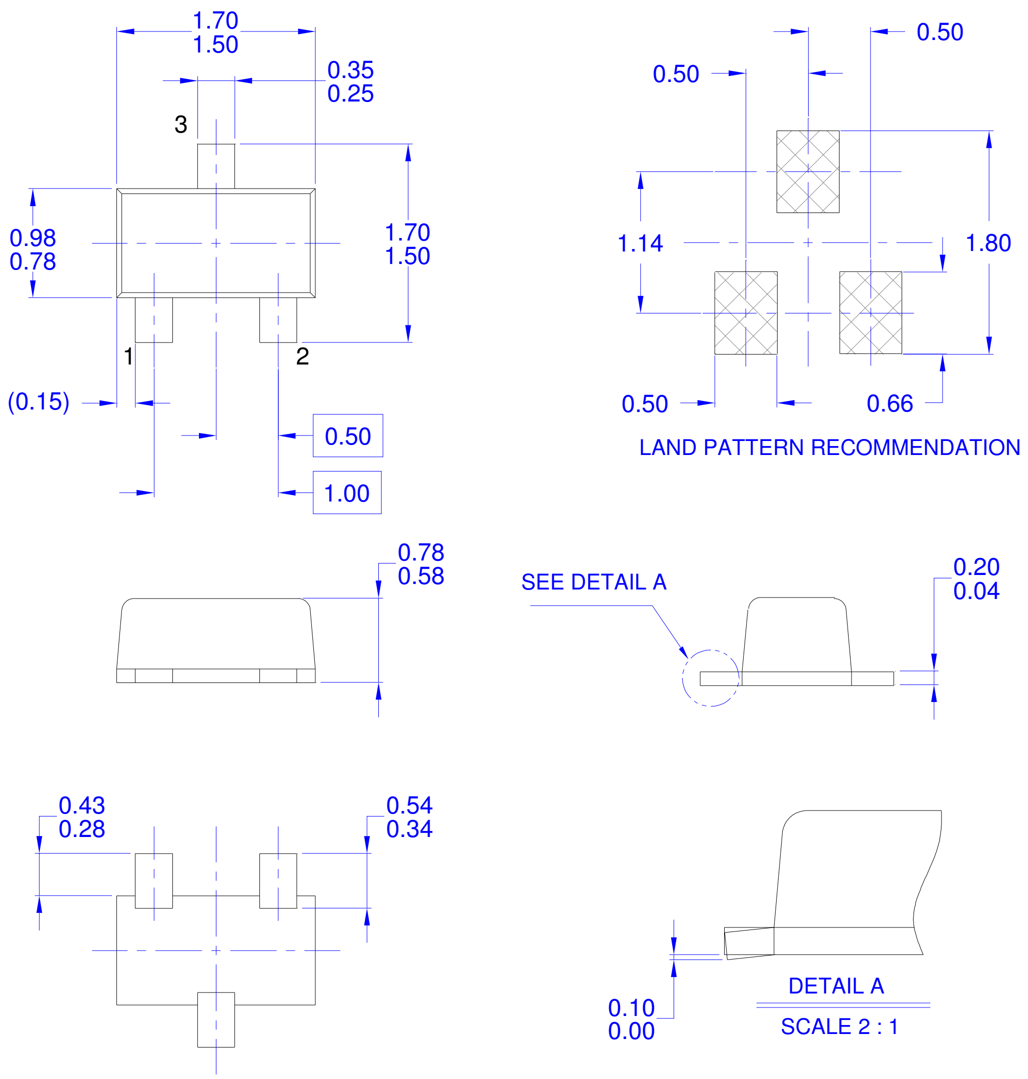


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO EIAJ SC89 PACKAGING STANDARD.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™
ActiveArray™
Bottomless™
Build it Now™
CoolFET™
CROSSVOLT™
DOME™
EcoSPARK™
E^2CMOS™
EnSigna™
FACT™
FACT Quiet Series™
FAST®
FASTr™
FPS™
FRFET™
GlobalOptoisolator™
GTO™
HiSeC™
I^2C™
i-Lo™
ImpliedDisconnect™
IntelliMAX™

Across the board. Around the world.™
The Power Franchise®
Programmable Active Droop™

ISOPLANAR™
LittleFET™
MICROCOUPLER™
MicroFET™
MicroPak™
MICROWIRE™
MSX™
MSXPro™
OCX™
OCXPro™
OPTOLOGIC®
OPTOPLANAR™
PACMAN™
POP™
Power247™
PowerEdge™
PowerSaver™
PowerTrench®
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
RapidConnect™
μSerDes™
ScalarPump™
SILENT SWITCHER®
SMART START™
SPM™
Stealth™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
TCM™
TinyLogic®
TINYOPTO™
TruTranslation™
UHC™
UltraFET®
UniFET™
VCX™
Wire™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.