FAIRCHILD SEMICONDUCTOR®

August 2009

FAN2560
350mA Low-V_{IN} LDO with Fast Transient Response

Features

- 55µA Typical Quiescent Current
- Up to 350mA Output Current
- 2.9V to 5.5V Bias Supply Voltage
- V_{OUT}+0.1V to 5.5V Power Input Supply Voltage
- Fixed Voltage Options: 1.3V and 1.5V
- Thermal Shutdown Protection (TSD)
- Input Under-Voltage Lockout (UVLO)
- Short-Circuit Current Protection (SCP)
- 5-bump 0.96 x 1.33mm WLCSP

Applications

- Moderate Current Digital Loads
- DVB-H, DMB Processors
- Handsets, Smart Phones
- WLAN DC-DC Converter Modules
- PDA, DSC, PMP, and MP3 Players
- Portable Hard Disk Drives

Description

The FAN2560 is a linear low-dropout (LDO) regulator with a split-supply architecture. Separate bias and supply inputs allow bias to be taken directly from the battery, while the input is taken from a lower pre-regulated source. This allows a smaller differential voltage between input and output, which provides greater efficiency over a wider V_{BAT} range.

The FAN2560 is available in a fixed-voltage output, 5-bump, WLCSP package.

Typical Applications

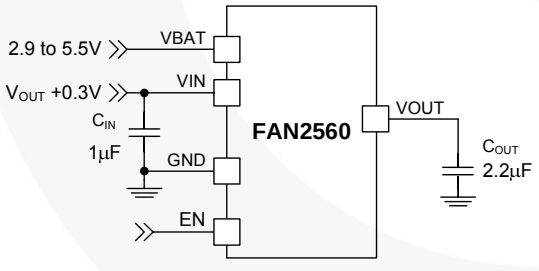


Figure 1. Separate Supply and Bias Line

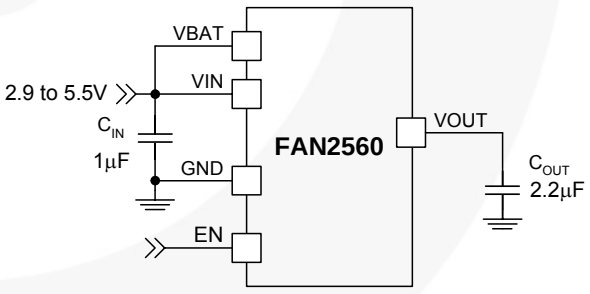


Figure 2. Connected Supply and Bias Line

Ordering Information

Part Number	Operating Temperature Range	Package	Eco Status	Packing Method
FAN2560UC13X	-40°C to 85°C	WLCSP-5 0.96 x 1.33mm	Green	Tape and Reel
FAN2560UC15X	-40°C to 85°C	WLCSP-5 0.96 x 1.33mm	Green	Tape and Reel

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Block Diagram

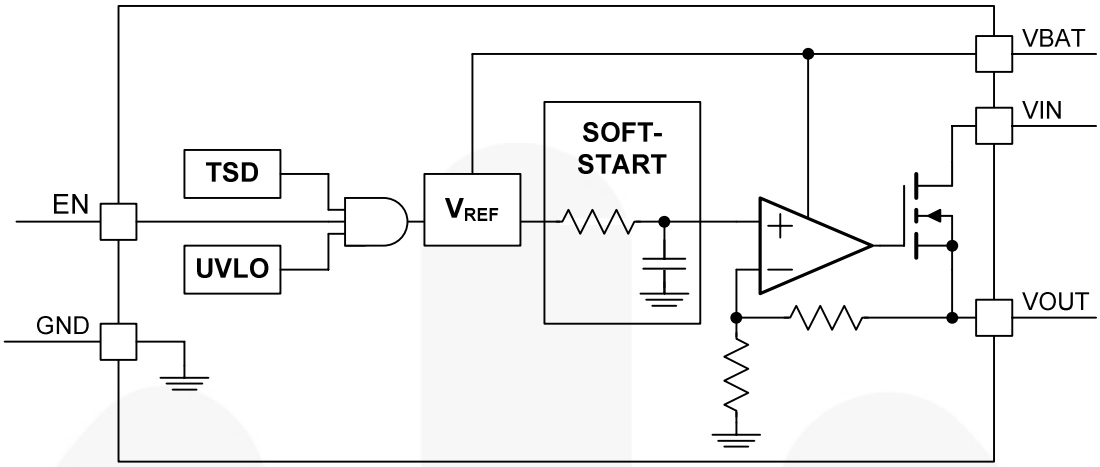


Figure 3. IC Block Diagram

Pin Configuration

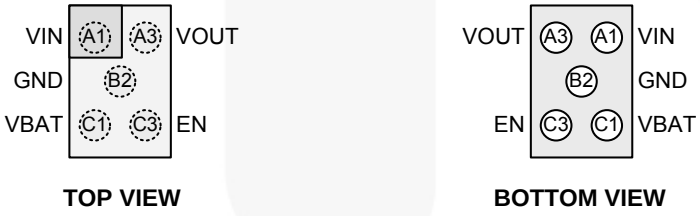


Figure 4. 0.96 x 1.33mm WLCSP package

Pin Definitions

Pin #	Name	Description
A1	VIN	Power supply input. A minimum 1μF MLCC is required to GND.
A3	VOUT	Output Voltage. A typical C_{OUT}=1μF to 2.2μF MLCC is required to GND, placed close to the V_{OUT} terminal.
C1	VBAT	Battery bias supply input. No capacitor is required unless another bulk capacitor is more than few inches away.
C3	EN	Enable input. The device is in shutdown mode when the voltage at this pin is <0.4V and enabled when >1.1V. The EN latches the LOW logic state once externally forced. Do not leave this pin floating when the device is turned ON.
B2	GND	Ground pin. Connect to a PCB GND plane.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Units
	V_{BAT}, V_{IN}, EN		-0.3	6.0	V
V_{OUT}	Output Voltage		-0.3	V_{IN} + 0.3V	V
T_J	Junction Temperature		-40	+150	°C
T_{STG}	Storage Temperature		-65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	3.5		kV
		Charged Device Model per JESD22-C101	1.5		

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{BAT}	Bias Supply Range, (V_{OUT} + 1.4V) < V_{BAT}	2.9		5.5	V
V_{IN}	Power Supply Range, (V_{IN} < V_{BAT})	V_{OUT} + V_{DO}		V_{BAT}	V
I_{OUT}	Output Current	0		350	mA
C_{IN}	Input Capacitor (Effective Capacitance)	0.7	1.0		μF
	Equivalent Series Resistance (ESR)	0		300	mΩ
C_{OUT}	Output Capacitor (Effective Capacitance)	0.7	2.2	12.0	μF
	Equivalent Series Resistance (ESR)	3		300	mΩ
T_A	Operating Ambient Temperature Range	-40		+85	°C
T_J	Operating Junction Temperature Range	-40		+125	°C

Thermal Properties

Symbol	Parameter	Min.	Typ.	Max.	Units
Θ_{JA}	Junction-to-Ambient Thermal Resistance		180(1)		°C/W

Note:

1 Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer boards in accordance to JESD51- JEDEC standard. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature T_A.

Electrical Characteristics

V_{BAT}=2.9V to 5.5V, V_{IN}=V_{OUT} + 0.3V, T_A=-40°C to +85°C, Test Circuit Figure 1, unless otherwise noted. Typical values are at T_A=25°C, V_{BAT}=3.6V, I_{LOAD}=1mA, V_{EN}=1.8V.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supplies						
V_{BAT}	Battery Input Supply	(V_{OUT} + 1.4V) < V_{BAT}	2.9		5.5	V
V_{IN}	Input Voltage Range	V_{IN} < V_{BAT}	V_{OUT} + V_{DO}		V_{BAT}	V
I_{BAT}	V_{BAT} Supply Current	I_{LOAD}=0µA		55	70	µA
I_{IN}	V_{IN} Supply Current	I_{LOAD}=0µA		4	11	µA
I_{VBATSD}	V_{BAT} Shutdown Supply Current	V_{BAT}=3.6V, EN=GND		0.01	1.00	µA
I_{VINSD}	V_{IN} shutdown Supply Current	V_{BAT}=3.6V, EN=GND		0.01	1.00	µA
V_{UVLO}	Under-voltage Lockout Threshold	V_{BAT} Falling Edge		2.0	2.4	V
		Hysteresis		0.05		V
$V_{(EN)}$	Enable High-level Input Voltage		1.1			V
	Enable Low-level Input Voltage				0.4	
$I_{(EN)}$	Enable Input Leakage Current	EN=V_{IN} or GND		0	0.5	µA
Regulation						
I_{OUT}	Maximum Output Current		350			mA
V_{DO}	Dropout Voltage with Respect to V_{IN}[2]	I_{LOAD}=350mA		70	200	mV
ΔV_{OUT}	Output Voltage Accuracy	Over Full V_{IN}, I_{OUT}, and Temperature Range	-2		2	%
$\Delta V_{OUTline}$	Line Regulation	Over Full V_{IN}, V_{BAT}, I_{OUT} Range		< 6		mV
$\Delta V_{OUTload}$	Load Regulation					
I_{SCP}	Short-circuit Current Limit			400		mA
I_{SU}	Start-up Peak Current	V_{BAT} and V_{IN} applied, EN from L to H, no load, T_A= -30C to +85C; 3V<V_{BAT} <4.5V		130	300	mA
		2.9V<V_{BAT} <5.5V			500	
TSD	Thermal Shutdown	Rising Temperature		150		°C
		Hysteresis		10		°C
PSRR	Power Supply Rejection Ratio	V_{IN}, 10Hz to 10kHz		> 60		dB
		V_{BAT}, 10Hz to 10kHz		> 50		
e_n	Output Noise Voltage	10Hz to 100kHz		60		μV_{RMS}
Timing Characteristics						
Peak $\Delta V_{OUTline}$	Line Transient Response	600mV, t_{RISE}=t_{FALL}=10µs		±2		mV
Peak $\Delta V_{OUTload}$	Load Transient Response	0 to 300mA, t_{RISE}=t_{FALL}=1µs		±15		mV
t_{ON}	Turn-on Time			70	200	µs

Note:

2 Dropout voltage is the minimum input to output differential voltage needed to maintain V_{OUT} in regulation, in specified conditions

Typical Characteristics

Unless otherwise specified, C_{IN}=1μF ceramic, C_{OUT}=2.2μF ceramic, V_{IN}=V_{OUTnom} + 0.3V, V_{BAT}=3.6V, T_A=25C, V_{EN}=1.8V.

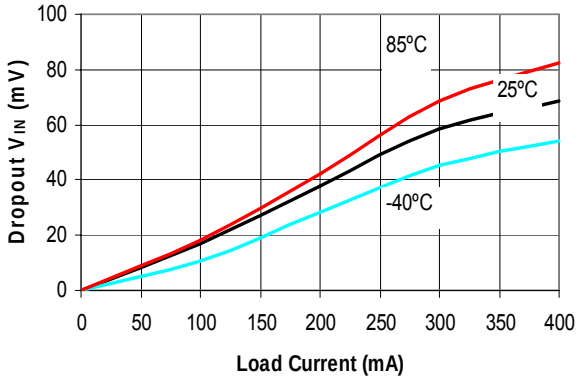


Figure 5. Dropout Voltage vs. Load Current

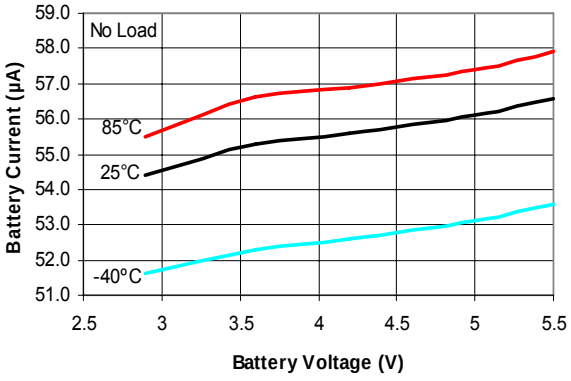


Figure 6. Battery Quiescent Supply Current

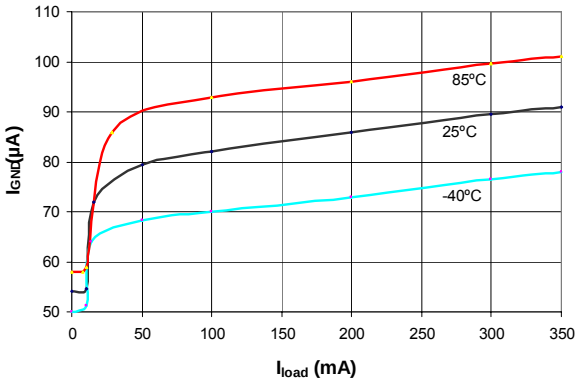


Figure 7. GND Current vs. Load Current

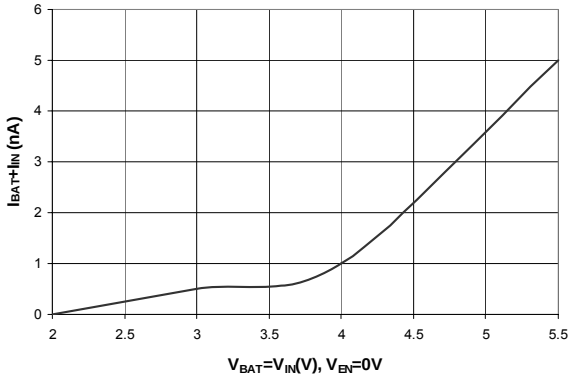


Figure 8. Off Mode Current

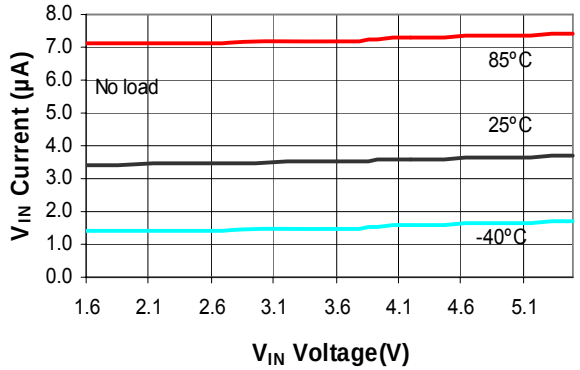


Figure 9. Input V_{IN} Quiescent Current (V_{BAT}=5.5V)

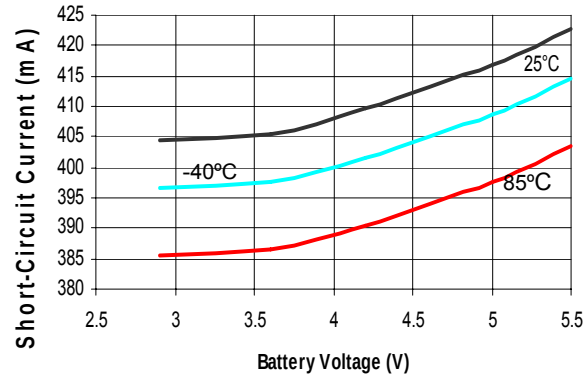


Figure 10. Output Short-Circuit Current

Typical Characteristics (Continued)

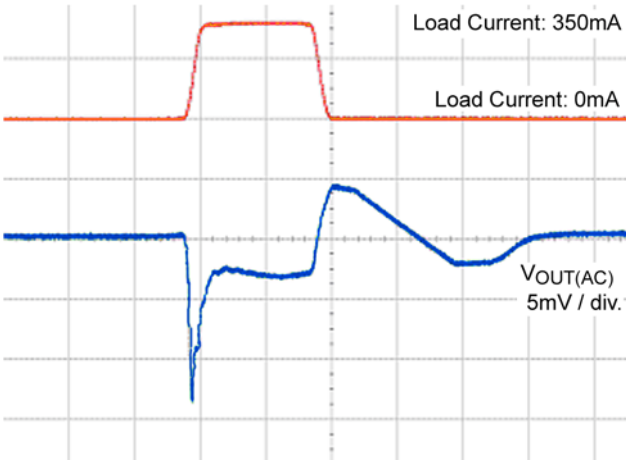


Figure 11. Load Transient Response (5µs/div.)

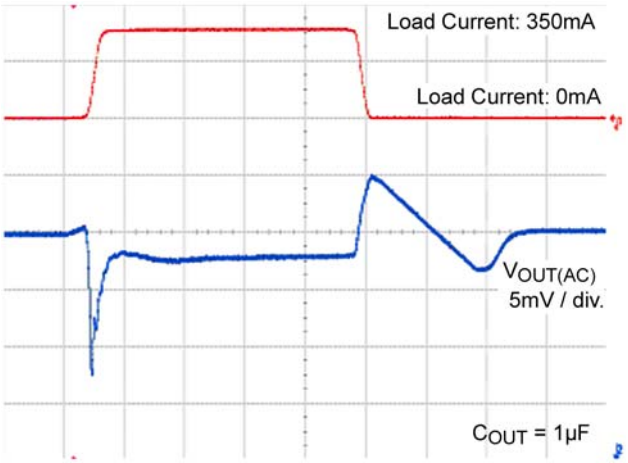


Figure 12. Load Transient Response (5µs/div.)

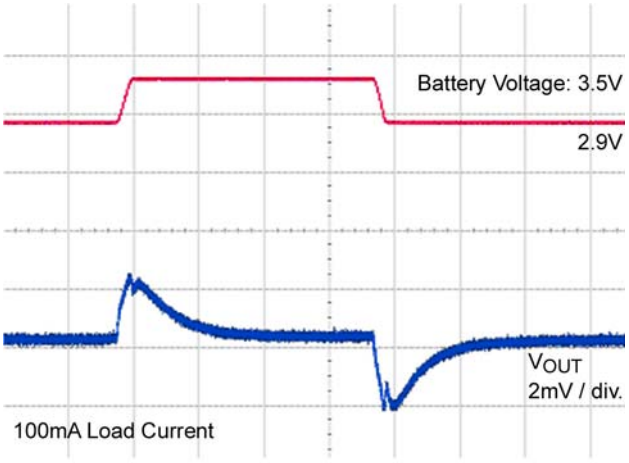


Figure 13. Line Transient Response (50µs/div.)

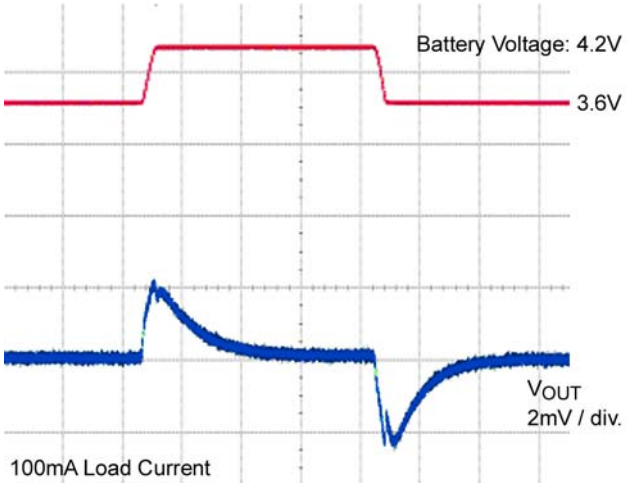


Figure 14. Line Transient Response (50µs/div.)

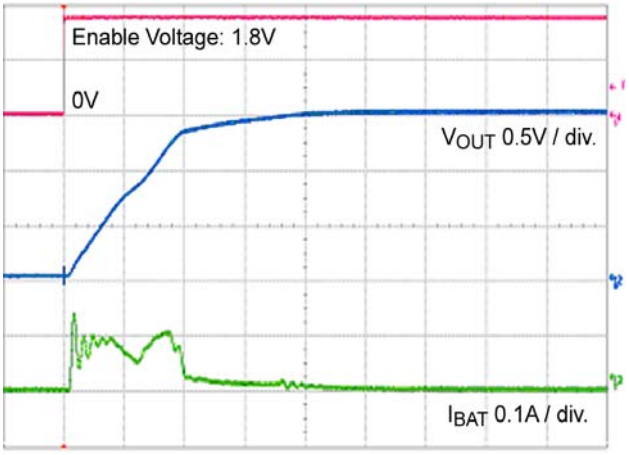


Figure 15. Start-up and Inrush Current (20µs/div.)

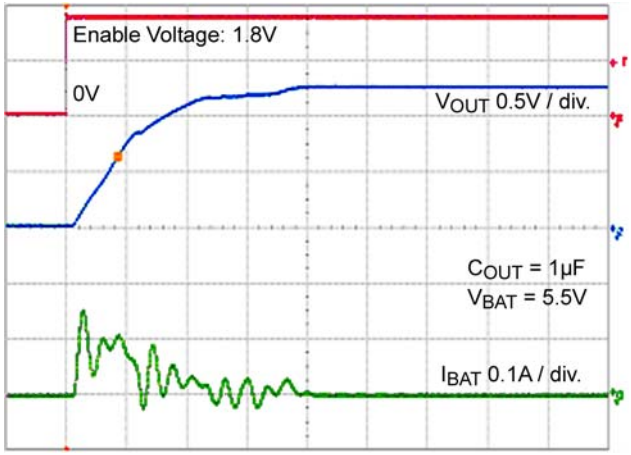


Figure 16. Start-up and Inrush Current (20µs/div.)

Typical Characteristics (Continued)

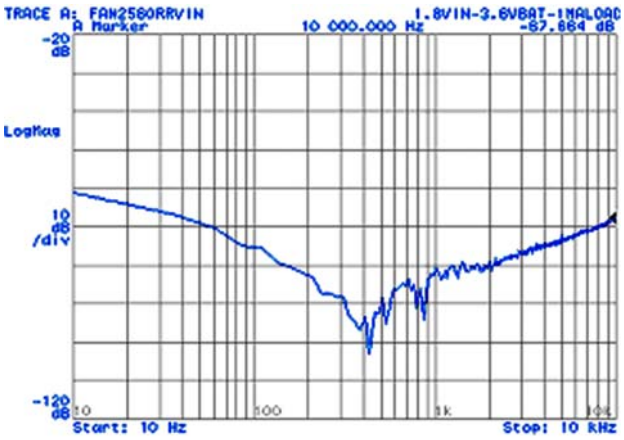


Figure 17. PSRR V_{IN}, 10Hz to 10kHz, 1mA

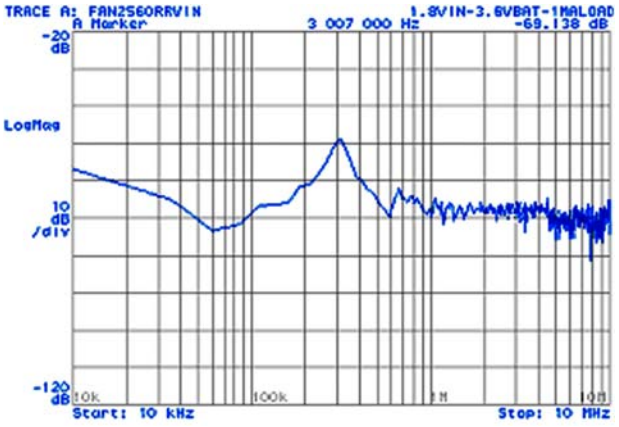


Figure 18. PSRR V_{IN}, 10kHz to 10MHz, 1mA

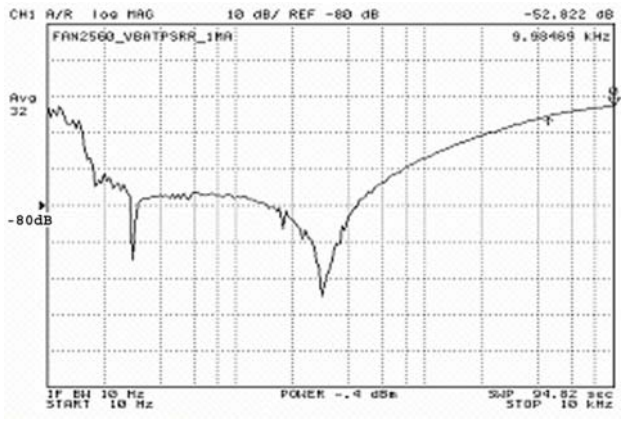


Figure 19. PSRR V_{BAT}, 10Hz to 10kHz, 1mA

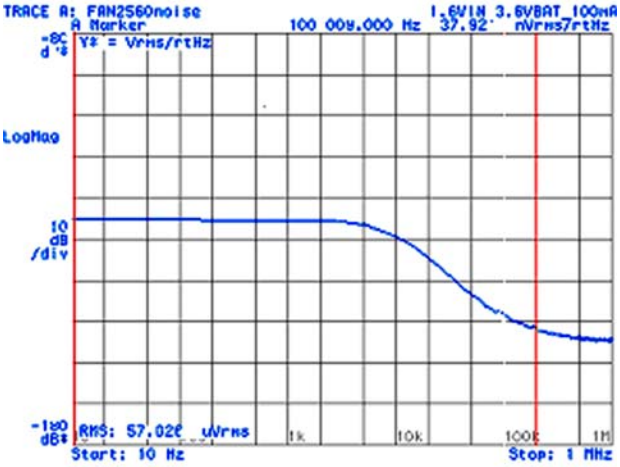


Figure 20. Noise Spectral Power Density, 100mA

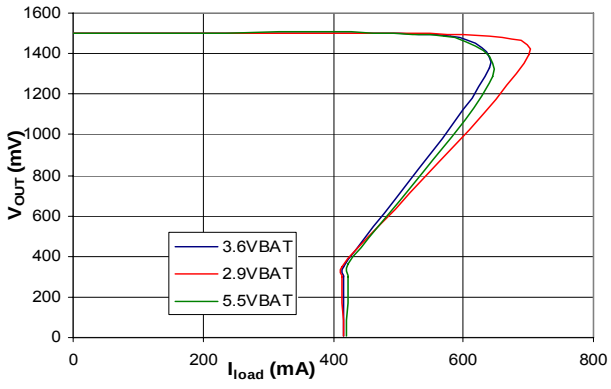


Figure 21. Output Current Voltage Characteristic, 1.5V Option

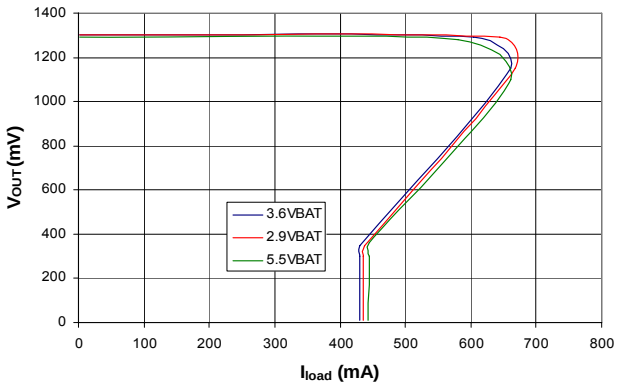


Figure 22. Output Current Voltage Characteristic, 1.3V Option

Application Information

ENABLE Latch

A pull-down resistor latches the LOW state of the EN input after this input is externally forced LOW. A low-side switch turns ON a 370 kΩ pull-down resistance to keep the EN in LOW state, even if the EN input is subsequently left floating.

Soft-Start

A soft-start function prevents an excessive input current flow during start-up. When the LDO is enabled, the soft-start circuit limits the peak inrush current below the specified maximum value, which increases when C_{OUT} increases. To further reduce the peak inrush current, the output capacitance may be lowered to 1µF, taking advantage of FAN2560 stability over a wide range of C_{OUT} capacitance.

Short-Circuit and Thermal Protection

The FAN2560 output current voltage characteristic has a fold-back shape that indicates a short-circuit current limit lower than the maximum load current. Although the short-circuit current is limited to below 500mA, the device can supply high peak output currents of up to 1A for brief periods. However, this output overload may cause the die temperature to increase and exceed maximum ratings due to power dissipation. In such cases, depending upon the ambient temperature, V_{IN}, load current, and the junction-to-air thermal resistance (θ_{JA}) of the die, the device may enter thermal shutdown. During output overload conditions, when the die temperature exceeds the shutdown limit temperature of 150°C, the onboard thermal protection disables the output until the temperature drops below this limit, at which point the output is re-enabled.

Thermal Considerations

For best performance, the die temperature and the power dissipated should be kept at moderate values. The maximum power dissipated can be evaluated based on the following relationship:

$$P_{D(max)} = \left\{ \frac{T_{J(max)} - T_A}{\Theta_{JA}} \right\} \quad (1)$$

where $T_{J(max)}$ is the maximum allowable junction temperature of the die, which is 125°C, and T_A is the ambient operating temperature. θ_{JA} is dependent on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground.

The addition of backside copper with through-holes, stiffeners, and other enhancements can also aid in reducing θ_{JA}. The heat contributed by the dissipation of other devices located nearby must be included in design considerations.

Reverse Current Path

During normal operation, V_{IN} is higher than V_{OUT} and the parasitic diode for the series power FET is reverse biased. If the output voltage is externally forced above the input voltage, the parasitic diode gets forward biased and starts to conduct. In this case, it is necessary to limit the reverse current to maximum 100mA to avoid adversely affecting reliability.

Capacitors Selection

The FAN2560 is stable with a wide range of ceramic output capacitors. An output capacitor of at least 0.7µF effective capacitance and the minimum ESR over the frequency range of 3 to 300mΩ is required to ensure stability over the full range of supply voltages and load currents. High-ESR tantalum or electrolytic capacitors may be used, but a low ESR ceramic capacitor has to be connected in parallel at the output, at a distance no more than 1-inch from the VOUT pin. The MLCC capacitors indicated in Table 1 have been successfully tested with the FAN2560.

Table 1. Recommended Capacitors

Capacitance	Size	Vendor	Part number
1µF	0603	MURATA	GRM188R71C105KA120
2.2µF	0603	MURATA	GRM188R61A225KF340
2.2µF	0402	MURATA	GRM155R60J225ME15

Application Example: Post Regulator for a Switching Converter

The FAN2560 is an ideal choice for battery-powered equipment. The low quiescent bias current can be supplied directly from the battery, while the input voltage can come from a high-efficiency buck regulator, like FAN5350. This combination provides both best efficiency and low noise output. As can be seen in the scope pictures below the schematic, the already-low output voltage ripple, inherent to a switching regulator, is significantly attenuated by the FAN2560 at any frequency within the switching operating range.

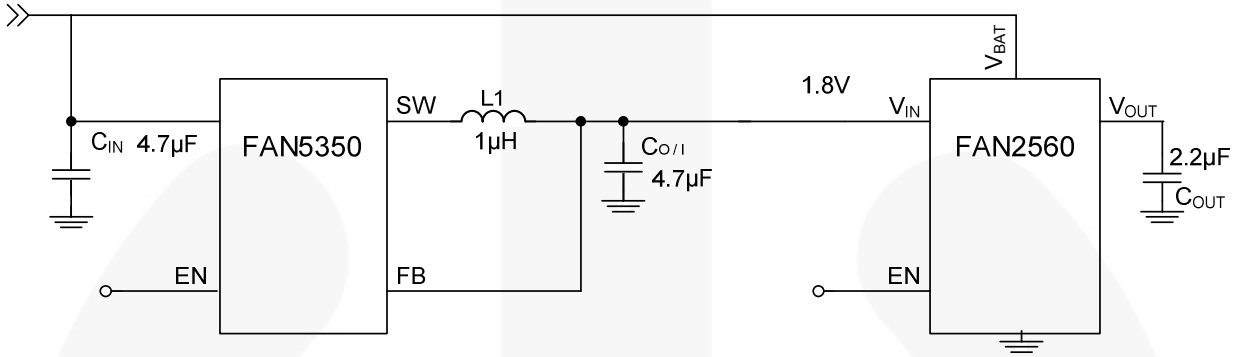


Figure 23. Post Regulator for a Switching Converter

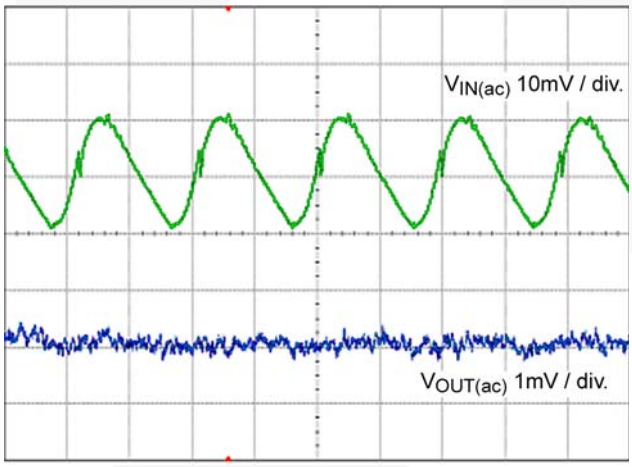


Figure 24. PFM Mode (100mA Load) Buck Ripple Rejection, Horizontal Scale: 500ns/div.

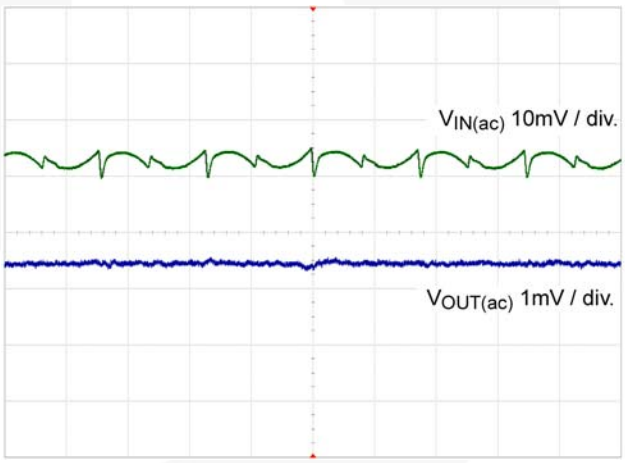
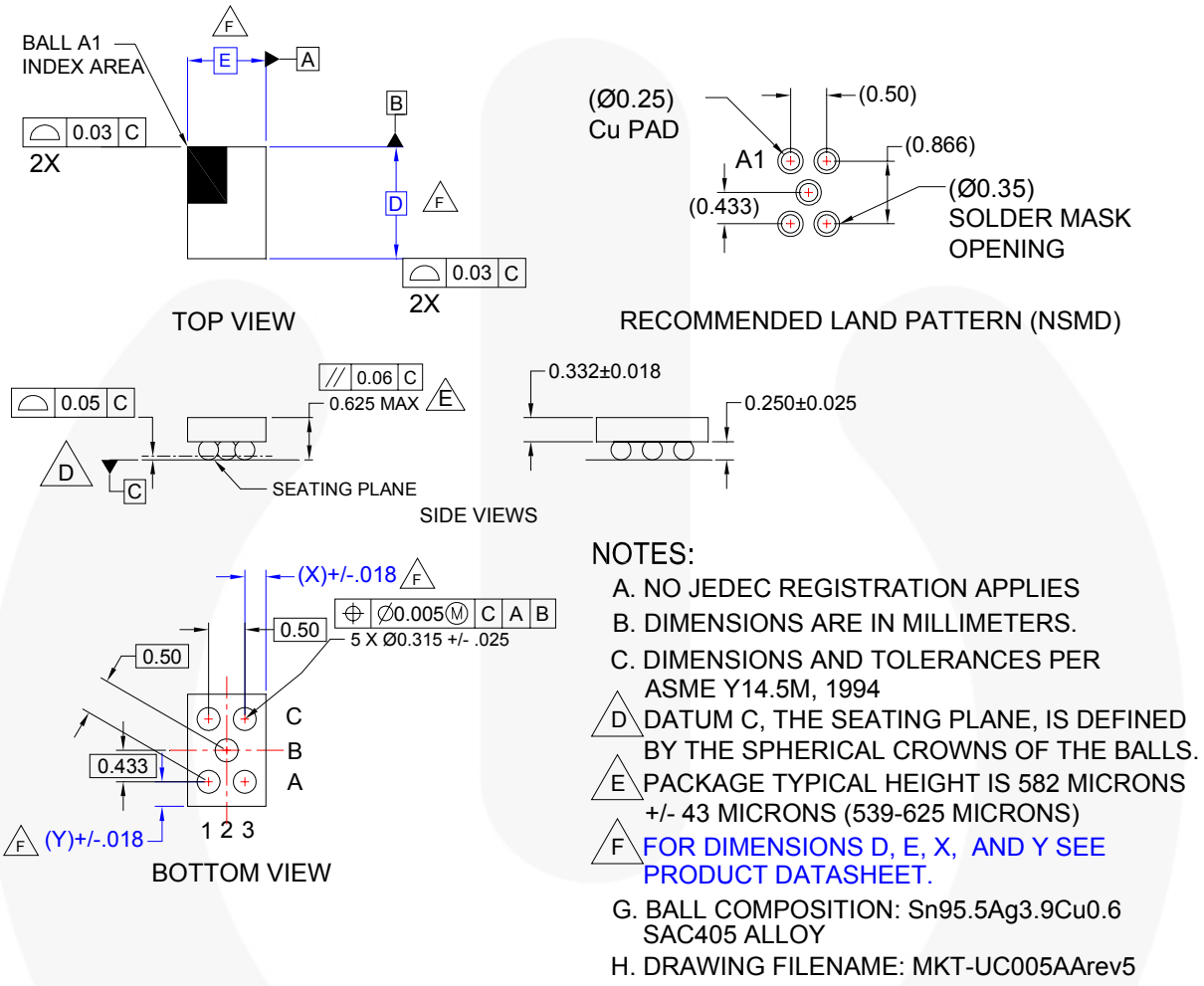


Figure 25. PWM, 3MHz (300mA Load) Buck Ripple Rejection, Horizontal Scale: 200ns/div.

Physical Dimensions



NOTES:

A. NO JEDEC REGISTRATION APPLIES

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

D. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE TYPICAL HEIGHT IS 582 MICRONS +/- 43 MICRONS (539-625 MICRONS)

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. BALL COMPOSITION: Sn95.5Ag3.9Cu0.6 SAC405 ALLOY

H. DRAWING FILENAME: MKT-UC005AArev5

Figure 26. Wafer-Level Chip-Scale Packaging (WLCSP)

Product Specific Dimensions

Product	D	E	X	Y
FAN2560UC13X	1.330 +/- 0.030	0.960 +/- 0.030	0.230	0.232
FAN2560UC15X	1.330 +/- 0.030	0.960 +/- 0.030	0.230	0.232

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FlashWriter®*
FPS™
F-PFS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
G*max*™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
MotionMax™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
PDP SPM™
Power-SPM™
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS™
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TinyBuck™
TinyCalc™
TinyLogic®
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TinyPower™
TinyPWM™
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Definition of Terms

Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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