DSPAUDIOEVM with DSP56720DB, DSP56721DB, DSP56724DB, or DSP56725DB User's Guide

freescale™
semiconductor

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 010 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
    Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
+1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
    @hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Document Number: DSP56720DBUG
Rev. 4, 06/2008

Contents

About This Book

Chapter 1
Overview

Chapter 2
Configuring the DSPAUDIOEVM Motherboard

Chapter 3
Configuring the DSP56720/DSP56724 Daughterboard

Chapter 4
Configuring the DSP56721/DSP56725 Daughterboard

DSPAUDIOEVM with DSP56720DB, DSP56721DB, DSP56724DB, or DSP56725DB, Rev. 4

Chapter 5
Getting Started

Appendix A
Programming the MCUs

About This Book

Use this document to install and configure a DSP56720, DSP56721, DSP56724, or DSP56725 daughterboard onto a DSPAUDIOEVM motherboard. Together, the daughterboard and motherboard comprise a hardware and software development platform for DSP5672x devices.

Audience

This document is intended for engineers and programmers who want to prototype and test systems using DSP5672x devices.

Organization

To install the DSP56720, DSP56721, DSP56724, or DSP56725 daughterboard onto the DSPAUDIOEVM motherboard, follow the procedures in this document.

Chapter 1 *Overview*   Describes the evaluation board set (daughterboard, motherboard), available debuggers, and basic configure/install/power-up plan.

Chapter 2 *Configuring the DSPAUDIOEVM Motherboard*
                    Shows how to configure the DSPAUDIOEVM motherboard.

Chapter 3 *Configuring the DSP56720 or DSP56724 Daughterboard*
                    Shows how to configure the DSP56720 or DSP56724 daughterboard.

Chapter 4 *Configuring the DSP56721 or DSP56725 Daughterboard*
                    Shows how to configure the DSP56721 or DSP56725 daughterboard.

Chapter 5 *Getting Started*
                    Describes how to complete the installation procedure, and pass audio using a passthru code or perform an external memory test.

Appendix A *Programming the MCUs*
                    Shows how to program the microcontrollers (CONFIG, DEBUG) on the motherboard

Revision History

The following table summarizes revisions to this document.

Revision History

Revision	Date	Description
4	June 2008	Updated to include DSP56724 and DSP56725.

Documentation Available

Documentation Available

Order Number	Document	Description
DSP56720FS	Symphony^{TM} Audio DSP56720/DSP56721 Fact Sheet	Provides a brief overview of DAP56720/DSP56721 features and benefits.
DSP56720PB	Symphony DSP56720 Dual-Core Audio Processor Product Brief	Provides a detailed overview of the DSP56720 device.
DSP56721PB	Symphony DSP56721 Dual-Core Audio Processor Product Brief	Provides a detailed overview of the DSP56721 device.
DSP56720RM	Symphony Audio DSP56720/DSP56721 Reference Manual	Provides detailed hardware-oriented information about the DSP56720 and DSP56721 devices.
DSP56724FS	Symphony^{TM} Audio DSP56724/DSP56725 Fact Sheet	Provides a brief overview of DAP56720/DSP56721 features and benefits.
DSP56724PB	Symphony DSP56724 Dual-Core Audio Processor Product Brief	Provides a detailed overview of the DSP56720 device.
DSP56725PB	Symphony DSP56725 Dual-Core Audio Processor Product Brief	Provides a detailed overview of the DSP56721 device.
DSP56724RM	Symphony Audio DSP56724/DSP56725 Reference Manual	Provides detailed hardware-oriented information about the DSP56720 and DSP56721 devices.
DSP56300FM	DSP56300 Family Manual	Provides the instruction set for the DSP563xx and DSP5672x devices.

Conventions

This document uses the following notational conventions:

- `Courier monospaced type` indicate commands, command parameters, code examples, expressions, datatypes, and directives.
- *Italic type* indicates replaceable command parameters.

Definitions, Acronyms, and Abbreviations

The following list defines the acronyms and abbreviations used in this document. As this template develops, this list will be generated from the document. As we develop more group resources, these acronyms will be easily defined from a common acronym dictionary. Please note that while the acronyms are in solid caps, terms in the definition should be initial capped ONLY IF they are trademarked names or proper nouns.

DSP	Digital Signal Processor
EVM or EVB	Evaluation Module or Evaluation Board
JTAG	Joint Test Access Group (a standard test interface)
OnCE™	On-Chip Emulation
PPI	Parallel Port Interface

Chapter 1
Overview

1.1   Introduction

The DSPAUDIOEVM evaluation board (called the motherboard) and the DSP56720DB, DSP56721DB, DSP56724DB, or DSP56725DB board (called the daughterboard) demonstrate the abilities of the DSP5672x family of digital signal processors, and also serve as a hardware platform for the development of applications that use these devices.

Used together, the DSPAUDIOEVM and a DSP5672x daughterboard perform the following functions:

- Allow you to become familiar with the features of the specific DSP architecture.
- Serve as a platform for real-time software development. The tool suite enables you to develop and simulate routines, download the software to on-chip or on-board RAM, and then run and debug the software using a debugger through the OnCE™ port. The breakpoint features of the OnCE port enable you to easily specify break conditions and to execute your developed software at full speed, until the break conditions are satisfied. The ability to examine and modify all user-accessible registers, memory, and peripherals through the OnCE port simplifies development problems.
- Serve as a platform for hardware development. The hardware platform enables you to connect external hardware peripherals. The on-board peripherals can be disabled, providing you with the ability to reassign any and all of the DSP's peripherals. The OnCE port's unobtrusive design means that all of the memory on the board and on the DSP chip is available to you.

1.1.1   Daughterboard

Different daughterboards are available that support the DSP5672x digital signal processor family. Each daughterboard connects to the motherboard using two 96-pin connectors and, depending on the DSP, also contains external SRAM, FLASH or EEPROM. For more information about specific daughterboards, refer to their specific chapter in this document.

1.1.2   Motherboard

The motherboard has a variety of digital and analog audio I/O including:

- Four switchable S/PDIF inputs (two optical and two coaxial)
- Four simultaneous S/PDIF outputs (three coaxial and one coaxial/optical)
- Twelve analog output channels (six stereo RCA-type connectors)
- Two analog microphone inputs
- Two analog inputs (one stereo RCA-type connectors)
- Headphone output (can mix any combination of analog signals using a switch array)

The motherboard uses an included external universal power supply (100–220 VAC, 50–60 Hz). The power supply uses an IEC three-pin power connector for the AC supply. You must supply your own AC cable to connect the included motherboard power supply to the region-specific AC power connection.

There are two HC08 Freescale microcontrollers included on the motherboard. The two microcontrollers each have a dedicated function (either debug or config) and are re-flashable if a field upgrade is required on the EVM. User programming of these two microcontrollers is possible but is not supported by Freescale Semiconductor. Table 1-1 describes the uses of the on-board microcontrollers.

Table 1-1. On-Board Microcontrollers

Microcontroller	Description
Config MPU	An HC908GP32 microcontroller pre-programmed with software to enable all of the on-board AKM components and clocking mode changes. This "config" microcontroller also controls the mute functionality of the final audio outputs and the switching of the inputs sourced to the DSP daughterboard.
Debug MPU	An HC908JB16 microcontroller which is pre-programmed with software to allow communication (from a host PC to the DSP) via the serial RS232 and USB ports in conjunction with the supplied SDI debugger software.

1.2 Debugger Interfaces

1.2.1 OnCE^{TM} Debugger

The motherboard supports multiple debugger interfaces. The Freescale high-speed parallel port OnCE command converter tool is embedded in the DSPAUDIOEVM (no special cables are required). An IEEE Std 1284™ parallel port cable is included in the EVM kit for convenience. Also included is a OnCE header, for use with external command converters.

The OnCE interface can be used with the Freescale Symphony Studio tool set. To get the latest software and documentation, go to http://www.freescale.com/symphonystudio.

1.2.2 Symphony Debugger Interface

In addition to OnCE debugging, the motherboard includes a real-time Symphony Debugger Interface (SDI). This debugger uses either an RS-232 or USB interface and allows SPI or I^{2}C communication to the DSP from a PC, for real-time debugging and configuration of the DSP. SDI software and documentation are available on Freescale's website (go to http://www.freescale.com/symphony and click on the Software Tools link.)

SDI version 2.5 or higher is required for use with a DSP56720 or DSP56721 daughterboard and may require an update to the motherboard firmware for proper operation. Only revision D motherboards are shipped from the factory with the SDI 2.5-compatible firmware. The firmware update is included in the online SDI download. Use the procedures in Section Appendix A, "Programming the MCUs," to update the motherboard firmware.

NOTE

The SDI debugger software is designed for use with the Software Architecture contained within the ROM of the DSP. The SDI debugger is not designed for use as a stand-alone, general purpose debugger.

1.3 Configuration, Installation, and Power-Up Procedures

To configure the motherboard and daughterboard evaluation system to run using the included sample code, follow the steps shown in Table 1-2.

Table 1-2. Configuration, Installation, and Power-Up Procedures

Step	Description	See this section...
1	Configure the motherboard.	Chapter 2, "Configuring the DSPAUDIOEVM Motherboard"
2	Configure the daughterboard.	Chapter 3, "Configuring the DSP56720/DSP56724 Daughterboard"
3	Install the daughterboard onto the motherboard.	Chapter 5, "Getting Started"
4	Connect the power supply to the motherboard and power up.	
5	Install/connect all peripherals, cables, and equipment.	
6	Run the passthru code.	
7	Observe LEDs.	
8	Power down.	

Chapter 2
Configuring the DSPAUDIOEVM Motherboard

2.1   DSPAUDIOEVM Motherboard Overview

There are eleven jumper blocks on the motherboard that allow you to select various board configurations.
Table 2-1 describes how to use this chapter's sections to configure your DSPAUDIOEVM motherboard.

Table 2-1. Configuring the DSPAUDIOEVM Motherboard

For Information About	Go to...	
Meet the DSPAUDIOEVM motherboard	Section 2.1, "DSPAUDIOEVM Motherboard Overview"	on page 2-1
Configure jumpers	Section 2.2, "Configuration Jumpers"	on page 2-1
Configure other controls and switches	Section 2.3, "Controls and Switches" Section 2.4, "Signal Headers and Connectors"	on page 2-6 on page 2-7

2.2   Configuration Jumpers

Set or verify the settings for jumpers JP1–JP11 on the motherboard using the tables and figures in this
section.

Table 2-2 lists the jumpers on the DSPAUDIOEVM motherboard; to locate the jumpers, see Figure 2-1.
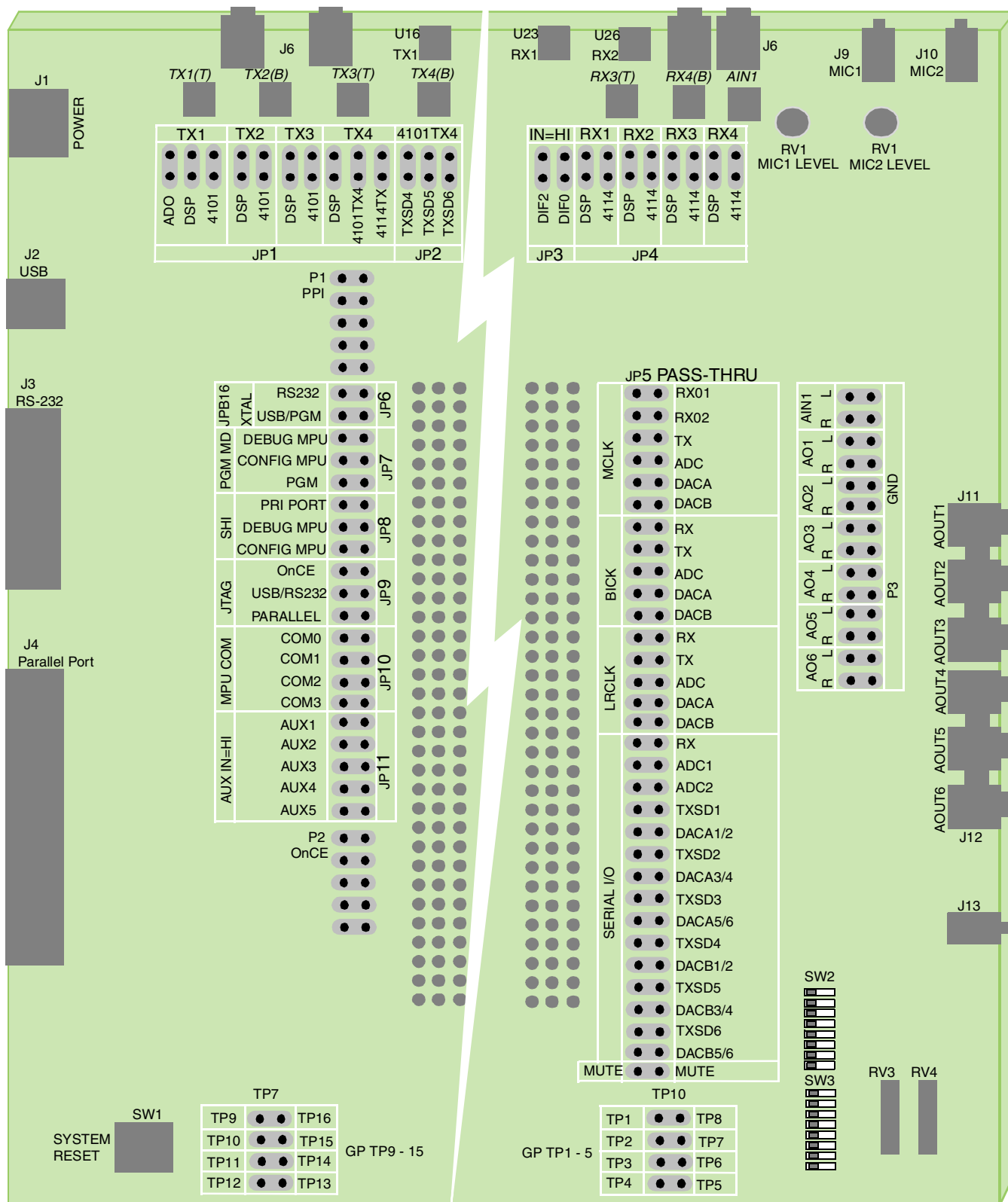
Figure 2-1. Locate Jumpers/Switches on DSPAUDIOEVM

Table 2-2. Jumper Options

Function	Jumper	Position	Description
JP1 — TX1 (ADO, DSP, 4101), TX2 (DSP, 4101), TX3 (DSP, 4101), TX4 (DSP, 4101TX4, 4114TX)	JP1		Use JP1 to select the S/PDIF output source. The output may be the daughterboard (DSP), AKM 4101 S/PDIF transmitter, or AKM 4114 S/PDIF receiver.
		ADO	This jumper is not supported by the DSP56720 or the DSP56721 daughterboard.
		DSP	The DSP option for each TX set allows for direct connection to the internal S/PDIF transmitter of the DSP. See the board-specific schematic to determine which DSP signal is connected in this position.
		4101	The 4101 option for each TX set allows for connection of the I2S outputs from the DSP to the AKM 4101 S/PDIF transmitter. See the board-specific schematic to determine which DSP signal is connected in this position.
		4101TX4	To send one of the S/PDIF signals (TXSD4, TXSD5, or TXSD6) to the TX4 output, select the S/PDIF signal (using a jumper in JP2) and select TX4 (using the 4101TX4 jumper in the TX4 section of JP1).
		4114TX4	The 4114TX jumper option on TX4 allows direct connection of the S/PDIF receiver to S/PDIF out.
JP2 — 4104TX4 (TXSD4, TXSD5, TXSD6)	JP2	TXSD4 TXSD5 TXSD6	See the board-specific schematic to determine which DSP signals are available for each jumper option.
JP3 — IN=HI (DIF2, DIF0)	JP3	DIF2 DIF0	The JP3 jumper allows for hardware configuration of the AKM 4114 S/PDIF receiver. The default setting is for software control mode, where the AKM 4114 is configured by the Freescale HC908GP32 configuration microcontroller on the motherboard. See the AKM 4114 manual for details on using this jumper to configure the S/PDIF receiver.
JP4 — RX1 (DSP, 4114), RX2 (DSP, 4114), RX3 (DSP, 4114), RX4 (DSP, 4114)	JP4		The JP4 jumper controls the S/PDIF receiver input source to allow direct routing to the daughterboard (using the DSP jumper setting) or to select connection to the AKM 4114.
		DSP	The DSP option connects the S/PDIF signal directly to the internal S/PDIF receiver of the DSP.
		4114	The 4114 option routes the incoming S/PDIF signal through the AKM 4114 S/PDIF receiver and to the I2S signals of the DSP.

See the board-specific schematics to determine which DSP signals are available for each jumper option. |

Table 2-2. Jumper Options (continued)

Function	Jumper	Position	Description
JP5 (MCLK, BICK, LRCLK, SERIAL I/O, MUTE jumper block as illustrated)	**JP5**	—	The JP5 jumper block provides convenient access to critical audio clocks and data lines. The JP5 jumpers can be removed to allow rerouting of the audio signals within the board and also to allow for expansion to external boards. For example, the JP5 header could be used to connect to an external audio codec board for evaluation of a DSP with a specific audio codec.
JP6 — JB16 EXTAL (RS232, USB/PGM)	**JP6**		Use the JP6 jumper to select the appropriate JB16 clock source. **CAUTION** Only one JP6 jumper should be connected at any one time. Using the wrong jumper setting can cause SDI communications to fail or cause a reduction in the data transfer rate.
		RS232	To use an RS-232 interface with the SDI debugger, install a jumper at the RS232 position.
		USB/PGM	Use this jumper if you are using the USB interface with the SDI debugger or to reprogram the debug and configuration microcontrollers.
JP7 — PGM MD (DEBUG MPU, CONFIG MPU, PGM)	**JP7**	**DEBUG MPU CONFIG MPU PGM**	Use the JP7 jumpers to re-program the on-board microcontrollers (Debug MPU, Config MPU). See Appendix A, "Programming the MCUs" for more details regarding re-programming the on-board mircocontrollers.

JP5 jumper labels (MCLK): RX01, RX02, TX, ADC, DACA, DACB
(BICK): RX, TX, ADC, DACA, DACB
(LRCLK): RX, TX, ADC, DACA, DACB
(SERIAL I/O): RX, ADC1, ADC2, TXSD1, DACA1/2, TXSD2, DACA3/4, TXSD3, DACA5/6, TXSD4, DACB1/2, TXSD5, DACB3/4, TXSD6, DACB5/6
(MUTE): MUTE

DSPAUDIOEVM with DSP56720DB, DSP56721DB, DSP56724DB, or DSP56725DB User's Guide, Rev. 4

Table 2-2. Jumper Options (continued)

Function	Jumper	Position	Description
JP8 SHI — PPI PORT / DEBUG MPU / CONFIG MPU	JP8		Use the JP8 jumpers to select SDI debugger modes. **CAUTION** Only one jumper should be installed at a time in any of the three JP8 jumper positions (DEBUG MPU, PPI PORT, CONFIG MPU).
		PPI PORT	Placing a jumper in the PPI PORT position allows for control via P1, the PPI header. This header can be used with legacy development tools or can be connected to an external microcontroler.
		DEBUG MPU	The default selection is to use the SDI debugger (jumper in DEBUG MPU position).
		CONFIG MPU	Not currently supported
JP9 JTAG — OnCE / USB/RS32 / PARALLEL	JP9		Use the JP9 jumpers to select the OnCE debugger interface. **CAUTION** Only one jumper should be installed at a time in any of the allowed JP9 jumper positions.
		OnCE	To connect an *external* OnCE/JTAG debugger interface to the board via the P2, the OnCE header, install a jumper in the OnCE jumper position.
		PARALLEL	Install a jumper in the PARALLEL position of the JP9 jumper and connect the EVM to a host PC with a parallel cable to use the on-board parallel OnCE interface.
		USB/232	Not currently supported.

DSPAUDIOEVM with DSP56720DB, DSP56721DB, DSP56724DB, or DSP56725DB User's Guide, Rev. 4

Table 2-2. Jumper Options (continued)

Function	Jumper	Position	Description
MPU COM — JP10 (COM0, COM1, COM2, COM3)	**JP10**	—	The JP10 jumpers provide a communication port between the debug microcontroller and the configuration microcontroller. If using the SDI debugger interface, install all JP10 jumpers (positions COM0 - COM3).
AUX IN=HI — JP11 (AUX1, AUX2, AUX3, AUX4, AUX5)	**JP11**	—	The JP11 jumper allows for manual control of the AKM 4114 input signal when not using the Symphony Debugger Interface (SDI) debugger. Inputs are selected as shown below. **Note:** When the Aux5 jumper is installed, the Aux4 jumper controls the mute functionality of the EVM motherboard. Installing a jumper in Aux4 mutes the DACs on the EVM. (see table below)

Input Selected	JP11				
	Aux5	**Aux4**	**Aux3**	**Aux2**	**Aux1**
RX1	1	0	0	0	0
RX2		0	0	0	1
RX3		0	0	1	0
RX4		0	0	1	1
AIN1 48 KHz		0	1	0	0
AIN1 96 KHz		0	1	0	1
SDI debugger selects input	0	X	X	X	X

1 = jumper is installed, 0 = jumper is not installed.

2.3 Controls and Switches

Other devices allow you additional control of the microphone and headphone functions. See Figure 2-1 for control and switch locations.

Table 2-3. Controls and Switches

Function	Control or Switch	Description
Microphone Gain Control	**RV1, RV2**	The RV1 and RV2 potentiometers control the input levels for MIC1 and MIC2 respectively. To prevent damage, always start with these controls in a low setting, turned all the way counter-clockwise. These inputs can be monitored directly by using the on-board headphone amplifier.

Table 2-3. Controls and Switches (continued)

Function	Control or Switch	Description
Headphone Volume Select	**RV3, RV4**	The RV3 and RV4 sliders control volume and balance adjustment for the headphone amplifier. To prevent damage to the headphones or your hearing, always start with the sliders in a low-volume position.
Headphone Channel Select	**SW2, SW3**	The SW2 and SW3 switches control which analog output is routed to the on-board headphone amplifier. Moving the switch to the right (the ON position) enables the corresponding channel. Multiple switches/channels can be enabled at one time, and the signals are summed into the corresponding headphone channel.

2.4   Signal Headers and Connectors

Signal headers and connectors allow external debugger connections, analog output signal measurement, and GPIO access. Headers and connectors are listed in Table 2-4.

Table 2-4. Signal Headers and Connectors

Function	Connector or Header	Description		
PPI	**P1**	The PPI header connections allow for backwards compatibility with legacy software tool sets, and also allow easy access to the SHI port signals from the DSP. To use the PPI header, JP8 must have a jumper installed in the PPI PORT location.	**P1 – PPI**	
			NC (Pin 1) * * SS/HA2	
			GND * * SCK/SCL	
			GND * * SS_1/HA2_1	
			MISO/SDA * * MOSI/HA0	
			3.3V * * MISO/SDA	
OnCE	**P2**	Use the P2 OnCE header to connect an external OnCE/JTAG debugger tool to the OnCE/JTAG port of the DSP on the daughterboard. When using an external OnCE/JTAG debugger tool, a jumper must be installed in the OnCE position of the JP9 JTAG jumper.	**P2 – OnCE**	
			TDI (Pin 1) * * GND	
			TDO * * GND	
			TCK * * GND	
			N/C * KEY	
			RESET * * TMS	
			3.3 V * * N/C	
			N/C * * N/C	

Table 2-4. Signal Headers and Connectors (continued)

Function	Connector or Header	Description
Analog I/O	**P3**	Use the Analog I/O header for analog access to input signals before the A/D (AIN1) op-amp stage and to the output signals after the D/A (AO1-6) op-amp stage. This header is provided for easy analog measurements and to support analog I/O connector relocation. *(see table below)*

AO6		**AO5**		**AO4**		**AO3**		**AO2**		**AO1**		**AIN1**	
R	L	R	L	R	L	R	L	R	L	R	L	R	L
*	*	*	*	*	*	*	*	*	*	*	*	*	*
*	*	*	*	*	*	*	*	*	*	*	*	*	*
GND													
P3													

Function	Connector or Header	Description
GPIO	**TP7, TP10**	TP7 and TP10 header blocks connect to the DSP daughterboard for GPIO test points and future flexibility. See the specific daughterboard schematics to determine which DSP signals are available at each header.

TP7: GP TP1–8				**TP10**: GP TP9–16			
TP1	*	*	TP8	TP9	*	*	TP16
TP2	*	*	TP7	TP10	*	*	TP15
TP3	*	*	TP6	TP11	*	*	TP14
TP4	*	*	TP5	TP12	*	*	TP13

Function	Connector or Header	Description
USB (for debugging)	**J2**	The J2 connector is used in conjunction with the SDI software to debug a DSP using USB communications. For the correct jumper settings to use the USB interface, see JP6 on page 2-4.
RS-232 (for debugging)	**J3**	The J3 connector can be used in conjunction with the SDI software for debugging or for in-field updating of the on-board microcontroller code. For the correct jumper settings to use the J3 connector for debugging, see JP6 on page 2-4 and JP8 on page 2-5.
Parallel Port (for debugging)	**J4**	The J4 connector is used with the on-board Parallel Port Command Converter. For the correct jumper settings to use the J4 connector, see JP9 on page 2-5.
Microphone Inputs	**J9, J10**	There are two microphone inputs (MIC1, MIC2) available at one-eighth-inch microphone connectors J9 and J10. These two microphone inputs can also be monitored using headphones by selecting MIC1 and MIC2 to be ON via switches SW2 and SW3. The input levels of the two microphone inputs can be adjusted with the RV1 and RV2 potentiometers (labeled MIC1 LEVEL and MIC2 LEVEL). **CAUTION** If one-fourth-inch to one-eighth-inch adaptors are used for the microphone connection, use only Stereo-Stereo or Mono-Mono style adapters. **Do not use Stereo-Mono or Mono-Stereo adapters** because that will short the incoming audio signal to ground.
Analog Outputs	**J11, J12**	Fixed pre-amp outputs (Variable through Digital Volume control on the DSP) are provided for 12 channels of output. These RCA connections can be routed into a variable or fixed amplifier stage. Please verify signal integrity *before* connecting to high power fixed amplifiers, to avoid audible noise or speaker damage. These outputs are located at J11 and J12. Refer to the board schematics to determine which signals are available at each connector.
Headphone Outputs	**J13**	The 12 analog output channels can also be monitored with the on-board headphone amplifier. To select which channel to listen to, use switches SW2 and SW3. Moving the switch to the right will enable the corresponding channel. There are also right and left volume sliders (RV3 and RV4) to adjust volume and balance. Plug the headphones into the J13 connector (one-eighth-inch).

DSPAUDIOEVM with DSP56720DB, DSP56721DB, DSP56724DB, or DSP56725DB User's Guide, Rev. 4

Chapter 3
Configuring the DSP56720/DSP56724 Daughterboard

There are 15 jumper sets and two DIP switches on the daughterboard that allow you to select various board configurations. Table 3-1 describes how to use this chapter's sections to configure your daughterboard.

Table 3-1. Configuring the DSP56720/DSP56724 Daughterboard

	Step	For information about...	Go to
1	Meet the DSP56720/DSP56724 daughterboard	Section 3.1, "DSP56720/DSP56724 Daughterboard Overview"	on page 3-1
2	Configure jumpers	Section 3.2, "Configuring Control Jumpers"	on page 3-1
3	Configure DIP switches	Section 3.3, "Configuring DIP Switches"	on page 3-5

3.1   DSP56720/DSP56724 Daughterboard Overview

The DSP56720/DSP56724 daughterboard connects to the DSPAUDIOEVM evaluation motherboard (EVM) using two 96-pin connectors. The daughterboard includes several types of external memories:

- 8M ($2 \times 2M \times 16$-bit $\times 4$ bank devices) of SDRAM
- 512K ($3 \times 512K \times 8$-bit devices) of SRAM
- 128K ($3 \times 128K \times 8$-bit devices) of FLASH
- 256 Mbyte I^2C EEPROM
- 256 Mbyte SPI EEPROM

Also included are multiple switches, jumpers, and headers that allow multiple board configurations.

3.2   Configuring Control Jumpers

Set or verify the settings of the jumpers on the daughterboard, using the tables and figures in this section.

Table 3-2 lists the jumpers on the daughterboard; see Figure 3-1 for the location of the jumpers.
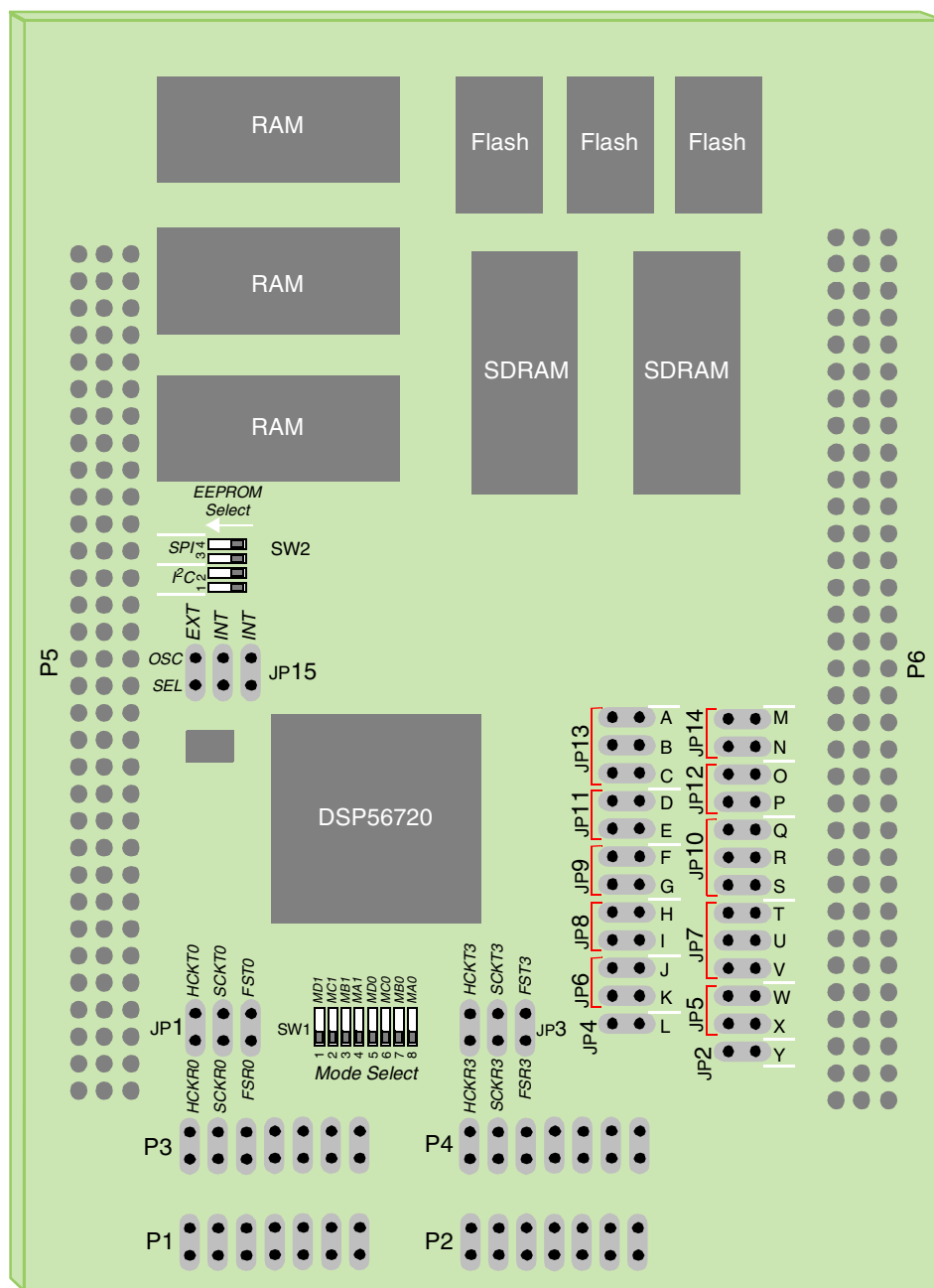

Figure 3-1. DSP56720/DSP56724 Daughterboard Jumpers and Switches Location

Table 3-2. DSP56720/DSP56724 Daughterboard Jumpers and Switches

Function	Jumper	Position	Description
Sync Core-0 ESAI TX and RX Clocks JP1 HCKR0 ● ● HCKT0 SCKR0 ● ● SCKT0 FSR0 ● ● FST0	JP1		Allows you to short corresponding transmit and receive clocks together for Core-0 ESAI.
		HCKR0–HCKT0	Jumper across 1–2 connects Core-0's Receiver High Frequency clock (HCKR) to its Transmitter High Frequency clock (HCKT).
		SCKR0–SCKT0	Jumper across 3–4 connects Core-0's Receiver Serial Bit clock (SCKR) to its Transmitter High Frequency clock (SCKT).
		FSR0–FST0	Jumper across 5–6 connects Core-0's Receiver Frame Sync signal (FSR) to its Transmitter Frame Sync signal (FST).
DAC Muting Control over GPIO JP2 ● ● Y	JP2		Allows you to control muting of the motherboard DACs by GPIO of the DSP.
		Y	Jumper in position Y connects the GPIO LA1 signal to the DAC mute signal.
Sync Core-1 ESAI TX and RX clocks JP3 HCKR3 ● ● HCKT3 SCKR3 ● ● SCKT3 FSR3 ● ● FST3	JP3		Allows you to short corresponding transmit and receive clocks together for Core-1 ESAI.
		HCKR3–HCKT3	Jumper across 1–2 connects Core-1's Receiver High Frequency clock (HCKR) to its Transmitter High Frequency clock (HCKT).
		SCKR3–SCKT3	Jumper across 3–4 connects Core-1's Receiver Serial Bit clock (SCKR) to its Transmitter High Frequency clock (SCKT).
		FSR3–FST3	Jumper across 5–6 connects Core-1's Receiver Frame Sync signal (FSR) to its Transmitter Frame Sync signal (FST).
Connect DSP Watchdog Timer to Reset Circuit JP4 ● ● L	JP4		Allows you to connect the DSP watchdog timer into the daughterboard reset circuit.
		1–2	Jumper across 1–2 connects DSP watchdog timer into the daughterboard reset circuit.
Set Single/Double Speed on Motherboard JP5 ● ● ● ● X W	JP5		Controls the single/double speed option of the Motherboard. No jumper in position W or X sets the Motherboard to single speed.
		W	Jumper in position W selects double speed.
		X	Jumper in position X allows the DSP to control the option via GPIO (LA0).
Select DAC1–3 L/R Clock Source JP6 ● ● ● ● K J	JP6		Selects the source of the DAC1-3 L/R clock.
		J	Jumper in position J selects Core-0 source (FST).
		K	Jumper in position K selects Core-1 source (FST_3).
Select DAC1–3 Serial Data Source JP7 ● ● ● ● ● ● V U T	JP7		Selects the serial data source for channels 5/6 of DAC1-3.
		T	Jumper in position T selects SDO4_0 as source.
		U	Jumper in position U selects SDO5_0 as source.
		V	Jumper in position V selects SDO5_2 as source.

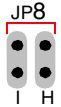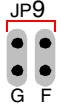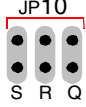**Table 3-2. DSP56720/DSP56724 Daughterboard Jumpers and Switches (continued)**
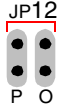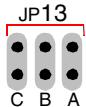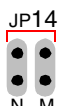
Function	Jumper	Position	Description
Select DAC1–3 Bit Clock Source JP8 I H	JP8		Selects the source for the DAC1-3 bit clock.
		H	Jumper in position H selects Core-0 source (SCKT).
		I	Jumper in position I selects Core-1 source (SCKT_3).
Select DAC1–3 Master Clock Source JP9 G F	JP9		Selects the source for the DAC1-3 master clock.
		F	Jumper in position F selects Core-0 source (HCKT).
		G	Jumper in position G selects Core-1 source (HCKT_3).
Select Routing of Incoming Audio Streams JP10 S R Q	JP10		Controls the routing of incoming serial audio streams from the Motherboard SPDIF receiver and ADCs.
		Q	Route DSP_SD05_1 to RX_SDTO
		R	Route DSP_SD04_1 to ADC1_SDTO
		S	Route DSP_SD03_1 to ADC2_SDTO
Select Motherboard SPDIF TX Master Clock Source JP11 E D	JP11		Selects the source for the Motherboard SPDIF transmitter master clock.
		D	Jumper in position D selects Core-0 source (HCKT).
		E	Jumper in position E selects Core-1 source (HCKT_3).
Select Motherboard SPDIF RX and ADC L/R Clock Sources JP12 P O	JP12		Controls routing of the Motherboard SPDIF receiver and ADC L/R clocks to/from FSR.
		O	Jumper in position O selects the Motherboard SPDIF receiver as source for the Core-0 L/R clock.
		P	Jumper in position P allows either the Motherboard SPDIF receiver or Core-0 to be the source of the L/R clock to the Motherboard ADCs.
Select Motherboard SPDIF RX and ADC Master Clock Sources JP13 C B A	JP13		Controls routing of the Motherboard SPDIF receiver and ADC master clocks to/from HCKR.
		A	Jumper in position A selects the Motherboard SPDIF receiver master clock 1 as the source of the Core-0 master clock.
		B	Jumper in position B selects the Motherboard SPDIF receiver master clock 2 as the source of the Core-0 master clock.
		C	Jumper in position C allows either of the Motherboard SPDIF receiver master clocks or Core-0 to be the source for the Motherboard ADC master clock.
Select Motherboard SPDIF RX and ADC Bit Clock Sources JP14 N M	JP14		Controls routing of the Motherboard SPDIF receiver and ADC bit clocks to/from SCKR.
		M	Jumper in position M selects the Motherboard SPDIF receiver as the source of the Core-0 bit clock.
		N	Jumper in position N allows either the Motherboard SPDIF receiver or Core-0 to be the source of the bit clock to the Motherboard ADCs.

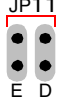**Table 3-2. DSP56720/DSP56724 Daughterboard Jumpers and Switches (continued)**

Function	Jumper	Position	Description
Select DSP Core Input Clock Source JP15 ● ● ● EXT ● ● ● INT ● ● ● INT	JP15		Controls sourcing for the DSP core input clock.
		EXT	Jumper in position EXT selects the 24.576 MHz oscillator on the Motherboard as the source.
		INT	Jumpers in either INT position select the internal DSP oscillator using the 24.575 MHz crystal on the daughterboard as the source. Both INT jumpers must must be placed to use the internal oscillator.
		INT	

3.3 Configuring DIP Switches

There are two DIP switches on the daughterboard: SW1 and SW2.

Table 3-3. DSP56720DB/DSP56724DB Switches

Function	Jumper	Step	For information about...	Go to
Mode Select	SW1	Selects the boot mode for each DSP core.	Section 3.3.1, "SW1: DSP Boot Mode Select"	on page 3-5
Memory Select	SW2	Allows selection of either the SPI or I^{2}C boot EEPROM.	Section 3.3.2, "SW2: EEPROM Select"	on page 3-6

3.3.1 SW1: DSP Boot Mode Select

There are two DSP cores in the device. You can select the boot-up mode for each core separately and independently, using the SW1 DIP switch:

- SW1 switches 1–4 control Core-1's boot mode.
- SW1 switches 5–8 control Core-0's boot mode.

A switch in the ON position means the correlating signal (mode pin) is pulled high.

There are 9 possible modes of operation for a core. Use Table 3-4 to configure SW1.

In Table 3-4, the mode pins (MD, MC, MB, MA) directly map to SW1 switches (1, 2, 3, 4) for Core-1, and to SW1 switches (5, 6, 7, 8) for Core-0.

Table 3-4. DSP56720/DSP56724 Bootstrap Modes

SW1
Core-1 1 MD1 / 2 MC1 / 3 MB1 / 4 MA1
Core-0 5 MD0 / 6 MC0 / 7 MB0 / 8 MA0
Mode Select

Mode	Mode Variables/Switch Positions (x=1 for Core-1, x=0 for Core-0)				Description MD1|MC1|MB1|MA1 for Core-1 or SW1 switches 1|2|3|4 MD0|MC0|MB0|MA0 for Core-0 or SW1 switches 5|6|7|8
	MDx 1 or 5	MCx 2 or 6	MBx 3 or 7	MAx 4 or 8	
0	0	0	0	0	Boot via SHI (SPI)
1	0	0	0	1	Boot via SHI (I^{2}C filter)
2	0	0	1	0	Jump to PROM (SPI)
3	0	0	1	1	Jump to PROM (I^{2}C filter)

DSPAUDIOEVM with DSP56720DB, DSP56721DB, DSP56724DB, or DSP56725DB User's Guide, Rev. 4

Table 3-4. DSP56720/DSP56724 Bootstrap Modes (continued)

SW1

Core-1
1 MD1
2 MC1
3 MB1
4 MA1

Core-0
5 MD0
6 MC0
7 MB0
8 MA0

Mode Select

Mode	Mode Variables/Switch Positions (x=1 for Core-1, x=0 for Core-0)				Description MD1|MC1|MB1|MA1 for Core-1 or SW1 switches 1|2|3|4 MD0|MC0|MB0|MA0 for Core-0 or SW1 switches 5|6|7|8
	MDx 1 or 5	MCx 2 or 6	MBx 3 or 7	MAx 4 or 8	
4	0	1	0	0	Boot from the other core
5	0	1	0	1	Boot via SHI, master (SPI EEPROM)
6	0	1	1	0	Boot via SHI, master (I^2C EEPROM)
7	0	1	1	1	Boot via GPIO, master (SPI EEPROM)
8	1	0	0	0	Boot via external memory word-wide
9	1	0	0	1	Boot via external memory byte-wide
A	1	0	1	0	Reserved
B	1	0	1	1	Reserved
C	1	1	0	0	Reserved
D	1	1	0	1	Reserved
E	1	1	1	0	Reserved
F	1	1	1	1	Reserved

Note: Mode 7 is not supported by the daughtercard hardware.

3.3.2   SW2: EEPROM Select

The daughterboard provides a choice of using two types of serial EEPROM memory: SPI or I^2C. Configure SW2 to select the type of EEPROM (SPI or I^2C) to use.

- To enable the I^2C EEPROM, set SW2 switches 1 and 2 to ON.
- To enable the SPI EEPROM, set SW2 switches 3 and 4 to ON.

The switches must be set in mutually exclusive pairs: 1 and 2 or 3 and 4 for correct operation of the selected EEPROM. When you are working with the SDI debugger, all four switches should be in the OFF position.

I^2C SPI

1 2 3 4

EEPROM Select

SW2

Chapter 4
Configuring the DSP56721/DSP56725 Daughterboard

There are 15 jumper sets and two DIP switches on the DSP56721/DSP56725 daughterboard that allow you to select various board configurations. Table 4-1 describes how to use this chapter's sections to configure your daughterboard.

Table 4-1. Configuring the DSP56721/DSP56725 Daughterboard

	Step	For information about...	Go to
1	Meet the DSP56721/DSP56725 daughterboard	Section 4.1, "DSP56721/DSP56725 Daughterboard Overview"	on page 4-1
2	Configure jumpers	Section 4.2, "Configuring Control Jumpers"	on page 4-1
3	Configure DIP switches	Section 4.3, "Configuring DIP Switches"	on page 4-6

4.1 DSP56721/DSP56725 Daughterboard Overview

The DSP56721/DSP56725 daughterboard connects to the DSPAUDIOEVM evaluation motherboard (EVM) using two 96-pin connectors. The daughterboard includes two serial EEPROM memories:

- 256 Mbyte I2C EEPROM
- 256 Mbyte SPI EEPROM

Also included are multiple switches, jumpers, and headers that allow multiple board configurations.

NOTE

The DSP56721 is available in an 80-pin package and a 144-pin package. Functional limitations with regard to the daughterboard design for each package are described in this chapter.

The DSP56725 is available only in the 80-pin package.

4.2 Configuring Control Jumpers

Set or verify the settings of the jumpers on the daughterboard, using the tables and figures in this section.

Table 4-2 lists the jumpers on the daughterboard; to locate the jumpers, refer to Figure 4-1.
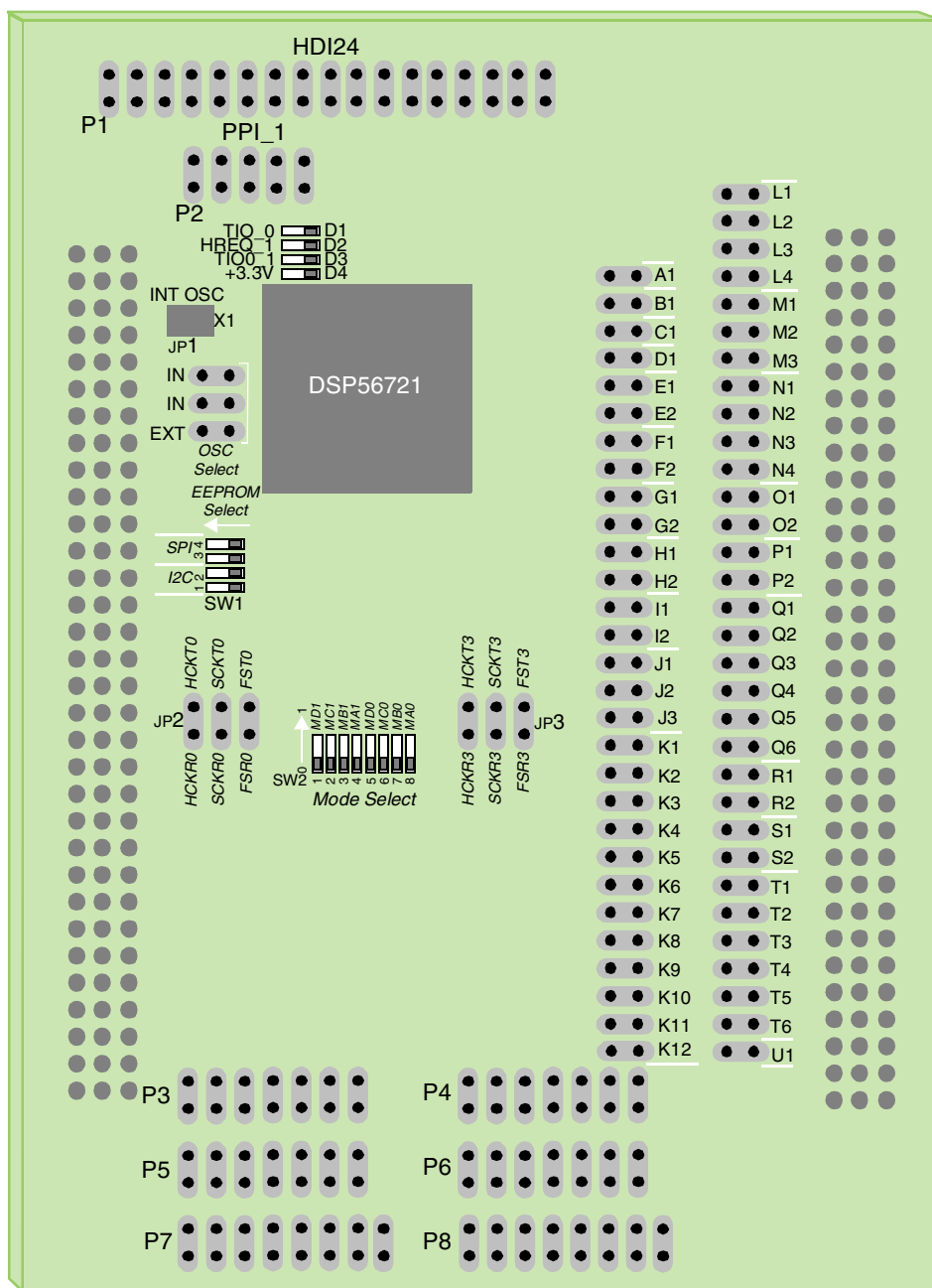

Figure 4-1. DSP56721/DSP56725 Daughterboard Jumpers and Switches Location

Table 4-2. DSP56721/DSP56725 Daughterboard Jumpers and Switches

Function	Jumper	Position	Description
JP1 INT INT EXT	JP1	**INT, INT**	Jumpered when using the internal DSP oscillator as the core clock source referenced from the 24.576MHz crystal X1.
		EXT	Jumpered when using the 24.576MHz oscillator on the motherboard as the core clock source.
JP2 HCKR0 — HCKT0 SCKR0 — SCKT0 FSR0 — FST0	JP2		Used to short the ESAI_0 transmit clocks to the ESAI_0 receive clocks.
JP3 HCKR3 — HCKT3 SCKR3 — SCKT3 FSR3 — FST3	JP3		Used to short the ESAI_3 transmit clocks to the ESAI_3 receive clocks.
A1	A	A1	**Used only with the 144-pin package.** When jumpered, SHI_0 and SHI_1 data and clock signals are bussed together, allowing use of the SDI debugger through the motherboard. When not jumpered, SHI_0 is routed to the motherboard and SHI_1 is routed to the PPI_1 header on the daughterboard.
B1	B	B1	When jumpered allows connection of the DSPs internal S/PDIF receivers to the motherboard S/PDIF connectors. (link to the JP4 table in the motherboard section)
C1	C	C1	**Used only with the 144-pin package.** Must be placed when jumper A1 is placed to allow use of the SDI debugger.
D1	D	D1	When jumpered, allows connection of the DSPs internal S/PDIF receivers to the motherboard S/PDIF connectors. (link to the JP4 table in the motherboard section)
E E1 E2	E	E1	Connects HCKT_0 to the AK4101 motherboard S/PDIF transmitter master clock input.
		E2	Connects HCKT_3 to the AK4101 motherboard S/PDIF transmitter master clock input.
F F1 F2	F	F1	Connects HCKT_0 to the AK4101 motherboard S/PDIF transmitter master clock input.
		F2	Connects HCKT_3 to the AK4101 motherboard S/PDIF transmitter master clock input.
G G1 G2	G	G1	When jumpered, places the motherbaord in double speed mode.
		G2	When jumpered, allows the DSP to control the single or double speed mode of the motherboard via GPIO.
H H1 H2	H	H1	Connects FST_0 to the AK4101 motherboard S/PDIF transmitter L/R clock input.
		H2	Connects FST_3 to the AK4101 motherboard S/PDIF transmitter L/R clock input.

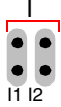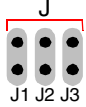**Table 4-2. DSP56721/DSP56725 Daughterboard Jumpers and Switches (continued)**
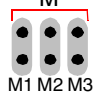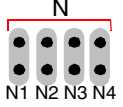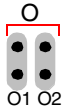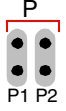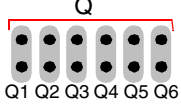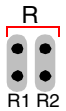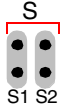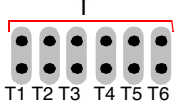
Function	Jumper	Position	Description
I I1 I2	I	I1	**Used only with the 80-pin package.** This jumper must be placed to use the internal S/PDIF reciever in the 80-pin package. Ensure there are no conflicting signals by removing jumpers T1 and K1.
		I2	**Used only with the 80-pin package.** This jumper must be placed to use the internal S/PDIF transmitter in the 80-pin package. Ensure there are no conflicting signals by removing jumpers T3 and K3.
J J1 J2 J3	J	J1	Connects SDI0_1 to the AK4114 motherboard S/PDIF receiver serial data output.
		J2	Connects SDI1_1 to the motherboard AK5380 ADC1 serial data output (AIN1 connector).
		J3	Connects SDI2_1 to the motherboard AK5380 ADC2 serial data output (MIC1 & MIC2 connectors).
K K1 K2 K3 K4 K5 K6 K7 K8 K9 K10 K11 K12	K	K1 K3 K5 K7 K9 K11	Connects ESAI_2 transmitters to the motherboard AK4101 S/PDIF transmitter. See the descriptions of JP1 and JP2 on the motherboard.
		K2 K4 K6 K8 K10 K12	Connects ESAI_0 transmitters to the motherboard AK4101 S/PDIF transmitter. See the descriptions of JP1 and JP2 on the motherboard.
L L1 L2 L3 L4	L	L1	Connects FSR_0 to the AK4114 motherboard S/PDIF receiver L/R clock output.
		L2	Connects FSR_1 to the AK4114 motherboard S/PDIF receiver L/R clock output.
		L3	Connects FSR_0 to both motherboard AK5380 ADCs L/R clock inputs.
		L4	Connects FSR_1 to both motherboard AK5380 ADCs L/R clock inputs.
M M1 M2 M3	M	M1	Connects HCKR_0 to the AK4114 motherboard S/PDIF receiver MCLK01 master clock output.
		M2	Connects HCKR_0 to the AK4114 motherboard S/PDIF receiver MCLK02 master clock output.
		M3	Connects HCKR_0 to both motherboard AK5380 ADCs master clock inputs.
N N1 N2 N3 N4	N	N1	Connects SCKR_0 to the motherboard AK4114 S/PDIF receiver bit clock output.
		N2	Connects SCKR_1 to the motherboard AK4114 S/PDIF receiver bit clock output.
		N3	Connects SCKR_0 to both motherboard AK5380 ADCs bit clock inputs.
		N4	Connects SCKR_1 to both motherboard AK5380 ADCs bit clock inputs.

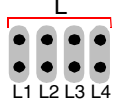**Table 4-2. DSP56721/DSP56725 Daughterboard Jumpers and Switches (continued)**

Function	Jumper	Position	Description
O O1 O2	O	O1	Connects SCKT_0 to the motherboard AK4355 DACA bit clock input.
		O2	Connects SCKT_1 to the motherboard AK4355 DACA bit clock input.
P P1 P2	P	P1	Connects FST_0 to the motherboard AK4355 DACA L/R clock input.
		P2	Connects FST_1 to the motherboard AK4355 DACA L/R clock input.
Q Q1 Q2 Q3 Q4 Q5 Q6	Q	Q1	Connects SDO2_0 to the motherboard AK4355 DACA serial data input 1.
		Q2	Connects SDO2_1 to the motherboard AK4355 DACA serial data input 1.
		Q3	Connects SDO2_0 to the motherboard AK4355 DACA serial data input 2.
		Q4	Connects SDO2_1 to the motherboard AK4355 DACA serial data input 2.
		Q5	Connects SDO2_0 to the motherboard AK4355 DACA serial data input 3.
		Q6	Connects SDO2_2 to the motherboard AK4355 DACA serial data input 3.
R R1 R2	R	R1	Connects SCKT_2 to the motherboard AK4355 DACB bit clock input
		R2	Connects SCKT_3 to the motherboard AK4355 DACB bit clock input
S S1 S2	S	S1	Connects FST_2 to the motheboard AK4355 DACB L/R clock input.
		S2	Connects FST_3 to the motheboard AK4355 DACB L/R clock input
T T1 T2 T3 T4 T5 T6	T	T1	Connects SDO2_2 to the motherboard AK4355 DACB serial data input 1.
		T2	Connects SDO2_3 to the motherboard AK4355 DACA serial data input 1.
		T3	Connects SDO2_2 to the motherboard AK4355 DACA serial data input 2.
		T4	Connects SDO2_3 to the motherboard AK4355 DACA serial data input 2.
		T5	Connects SDO2_2 to the motherboard AK4355 DACA serial data input 3.
		T6	Connects SDO2_3 to the motherboard AK4355 DACA serial data input 3.
U1	U	U1	When jumpered, allows the DSP to control the mute fucntion of the motherboard via GPIO.

DSPAUDIOEVM with DSP56720DB, DSP56721DB, DSP56724DB, or DSP56725DB User's Guide, Rev. 4

4.3   Configuring DIP Switches

There are two DIP switches on the daughterboard: SW1 and SW2. Configure or confirm the settings on the SW1 and SW2 DIP switches.

Table 4-3. DSP56721/DSP56725 Daughterboard Switches

Function	Jumper	Step	For information about...	Go to
Memory Select	SW1	Allows selection of either the SPI or I²C boot EEPROM.	Section 4.3.1, "SW1: EEPROM Select"	on page 4-6
Mode Select	SW2	Selects the boot mode for each DSP core.	Section 4.3.2, "SW2: DSP Boot Mode Select"	on page 4-6

4.3.1   SW1: EEPROM Select

The DSP56721/DSP56725 daughterboard provides a choice of two types of serial EEPROM memory: SPI or I2C. Configure SW1 to select the type of EEPROM (SPI or I2C) to use.

-   To enable the I2C EEPROM, set SW1 switches 1 and 2 to ON.
-   To enable the SPI EEPROM, set SW1 switches 3 and 4 to ON.

The switches must be set in mutually exclusive pairs: 1 and 2 or 3 and 4 for correct operation of the selected EEPROM.

4.3.2   SW2: DSP Boot Mode Select

There are two DSP cores in the DSP56721/DSP56725 device. You can select the boot-up mode for each core separately and independently, using the SW2 DIP switch:

-   SW2 switches 1–4 control Core-1's boot mode.
-   SW2 switches 5–8 control Core-0's boot mode.

A switch in the ON position means the correlating signal (mode pin) is pulled high. The mode pins are all MOD*x*, where *x* is A, B, C, or D.

There are 11 possible modes of operation for a DSP56721/DSP56725 core. Use Table 4-4 to configure SW2.

In Table 4-4, the mode pins (MD, MC, MB, MA) directly map to SW2 switches (1, 2, 3, 4) for Core-1, and to SW2 switches (5, 6, 7, 8) for Core-0.

Table 4-4. DSP56721/DSP56725 Bootstrap Modes

SW2

Core-1

1 MD1
2 MC1
3 MB1
4 MA1

Core-0

5 MD0
6 MC0
7 MB0
8 MA0

Mode Select

Mode	Mode Variables/Switch Positions (x=1 for Core-1, x=0 for Core-0)				Description MD1|MC1|MB1|MA1 for Core-1 or SW1 switches 1|2|3|4 MD0|MC0|MB0|MA0 for Core-0 or SW1 switches 5|6|7|8
	MDx 1 or 5	**MCx 2 or 6**	**MBx 3 or 7**	**MAx 4 or 8**	
0	0	0	0	0	Boot via SHI (SPI)
1	0	0	0	1	Boot via SHI (I^2C filter)
2	0	0	1	0	Jump to PROM (SPI)
3	0	0	1	1	Jump to PROM (I^2C filter)
4	0	1	0	0	Boot from the other core
5	0	1	0	1	Boot via SHI, master (SPI EEPROM)
6	0	1	1	0	Boot via SHI, master (I^2C EEPROM)
7	0	1	1	1	Boot via GPIO, master (SPI EEPROM)
8	1	0	0	0	Reserved
9	1	0	0	1	Reserved
A	1	0	1	0	Reserved
B	1	0	1	1	Reserved
C	1	1	0	0	Boot via HDI24 in ISA mode
D	1	1	0	1	Boot via HDI24 in HC11 mode
E	1	1	1	0	Boot via HDI24 in 8051 mode
F	1	1	1	1	Boot via HDI24 in 68302 mode

Note: Mode 7 is not supported by the daughterboard hardware. Modes C, D, E and F are not supported by the DSP56721 80-pin package or by the DSP56725.

Chapter 5
Getting Started

Two options are available to bring up the EVM system and run it in a demonstration mode. The EVM can do the following:

- Can run a self-test on the external SRAM and SDRAM if the daughterboard is equipped (Section 5.1, "Running the External Memory Self-Test")
- Or can perform an audio passthru (Section 5.2, "Running the Audio Passthru Demo")

There is external memory test code already stored in flash memory, and passthru code is resident in both EEPROMs.

5.1   Running the External Memory Self-Test

To run a self-test on the external SRAM and SDRAM, follow the steps shown in Table 5-1.

Table 5-1. Running External Memory Self-Test Procedure

Step	Description	Procedure
1	Configure the motherboard.	No special motherboard configuration is required for this demo.
2	Configure the daughterboard.	Configure Core-0 or Core-1 to boot from external word-wide memory (mode 8).
3	Install the daughterboard onto the motherboard.	• The connectors are keyed to be inserted in one direction only. • Determine the correct orientation and install the daughterboard at this time.
4	Connect the power supply to the motherboard and power up.	• Freescale recommends always using a grounded AC power cord for both improved audio performance and safety. • First connect the power supply to the AC power source, and then connect to the motherboard at the round J1 connector. • When the J1 connector is properly seated, all five of the power LEDs located next to the J1 connector should be illuminated.
5	Watch the AUX LED.	• If the test passes, then the AUX LED will light and remain lighted. • If the test fails, then the AUX LED will flash on and off.
6	Power down.	—

5.2 Running the Audio Passthru Demo

To run a simple audio passthru demo, follow the steps in Table 5-2.

Table 5-2. Running External Memory Self-Test Procedure

	Step	Procedure
1	Configure the motherboard.	Configure JP11 for the audio source input. Make sure that JP8 is set for PPI Port.
2	Configure the daughterboard.	**DSP56720DB/DSP56724DB** **Configure the jumpers** below to properly run the passthru code stored in EEPROM. (This is the factory default, but you should confirm the settings.) • JP15: INT, INT • JP1: all • JP3: all • Jumpers on A, C, D, E, F, G, H, I, J, K, M, N, O, P, Q, T (see Table 3-2) **Configure the switches.** The switches have multiple options depending on which EEPROM you are using, but the bootmode must match the EEPROM selected (for example, if you are using the SPI, the boot SPI EEPROM mode must be selected). **Note:** At this time, only one core can boot and run passthru code; more specifically, only Core-0 can boot from the EEPROM and run passthru code. Core-1 should be set to boot in mode 4 to ensure it does not interfere with the SHI boot communication.
		DSP56721DB/DSP56725DB **Configure the jumpers** below to properly run the passthru code stored in EEPROM. (This is the factory default, but you should confirm the settings.) • JP1: INT, INT • JP2: HCKR0, HCKT0 • JP3: HCKR3, HCKT3 • Jumpers on A1, E1, E2, J1, L1, L3, M2, M3, N1, N3, O1, P1, Q1, Q3, Q5, R2, S2, T1, T3, T5 (see Table 3-2) **Configure the switches.** The switches have multiple options depending on which EEPROM you are using, but the bootmode must match the EEPROM selected (for example, if you are using the SPI, the boot SPI EEPROM mode must be selected). **Note:** At this time, only one core can boot and run passthru code; more specifically, only Core-0 can boot from the EEPROM and run passthru code. Core-1 should be set to boot in mode 4 to ensure it does not interfere with the SHI boot communication.
3	Install the daughterboard onto the motherboard.	• The connectors are keyed to be inserted in one direction only. • Determine the correct orientation and install the daughterboard at this time.
4	Connect external cables and peripherals.	• Connect the audio source to the input selected in step 1. • Connect headphones and select the output channel to monitor and adjust the headphone volume, or connect the line outputs to an amplifier and speaker system.
5	Connect the power supply to the motherboard and power up.	• Freescale recommends always using a grounded AC power cord for both improved audio performance and safety. • First connect the power supply to the AC power source, and then connect to the motherboard at the round J1 connector. • When the J1 connector is properly seated, all five of the power LEDs located next to the J1 connector should be illuminated.
6	Monitor the headphones or lineouts.	Audio should be present on AOUT1-3.
7	Power down.	—

Appendix A
Programming the MCUs

To use the SDI debugger and software architecture, you must first upgrade the DEBUG MPU firmware of the motherboard.

- SDI version 2.5 or newer with the accompanying firmware (available on www.freescale.com) is required to work with any DSP5672x device.
- This SDI and firmware upgrade is backwards-compatible with all previous Symphony DSPs.
- All revision D motherboards ship with the updated firmware for SDI 2.5 already programmed in the DEBUG MPU.

To program the MCUs on the motherboard, follow the steps in Table A-1:

Table A-1. To Program an MCU

Step	Description
1	Section A.1, "Configuring the Motherboard"
2	Section A.2, "Programming the CONFIG MPU (GP32)"
Or	
2	Section A.3, "Programming the DEBUG MPU (JB16)"

Also see Section A.4, "Troubleshooting Tips."

A.1   Configuring the Motherboard

To program an MCU on the motherboard, install a jumper to select which MPU (CONFIG or DEBUG) that you want to program. You can only program one MPU at a time.

1. On the motherboard, place a connecting jumper on the USB/PGM pins at JP6
2. Make sure that there is no jumper at the RS232 pins.
3. Place a connecting jumper on the PGM pins at JP7.
4. Place a connecting jumper on the specific pins that you wish to program:
   to program the 908GP32, place a jumper at the CONFIG MPU pins,
   to program the 908JB16, place a jumper at the DEBUG MPU pins.

CAUTION

There should only be a jumper at the DEBUG MPU pins or at the CONFIG MPU pins. Do not install jumpers on both of these sets of pins at the same time.

A.2   Programming the CONFIG MPU (GP32)

1. Download the programming software from `http://www.pemicro.com/ics08/index.html`. Register to P&E. For the GP32 device: ICS08GPGT software for 68HC908GP32/GT16/GT8 is available in the following location:

    `http://www.pemicro.com/ics08/ics08gpgtz_version_1_42_040202.exe`

2. After you have downloaded the software, run the programmer executive:

    `C:\pemicro\ics08gpgtz\prog08sz.exe`

3. You should now see a pop-up window showing "Attempting to contact target and pass security."

4. Select the following options in Table A-2:

Table A-2. Select These Options

Option	Select
Target Hardware Type	Class III Direct serial to target w/MON08 serial port circuitry built-in
Serial Port	1 (if that is the port that that your PC is using)
Baud	9600 Baud
Target MCU Security bytes	Attempt FF-FF-FF-FF-FF-FF-FF-FF (Blank Device)

5. Check the box "Show this dialog before attempting to contact the 68HC08 board," then click on "Contact target with these settings." You should now see the programming environment and status window display.

6. If prompted, press the RESET button on the board and then click OK.

7. Power the EVM board off and on when prompted, allowing a few seconds for the capacitors to discharge.

8. If communication is successful and monitor mode is passed, next you will be prompted to select a programming algorithm to use. Choose the "`908_gp32.08p`" algorithm.

9. Before programming the GP32 device, the GP32 device must be blank and unsecured. To verify that the V device is blank, double-click the "BM Blank check module." If the GP32 device is not blank or is not unsecured, then execute the "EM Erase module" command before programming the GP32 device.

10. After the GP32 device is verified to be blank and unsecured, next specify the S-Record to be used. Select the S-Record by executing the "SS Specify S Record" command. After the S-Record is specified, you can program the device by executing the "PM Program module" command, followed by the "Verify module" command to confirm that the programming action was successful.

11. Exit the programming program by selecting File/Exit.

A.3   Programming the DEBUG MPU (JB16)

1. Download the programming software from `http://www.pemicro.com/ics08/index.html`. Register to P&E and download the software. For the JB16 device: ICS08JB software for 68HC908JB8 is available at `http://www.pemicro.com/ics08/ics08jbz_version_1_05A_020402.exe`. Note that for programming the JB16, you will also need the `908_jg16.08p` file.

2. After you have downloaded the software, run the programmer executive:

   `C:\pemicro\ics08jbz\prog08sz.exe`

3. You should now see a pop-up window showing "Attempting to contact target and pass security."

4. Select the following options in :

Table A-3. Select These Options

Option	Select
Target Hardware Type	Class III Direct serial to target w/MON08 serial port circuitry built in. (NODTR - No power control)
Serial Port	1 (if that is the port that that your PC is using)
Baud	19200 Baud
Target MCU Security bytes	Attempt FF-FF-FF-FF-FF-FF-FF-FF (Blank Device)

5. Check the box "Show this dialog before attempting to contact the 68HC08 board," then click on "Contact target with these settings." You should now see the programming environment and status window appear.

6. If prompted, press the RESET button on the board and then click OK.

7. Power the EVM board off and on when prompted, allowing a few seconds for the capacitors to discharge.

8. If communication is successful and monitor mode is passed, next you will be prompted to select a programming algorithm to use. Choose the "`908_jg16.08p`" algorithm.

9. Before programming the JB16 device, the JB16 device must be blank and unsecured. To verify that the V device is blank, double-click the "BM Blank check module." If the JB16 device is not blank or is not unsecured, then execute the "EM Erase module" command before programming the JB16 device.

10. After the JB16 device is verified to be blank and unsecured, next specify the S-Record to be used. Select the S-Record by executing the "SS Specify S Record'" command. After the S-Record is specified, you can program the device by executing the "PM Program module" command, followed by the "Verify module" command to confirm that the programming action was successful.

11. Exit the programming program by selecting File/Exit.

A.4 Troubleshooting Tips

Table A-4. Troubleshooting Tips

Status Message	Tips
68HC08 Device responded properly, but ROM is SECURE	• Specify security bytes or select "IGNORE." • Select the option "IGNORE security failure and enter monitor mode." • Now perform a power cycle sequence again. In general, follow the sequence: 1. Erase the device. 2. Unsecure the device. 3. Program the device. Before programming a device, you must first erase the device fully, then second un-secure it.

THIS PAGE INTENTIONALLY LEFT BLANK

THIS PAGE INTENTIONALLY LEFT BLANK