DS92LV090A 9 Channel Bus LVDS Transceiver

Check for Samples: DS92LV090A

FEATURES

- **Bus LVDS Signaling**
- **3.2 nanosecond propagation delay max**
- **Chip to Chip skew ±800ps**
- **Low power CMOS design**
- **High Signaling Rate Capability (above 100 Mbps)**
- **0.1V to 2.3V Common Mode Range for V_{ID} = 200mV**
- **±100 mV Receiver Sensitivity**
- **Supports open and terminated failsafe on port pins**
- **3.3V operation**
- **Glitch free power up/down (Driver & Receiver disabled)**
- **Light Bus Loading (5 pF typical) per Bus LVDS load**
- **Designed for Double Termination Applications**
- **Balanced Output Impedance**
- **Product offered in 64 pin TQFP package**
- **High impedance Bus pins on power off (V_{CC} = 0V)**
- **Driver Channel to Channel skew (same device) 230ps typical**
- **Receiver Channel to Channel skew (same device) 370ps typical**

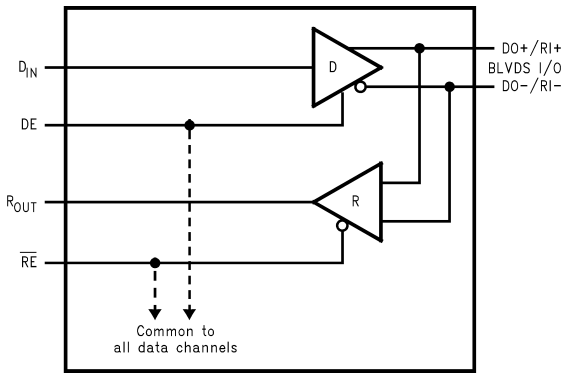
DESCRIPTION

The DS92LV090A is one in a series of Bus LVDS transceivers designed specifically for the high speed, low power proprietary backplane or cable interfaces. The device operates from a single 3.3V power supply and includes nine differential line drivers and nine receivers. To minimize bus loading, the driver outputs and receiver inputs are internally connected. The separate I/O of the logic side allows for loop back support. The device also features a flow through pin out which allows easy PCB routing for short stubs between its pins and the connector.

The driver translates 3V TTL levels (single-ended) to differential Bus LVDS (BLVDS) output levels. This allows for high speed operation, while consuming minimal power with reduced EMI. In addition, the differential signaling provides common mode noise rejection of ±1V.

The receiver threshold is less than ±100 mV over a ±1V common mode range and translates the differential Bus LVDS to standard (TTL/CMOS) levels. (See Applications Information Section for more details.)

Simplified Functional Diagram



Connection Diagram

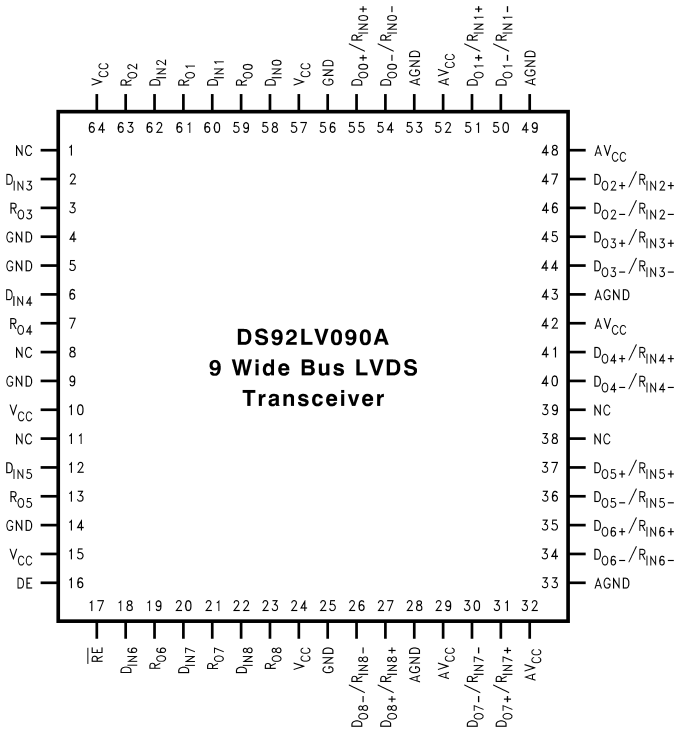


Figure 1. Top View
Order Number DS92LV090ATVEH
See NS Package Number VEH064DB

Pin Functions

Pin Descriptions

Pin Name	Pin #	Input/Output	Descriptions
DO+/RI+	27, 31, 35, 37, 41, 45, 47, 51, 55	I/O	True Bus LVDS Driver Outputs and Receiver Inputs.
DO−/RI−	26, 30, 34, 36, 40, 44, 46, 50, 54	I/O	Complimentary Bus LVDS Driver Outputs and Receiver Inputs.
D_{IN}	2, 6, 12, 18, 20, 22, 58, 60, 62	I	TTL Driver Input.
RO	3, 7, 13, 19, 21, 23, 59, 61, 63	O	TTL Receiver Output.
$\overline{RE}$	17	I	Receiver Enable TTL Input (Active Low).
DE	16	I	Driver Enable TTL Input (Active High).
GND	4, 5, 9, 14, 25, 56	Power	Ground for digital circuitry (must connect to GND on PC board). These pins connected internally.
V_{CC}	10, 15, 24, 57, 64	Power	V_{CC} for digital circuitry (must connect to V_{CC} on PC board). These pins connected internally.
AGND	28, 33, 43, 49, 53	Power	Ground for analog circuitry (must connect to GND on PC board). These pins connected internally.
AV_{CC}	29, 32, 42, 48, 52	Power	Analog V_{CC} (must connect to V_{CC} on PC board). These pins connected internally.
NC	1, 8, 11, 38, 39	N/A	Leave open circuit, do not connect.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

Supply Voltage (V_{CC})	4.0V
Enable Input Voltage	
(DE, $\overline{RE}$)	−0.3V to (V_{CC} +0.3V)
Driver Input Voltage (D_{IN})	−0.3V to (V_{CC} +0.3V)
Receiver Output Voltage	
(R_{OUT})	−0.3V to (V_{CC} +0.3V)
Bus Pin Voltage (DO/RI±)	−0.3V to +3.9V
ESD (HBM 1.5 kΩ, 100 pF)	>4.5 kV
Driver Short Circuit Duration	momentary
Receiver Short Circuit Duration	momentary
Maximum Package Power Dissipation at 25°C	
TQFP	1.74 W
Derate TQFP Package	13.9 mW/°C
θ_{ja}	71.7°C/W
θ_{jc}	10.9°C/W
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
(Soldering, 4 sec.)	260°C

(1) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified except V_{OD}, ΔV_{OD} and V_{ID}.
(2) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	3.0	3.6	V
Receiver Input Voltage	0.0	2.4	V
Operating Free Air Temperature	−40	+85	°C
Maximum Input Edge Rate			
(1)(20% to 80%)			Δt/ΔV
Data		1.0	ns/V
Control		3.0	ns/V

(1) Generator waveforms for all tests unless otherwise specified: f = 25 MHz, Z_O = 50Ω, t_r, t_f = <1.0 ns (0%–100%). To ensure fastest propagation delay and minimum skew, data input edge rates should be equal to or faster than 1ns/V; control signals equal to or faster than 3ns/V. In general, the faster the input edge rate, the better the AC performance.

DC Electrical Characteristics

Over recommended operating supply voltage and temperature ranges unless otherwise specified (1) (2)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
V_{OD}	Output Differential Voltage	R_L = 27Ω, Figure 2		DO+/RI+, DO−/RI−	240	300	460	mV
ΔV_{OD}	V_{OD} Magnitude Change						27	mV
V_{OS}	Offset Voltage				1.1	1.3	1.5	V
ΔV_{OS}	Offset Magnitude Change					5	10	mV
V_{OH}	Driver Output High Voltage	R_L = 27Ω				1.4	1.65	V
V_{OL}	Driver Output Low Voltage	R_L = 27Ω			0.95	1.1		V
I_{OSD}	Output Short Circuit Current (3)	V_{OD} = 0V, DE = V_{CC}, Driver outputs shorted together				|36|	|65|	mA
V_{OH}	Voltage Output High (4)	V_{ID} = +300 mV	I_{OH} = −400 µA	R_{OUT}	V_{CC}−0.2			V
		Inputs Open			V_{CC}−0.2			V
		Inputs Terminated, R_L = 27Ω			V_{CC}−0.2			V
V_{OL}	Voltage Output Low	I_{OL} = 2.0 mA, V_{ID} = −300 mV				0.05	0.075	V
I_{OD}	Receiver Output Dynamic Current (3)	V_{ID} = 300mV, V_{OUT} = V_{CC}−1.0V			−110	|75|		mA
		V_{ID} = −300mV, V_{OUT} = 1.0V				|75|	110	mA
V_{TH}	Input Threshold High	DE = 0V, V_{CM} = 1.5V		DO+/RI+, DO−/RI−			+100	mV
V_{TL}	Input Threshold Low				−100			mV
V_{CMR}	Receiver Common Mode Range				$\|V_{ID}\|/2$		2.4 − $\|V_{ID}\|/2$	V
I_{IN}	Input Current	DE = 0V, $\overline{RE}$ = 2.4V, V_{IN} = +2.4V or 0V			−20	±1	+20	µA
		V_{CC} = 0V, V_{IN} = +2.4V or 0V			−20	±1	+20	µA
V_{IH}	Minimum Input High Voltage			D_{IN}, DE, $\overline{RE}$	2.0		V_{CC}	V
V_{IL}	Maximum Input Low Voltage				GND		0.8	V
I_{IH}	Input High Current	V_{IN} = V_{CC} or 2.4V			−20	±10	+20	µA
I_{IL}	Input Low Current	V_{IN} = GND or 0.4V			−20	±10	+20	µA
V_{CL}	Input Diode Clamp Voltage	I_{CLAMP} = −18 mA			−1.5	−0.8		V
I_{CCD}	Power Supply Current Drivers Enabled, Receivers Disabled	No Load, DE = $\overline{RE}$ = V_{CC}, DIN = V_{CC} or GND		V_{CC}		55	80	mA
I_{CCR}	Power Supply Current Drivers Disabled, Receivers Enabled	DE = $\overline{RE}$ = 0V, V_{ID} = ±300mV				73	80	mA
I_{CCZ}	Power Supply Current, Drivers and Receivers TRI-STATE®	DE = 0V; $\overline{RE}$ = V_{CC}, DIN = V_{CC} or GND				35	80	mA
I_{CC}	Power Supply Current, Drivers and Receivers Enabled	DE = V_{CC}; $\overline{RE}$ = 0V, DIN = V_{CC} or GND, R_L = 27Ω				170	210	mA
I_{OFF}	Power Off Leakage Current	V_{CC} = 0V or OPEN, D_{IN}, DE, $\overline{RE}$ = 0V or OPEN, $V_{APPLIED}$ = 3.6V (Port Pins)		DO+/RI+, DO−/RI−	−20		+20	µA
C_{OUTPUT}	Capacitance @ Bus Pins			DO+/RI+, DO−/RI−		5		pF
c_{OUTPUT}	Capacitance @ R_{OUT}			R_{OUT}		7		pF

(1) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified except V_{OD}, ΔV_{OD} and V_{ID}.
(2) All typicals are given for V_{CC} = +3.3V and T_A = +25°C, unless otherwise stated.
(3) Only one output at a time should be shorted, do not exceed maximum package power dissipation capacity.
(4) V_{OH} failsafe terminated test performed with 27Ω connected between RI+ and RI− inputs. No external voltage is applied.

AC Electrical Characteristics

Over recommended operating supply voltage and temperature ranges unless otherwise specified (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIFFERENTIAL DRIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Prop. Delay High to Low (2)	R_L = 27Ω, Figure 3 Figure 4, C_L = 10 pF	0.6	1.4	2.2	ns
t_{PLHD}	Differential Prop. Delay Low to High (2)		0.6	1.4	2.2	ns
t_{SKD1}	Differential Skew $\|t_{PHLD}–t_{PLHD}\|$ (3)			80		ps
t_{SKD2}	Chip to Chip Skew (4)				1.6	ns
t_{SKD3}	Channel to Channel Skew (5)			0.25	0.45	ns
t_{TLH}	Transition Time Low to High			0.6	1.2	ns
t_{THL}	Transition Time High to Low			0.5	1.2	ns
t_{PHZ}	Disable Time High to Z	R_L = 27Ω, Figure 5 Figure 6, C_L = 10 pF		3	8	ns
t_{PLZ}	Disable Time Low to Z			3	8	ns
t_{PZH}	Enable Time Z to High			3	8	ns
t_{PZL}	Enable Time Z to Low			3	8	ns
DIFFERENTIAL RECEIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Prop. Delay High to Low (2)	Figure 7 Figure 8, C_L = 35 pF	1.6	2.4	3.2	ns
t_{PLHD}	Differential Prop Delay Low to High (2)		1.6	2.4	3.2	ns
t_{SDK1}	Differential Skew $\|t_{PHLD}–t_{PLHD}\|$ (3)			80		ps
t_{SDK2}	Chip to Chip Skew (4)				1.6	ns
t_{SDK3}	Channel to Channel Skew (5)			0.35	0.60	ns
t_{TLH}	Transition Time Low to High			1.5	2.5	ns
t_{THL}	Transition Time High to Low			1.5	2.5	ns
t_{PHZ}	Disable Time High to Z	R_L = 500Ω, Figure 9 Figure 10, C_L = 35 pF		4.5	10	ns
t_{PLZ}	Disable Time Low to Z			3.5	8	ns
t_{PZH}	Enable Time Z to High			3.5	8	ns
t_{PZL}	Enable Time Z to Low			3.5	8	ns

(1) Generator waveforms for all tests unless otherwise specified: f = 25 MHz, Z_O = 50Ω, t_r, t_f = <1.0 ns (0%–100%). To ensure fastest propagation delay and minimum skew, data input edge rates should be equal to or faster than 1ns/V; control signals equal to or faster than 3ns/V. In general, the faster the input edge rate, the better the AC performance.
(2) Propagation delays are guaranteed by design and characterization.
(3) t_{SKD1} $|t_{PHLD}–t_{PLHD}|$ is the worse case skew between any channel and any device over recommended operation conditions.
(4) Chip to Chip skew is the difference in differential propagation delay between any channels of any devices, either edge.
(5) Channel to Channel skew is the difference in driver output or receiver output propagation delay between any channels within a device, either edge.

Applications Information

General application guidelines and hints may be found in the following application notes: AN-808, AN-903, AN-971, AN-977, and AN-1108.

There are a few common practices which should be implied when designing PCB for Bus LVDS signaling. Recommended practices are:

- Use at least 4 PCB board layer (Bus LVDS signals, ground, power and TTL signals).
- Keep drivers and receivers as close to the (Bus LVDS port side) connector as possible.
- Bypass each Bus LVDS device and also use distributed bulk capacitance between power planes. Surface mount capacitors placed close to power and ground pins work best. Two or three high frequency, multi-layer ceramic (MLC) surface mount (0.1 µF, 0.01 µF, 0.001 µF) in parallel should be used between each V_{CC} and ground. The capacitors should be as close as possible to the V_{CC} pin.
  - Multiple vias should be used to connect V_{CC} and Ground planes to the pads of the by-pass capacitors.
  - In addition, randomly distributed by-pass capacitors should be used.
- Use the termination resistor which best matches the differential impedance of your transmission line.
- Leave unused Bus LVDS receiver inputs open (floating). Limit traces on unused inputs to <0.5 inches.

- Isolate TTL signals from Bus LVDS signals

MEDIA (CONNECTOR or BACKPLANE) SELECTION:

- Use controlled impedance media. The backplane and connectors should have a matched differential impedance.

Table 1. Functional Table

MODE SELECTED	DE	$\overline{RE}$
DRIVER MODE	H	H
RECEIVER MODE	L	L
TRI-STATE™ MODE	L	H
LOOP BACK MODE	H	L

Table 2. Transmitter Mode

INPUTS		OUTPUTS	
DE	**D_{IN}**	**DO+**	**DO−**
H	L	L	H
H	H	H	L
H	0.8V< D_{IN} <2.0V	X	X
L	X	Z	Z

Table 3. Receiver Mode

INPUTS		OUTPUT
$\overline{RE}$	**(RI+) – (RI−)**	
L	L (< −100 mV)	L
L	H (> +100 mV)	H
L	−100 mV < V_{ID} < +100 mV	X
H	X	Z

Test Circuits and Timing Waveforms

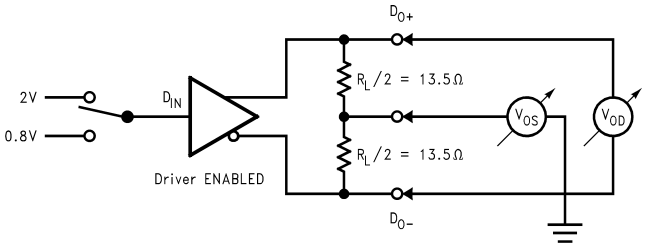


Figure 2. Differential Driver DC Test Circuit

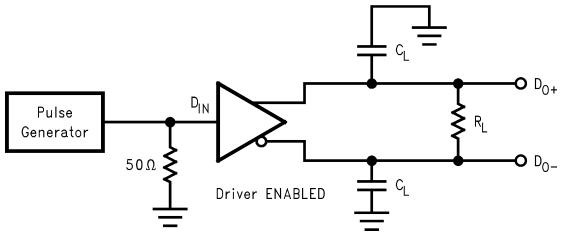


Figure 3. Differential Driver Propagation Delay and Transition Time Test Circuit

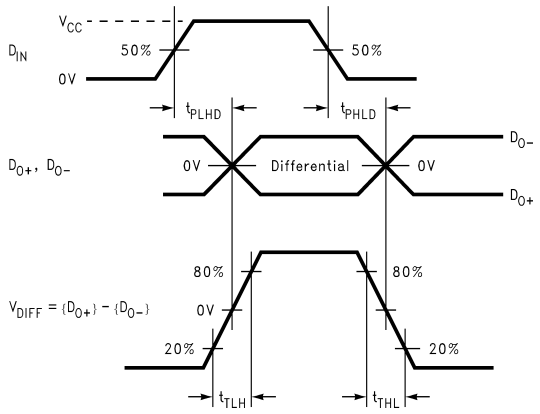


Figure 4. Differential Driver Propagation Delay and Transition Time Waveforms

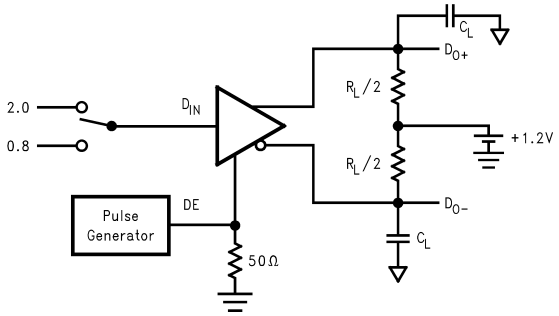


Figure 5. Driver TRI-STATE™ Delay Test Circuit

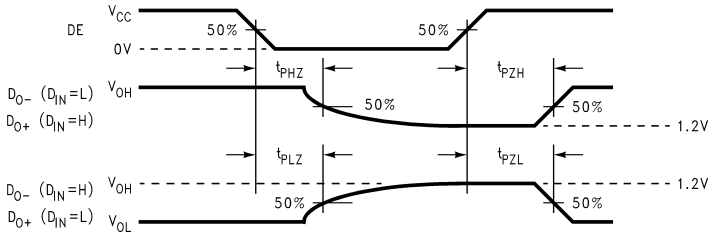


Figure 6. Driver TRI-STATE™ Delay Waveforms

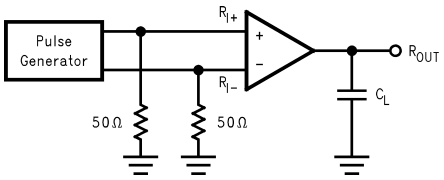


Figure 7. Receiver Propagation Delay and Transition Time Test Circuit

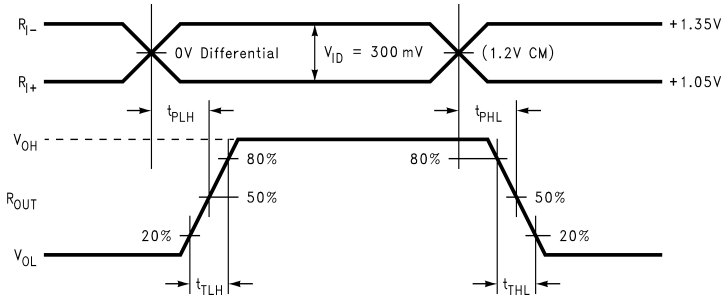


Figure 8. Receiver Propagation Delay and Transition Time Waveforms

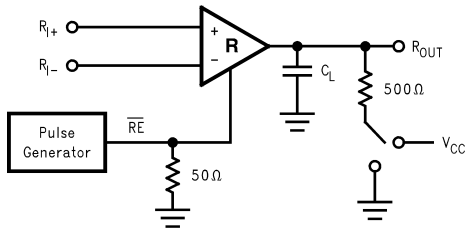


Figure 9. Receiver TRI-STATE™ Delay Test Circuit

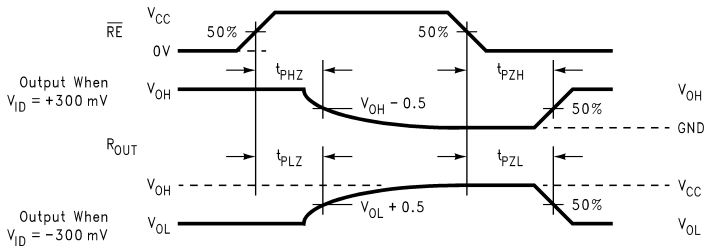


Figure 10. Receiver TRI-STATE™ Delay Waveforms

Typical Bus Application Configurations

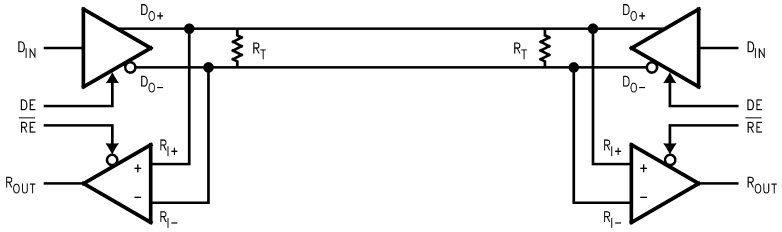


Figure 11. Bi-Directional Half-Duplex Point-to-Point Applications

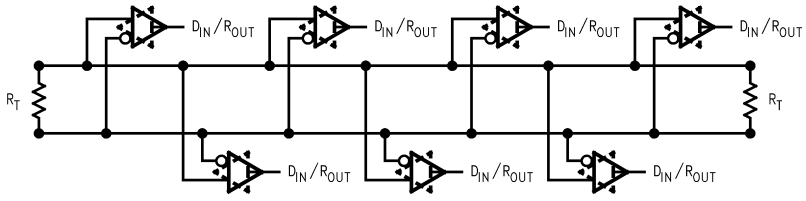


Figure 12. Multi-Point Bus Applications

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS92LV090ATVEH/NOPB	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 85	DS92LV090A TVEH	Samples
DS92LV090ATVEHX/NOPB	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	DS92LV090A TVEH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

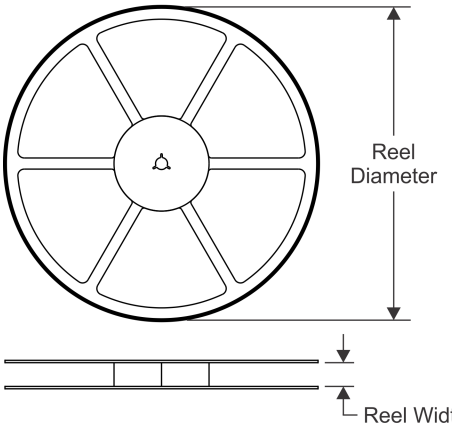
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

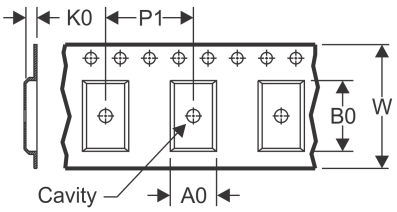
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

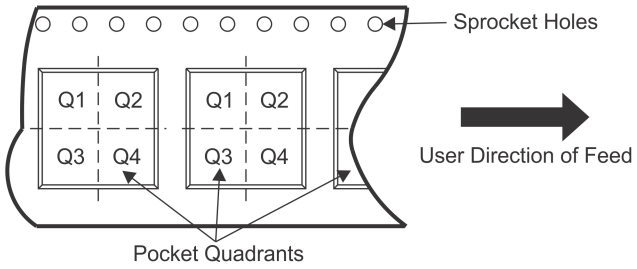


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

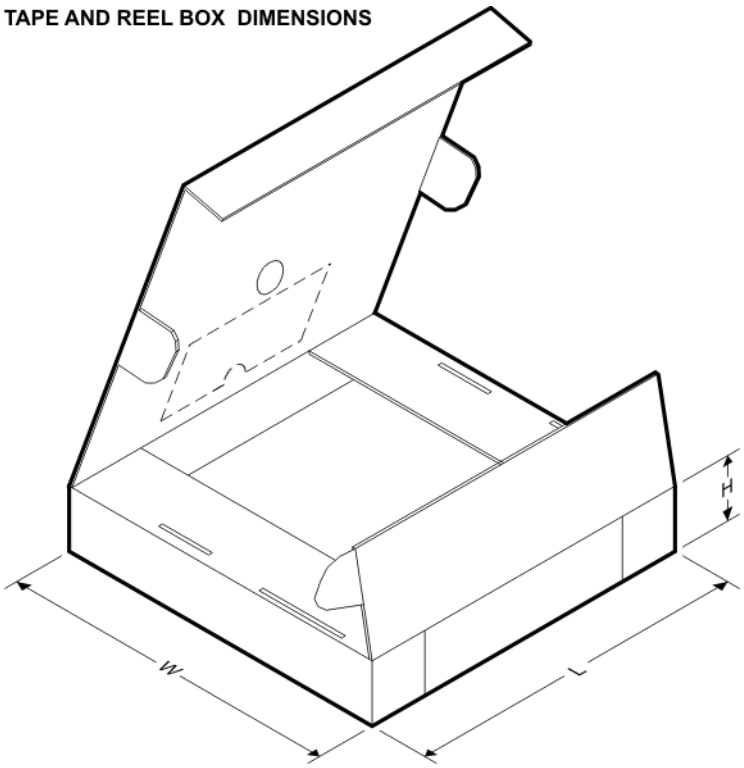
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS92LV090ATVEHX/NOPB	LQFP	PM	64	1000	330.0	24.4	12.35	12.35	2.2	16.0	24.0	Q2

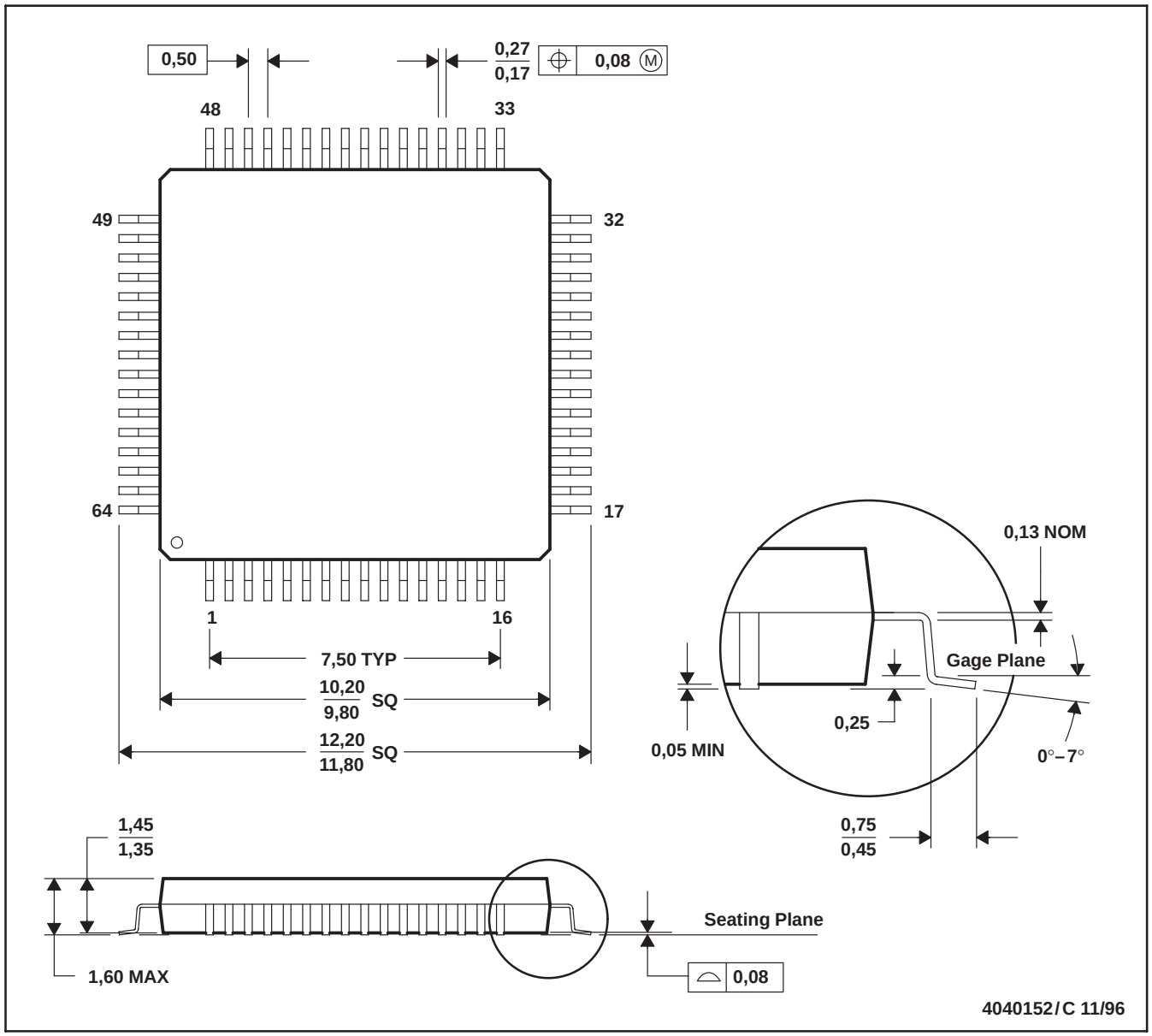
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS92LV090ATVEHX/NOPB	LQFP	PM	64	1000	367.0	367.0	45.0

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265