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**DS90CR213, DS90CR214**

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## DS90CR213/DS90CR214 21-Bit Channel Link—66 MHz

Check for Samples: DS90CR213, DS90CR214

# FEATURES

- **66 MHz Clock Support**
- **Up to 173 Mbytes/s Bandwidth**
- **Low Power CMOS Design (<610 mW)**
- **Power-down Mode (<0.5 mW total)**
- **Up to 1.386 Gbit/s Data Throughput**

- **Narrow Bus Reduces Cable Size and Cost**
- **290 mV Swing LVDS Devices for Low EMI**
- **PLL Requires No External Components**
- **Low Profile 48-Lead TSSOP Package**
- **Rising Edge Data Strobe**
- **Compatible with TIA/EIA-644 LVDS Standard**

# DESCRIPTION

The DS90CR213 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CR214 receiver converts the LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 66 MHz, 21 bits of TTL data are transmitted at a rate of 462 Mbps per LVDS data channel. Using a 66 MHz clock, the data throughput is 1.386 Gbit/s (173 Mbytes/s).

The multiplexing of the data lines provides a substantial cable reduction. Long distance parallel single-ended buses typically require a ground wire per active signal (and have very limited noise rejection capability). Thus, for a 21-bit wide data and one clock, up to 44 conductors are required. With the Channel Link chipset as few as 9 conductors (3 data pairs, 1 clock pair and a minimum of one ground) are needed. This provides an 80% reduction in required cable width, which provides a system cost savings, reduces connector physical size and cost, and reduces shielding requirements due to the cable's smaller form factor.

The 21 CMOS/TTL inputs can support a variety of signal combinations. For example, 5 4-bit nibbles (byte + parity) or 2 9-bit (byte + 3 parity) and 1 control.

# BLOCK DIAGRAM
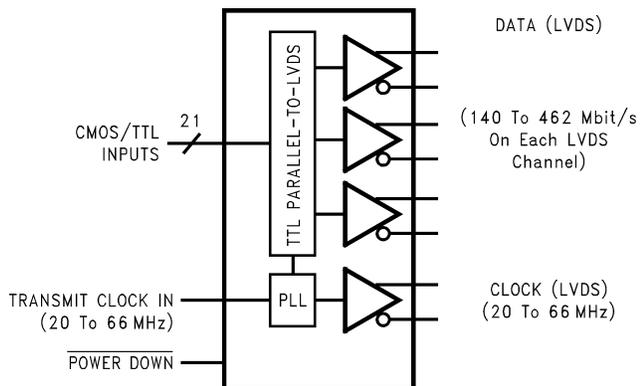


**Figure 1. DS90CR213**
**See Package Number DGG0048A**
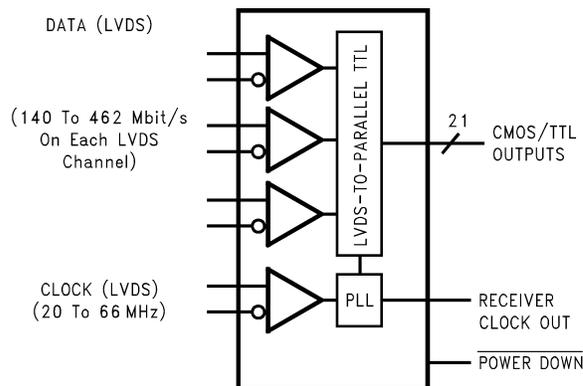


**Figure 2. DS90CR214**
**See NS Package Number DGG0048A**

## Connection Diagrams

OBSOLETE

# DS90CR213, DS90CR214

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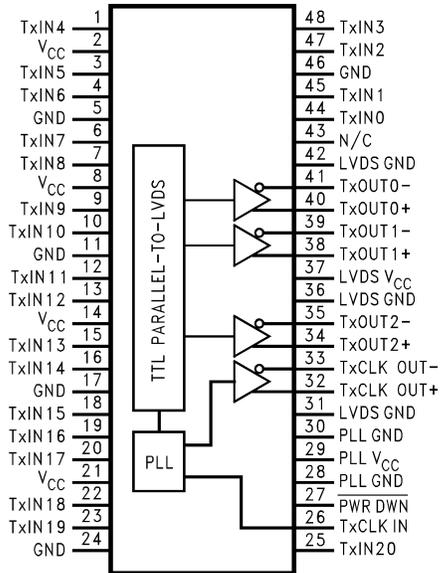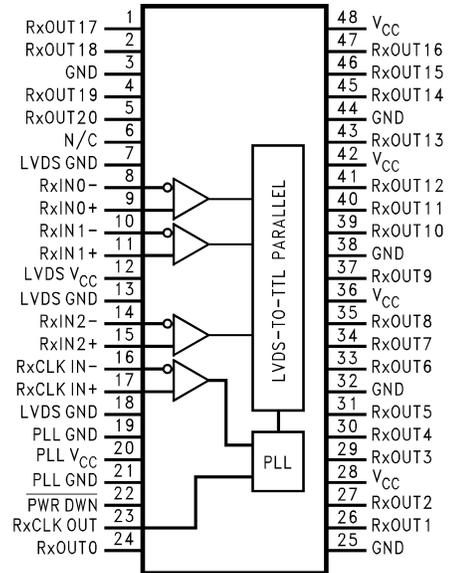
**Figure 3. DS90CR213**



**Figure 4. DS90CR214**

## Typical Application
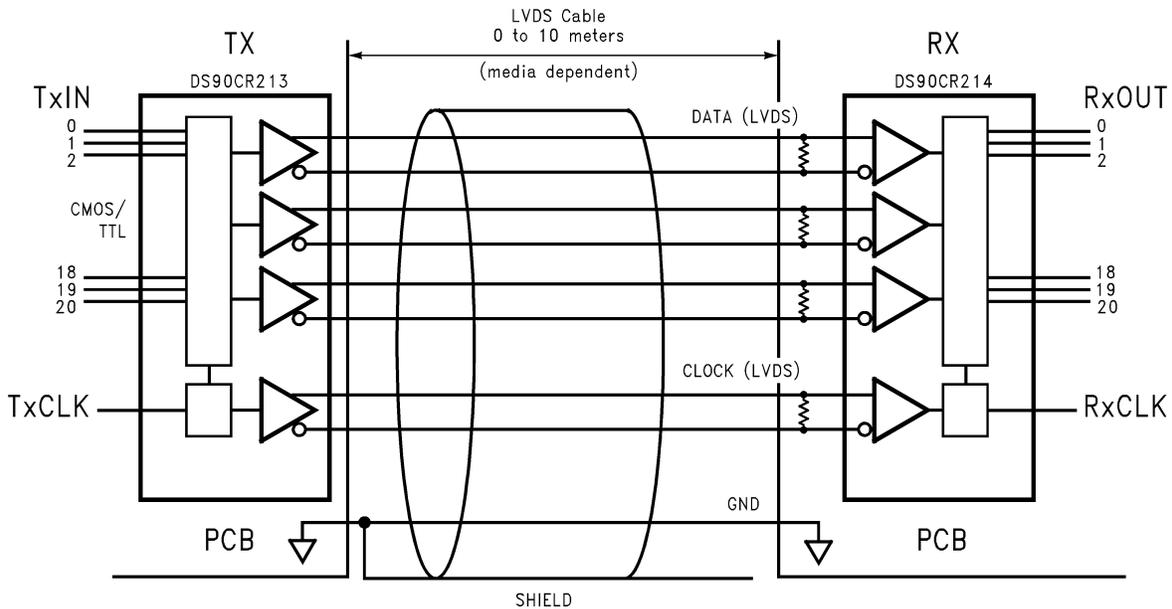


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Product Folder Links: *DS90CR213  DS90CR214*

## Absolute Maximum Ratings[1][2]

| | | |
|---|---|---|
| Supply Voltage ($V_{CC}$) | | −0.3V to +6V |
| CMOS/TTL Input Voltage | | −0.3V to ($V_{CC}$ + 0.3V) |
| CMOS/TTL Output Voltage | | −0.3V to ($V_{CC}$ + 0.3V) |
| LVDS Receiver Input Voltage | | −0.3V to ($V_{CC}$ + 0.3V) |
| LVDS Driver Output Voltage | | −0.3V to ($V_{CC}$ + 0.3V) |
| LVDS Output Short Circuit    Duration | | Continuous |
| Junction Temperature | | +150°C |
| Storage Temperature | | −65°C to +150°C |
| Lead Temperature (Soldering, 4 sec) | | +260°C |
| Maximum Package Power Dissipation Capacity | | @25°C |
| DGG0048A (TSSOP) Package | DS90CR213 | 1.98W |
| | DS90CR214 | 1.89W |
| Package Derating: | DS90CR213 | 16 mW/°C above +25°C |
| | DS90CR214 | 15 mW/°C above +25°C |
| ESD Rating[3]This device does not meet 2000V | | |

(1)   Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(2)   "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. "Electrical Characteristics" specify conditions for device operation.
(3)   ESD Rating: HBM (1.5 kΩ, 100 pF)   PLL $V_{CC}$ ≥ 1000V   All Other Pins ≥ 2000V   EIAJ (0Ω, 200 pF) ≥ 150V

## Recommended Operating Conditions

| | Min | Nom | Max | Units |
|---|---|---|---|---|
| Supply Voltage ($V_{CC}$) | 4.75 | 5.0 | 5.25 | V |
| Operating Free Air Temperature ($T_A$) | −10 | +25 | +70 | °C |
| Receiver Input Range | 0 | | 2.4 | V |
| Supply Noise Voltage ($V_{CC}$) | | | 100 | $mV_{P-P}$ |

## Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CMOS/TTL DC SPECIFICATIONS** | | | | | | |
| $V_{IH}$ | High Level Input Voltage | | 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Low Level Input Voltage | | GND | | 0.8 | V |
| $V_{OH}$ | High Level Output Voltage | $I_{OH}$ = −0.4 mA | 3.8 | 4.9 | | V |
| $V_{OL}$ | Low Level Output Voltage | $I_{OL}$ = 2 mA | | 0.1 | 0.3 | V |
| $V_{CL}$ | Input Clamp Voltage | $I_{CL}$ = −18 mA | | −0.79 | −1.5 | V |
| $I_{IN}$ | Input Current | $V_{IN}$ = $V_{CC}$, GND, 2.5V or 0.4V | | ±5.1 | ±10 | µA |
| $I_{OS}$ | Output Short Circuit Current | $V_{OUT}$ = 0V | | | −120 | mA |
| **LVDS DRIVER DC SPECIFICATIONS** | | | | | | |
| $V_{OD}$ | Differential Output Voltage | $R_L$ = 100Ω | 250 | 290 | 450 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ between Complimentary Output States | | | | 35 | mV |
| $V_{OS}$ | Offset Voltage | | 1.1 | 1.25 | 1.375 | V |
| $\Delta V_{OS}$ | Change in Magnitude of $V_{OS}$ between Complimentary Output States | | | | 35 | mV |
| $I_{OS}$ | Output Short Circuit Current | $V_{OUT}$ = 0V, $R_L$ = 100Ω | | −2.9 | −5 | mA |
| $I_{OZ}$ | Output TRI-STATE® Current | $\overline{Powerdown}$ = 0V, $V_{OUT}$ = 0V or $V_{CC}$ | | ±1 | ±10 | µA |
| **LVDS RECEIVER DC SPECIFICATIONS** | | | | | | |

## Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{TH}$ | Differential Input High Threshold | $V_{CM}$ = +1.2V | | | | +100 | mV |
| $V_{TL}$ | Differential Input Low Threshold | | | −100 | | | mV |
| $I_{IN}$ | Input Current | $V_{IN}$ = +2.4V, $V_{CC}$ = 5.0V | | | | ±10 | µA |
| | | $V_{IN}$ = 0V, $V_{CC}$ = 5.0V | | | | ±10 | µA |
| **TRANSMITTER SUPPLY CURRENT** | | | | | | | |
| $I_{CCTW}$ | Transmitter Supply Current | $R_L$ = 100Ω, $C_L$ = 5 pF, | f = 32.5 MHz | | 49 | 63 | mA |
| | Worst Case | Worst Case Pattern | f = 37.5 MHz | | 51 | 64 | mA |
| | | (Figure 5 and Figure 6 ) | f = 66 MHz | | 70 | 84 | mA |
| $I_{CCTZ}$ | Transmitter Supply Current | $\overline{Powerdown}$ = Low | | | | | |
| | Power Down | Driver Outputs in TRI-STATE under Powerdown Mode | | | 1 | 25 | µA |
| **RECEIVER SUPPLY CURRENT** | | | | | | | |
| $I_{CCRW}$ | Receiver Supply Current | $C_L$ = 8 pF, | f = 32.5 MHz | | 64 | 77 | mA |
| | Worst Case | Worst Case Pattern | f = 37.5 MHz | | 70 | 85 | mA |
| | | (Figure 5 and Figure 7 ) | f = 66 MHz | | 110 | 140 | mA |
| $I_{CCRZ}$ | Receiver Supply Current | $\overline{Powerdown}$ = Low | | | | | |
| | Power Down | Receiver Outputs in Previous State during Power Down Mode. | | | 1 | 10 | µA |

## Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| LLHT | LVDS Low-to-High Transition Time (Figure 6 ) | | | 0.75 | 1.5 | ns |
| LHLT | LVDS High-to-Low Transition Time (Figure 6 ) | | | 0.75 | 1.5 | ns |
| TCIT | TxCLK IN Transition Time (Figure 8 ) | | | | 8 | ns |
| TCCS | TxOUT Channel-to-Channel Skew [1] (Figure 9) | | | | 350 | ps |
| TPPos0 | Transmitter Output Pulse Position for Bit 0 (Figure 20 ) | | −0.30 | 0 | 0.30 | ns |
| TPPos1 | Transmitter Output Pulse Position for Bit 1 | | 1.70 | (1/7)Tclk | 2.50 | ns |
| TPPos2 | Transmitter Output Pulse Position for Bit 2 | | 3.60 | (2/7)Tclk | 4.50 | ns |
| TPPos3 | Transmitter Output Pulse Position for Bit 3 | f = 66 MHz | 5.90 | (3/7)Tclk | 6.75 | ns |
| TPPos4 | Transmitter Output Pulse Position for Bit 4 | | 8.30 | (4/7)Tclk | 9.00 | ns |
| TPPos5 | Transmitter Output Pulse Position for Bit 5 | | 10.40 | (5/7)Tclk | 11.10 | ns |
| TPPos6 | Transmitter Output Pulse Position for Bit 6 | | 12.70 | (6/7)Tclk | 13.40 | ns |
| TCIP | TxCLK IN Period (Figure 10 ) | | 15 | T | 50 | ns |
| TCIH | TxCLK IN High Time (Figure 10 ) | | 0.35T | 0.5T | 0.65T | ns |
| TCIL | TxCLK IN Low Time (Figure 10 ) | | 0.35T | 0.5T | 0.65T | ns |
| TSTC | TxIN Setup to TxCLK IN (Figure 10 ) | | 5 | 3.5 | | ns |
| THTC | TxIN Hold to TxCLK IN (Figure 10 ) | | 2.5 | 1.5 | | ns |
| TCCD | TxCLK IN to TxCLK OUT Delay @25°C, $V_{CC}$ = 5.0V (Figure 12 ) | | 3.5 | | 8.5 | ns |
| TPLLS | Transmitter Phase Lock Loop Set (Figure 14 ) | | | | 10 | ms |
| TPDD | Transmitter Powerdown Delay (Figure 18 ) | | | | 100 | ns |

(1)  This limit based on bench characterization.

## Receiver Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| CLHT | CMOS/TTL Low-to-High Transition Time (Figure 7 ) | | | 2.5 | 4.0 | ns |
| CHLT | CMOS/TTL High-to-Low Transition Time (Figure 7 ) | | | 2.0 | 4.0 | ns |
| RSKM | RxIN Skew Margin [1] V $_{CC}$ = 5V,T$_A$ = 25°C(Figure 21) | f = 40 MHz | 700 | | | ps |
| | | f = 66 MHz | 600 | | | ps |
| RCOP | RxCLK OUT Period (Figure 11 ) | | 15 | T | 50 | ns |
| RCOH | RxCLK OUT High Time (Figure 11 ) | f = 40 MHz | 6 | | | ns |
| | | f = 66 MHz | 4.3 | 5 | | ns |
| RCOL | RxCLK OUT Low Time (Figure 11 ) | f = 40 MHz | 10.5 | | | ns |
| | | f = 66 MHz | 7.0 | 9 | | ns |
| RSRC | RxOUT Setup to RxCLK OUT (Figure 11 ) | f = 40 MHz | 4.5 | | | ns |
| | | f = 66 MHz | 2.5 | 4.2 | | ns |
| RHRC | RxOUT Hold to RxCLK OUT (Figure 11 ) | f = 40 MHz | 6.5 | | | ns |
| | | f = 66 MHz | 4 | 5.2 | | ns |
| RCCD | RxCLK IN to RxCLK OUT Delay @25°C, V$_{CC}$ = 5.0V (Figure 13 ) | | 6.4 | | 10.7 | ns |
| RPLLS | Receiver Phase Lock Loop Set (Figure 15 ) | | | | 10 | ms |
| RPDD | Receiver Powerdown Delay (Figure 19 ) | | | | 1 | µs |

(1) Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account for transmitter output skew (TCCS) and the setup and hold time (internal data sampling window), allowing LVDS cable skew dependent on type/length and source clock (TxCLK IN) jitter.RSKM ≥ cable skew (type, length) + source clock jitter (cycle to cycle)

## AC Timing Diagrams
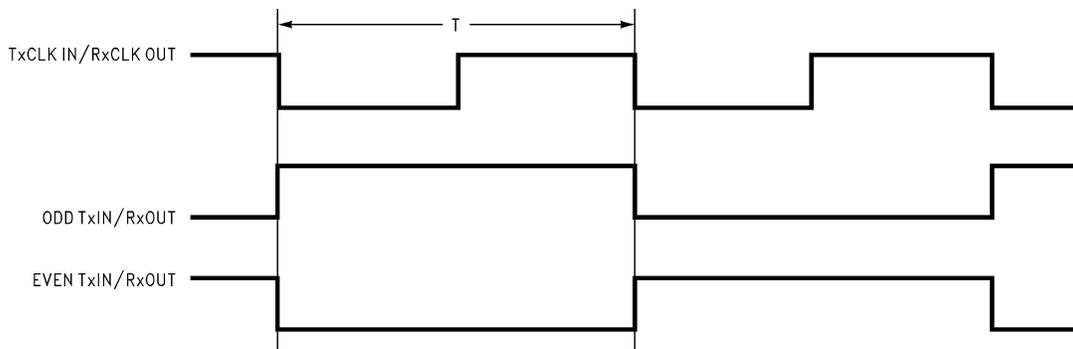


Figure 5.  "Worst Case" Test Pattern
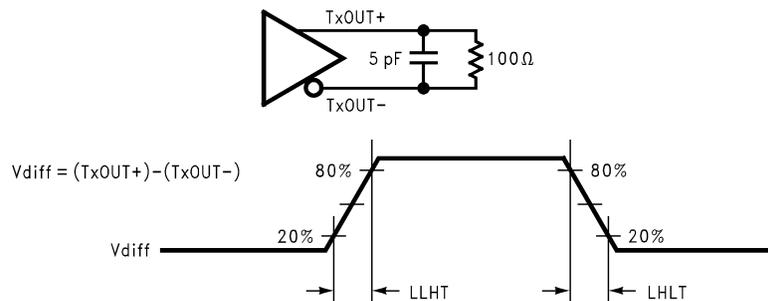


Figure 6.  DS90CR213 (Transmitter) Input Clock Transition Time
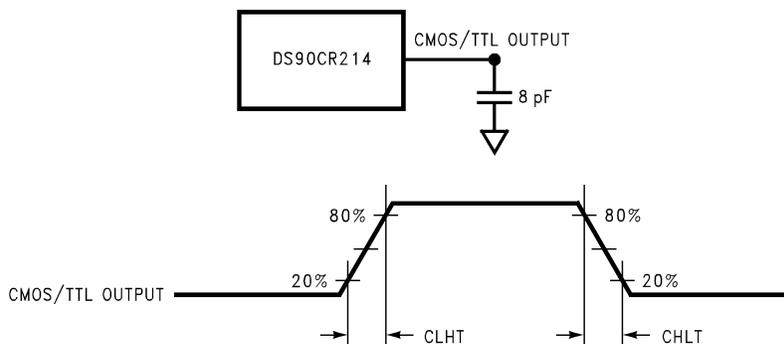
**Figure 7. DS90CR214 (Receiver) CMOS/TTL Output Load and Transition Times**
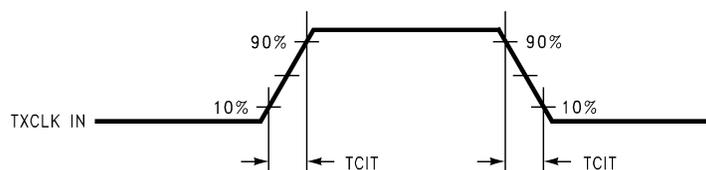


**Figure 8. DS90CR213 (Transmitter) Input Clock Transition Time**
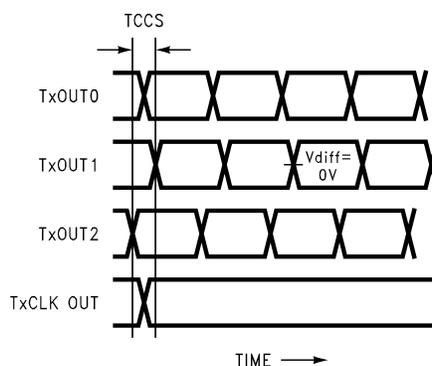


(1)   Measurements at $V_{diff}$ = 0V

(2)   TCSS measured between earliest and latest LVDS edges.

(3)   TxCLK Differential Low→High Edge

**Figure 9. DS90CR213 (Transmitter) Channel-to-Channel Skew**
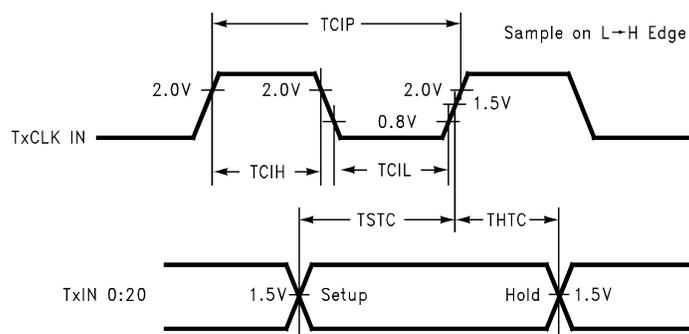


**Figure 10. DS90CR213 (Transmitter) Setup/Hold and High/Low Times**

Product Folder Links: *DS90CR213  DS90CR214*
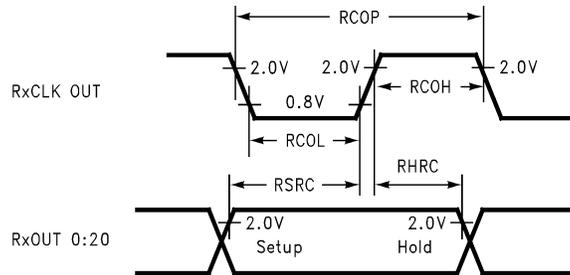
**Figure 11.  DS90CR214 (Receiver) Setup/Hold and High/Low Times**
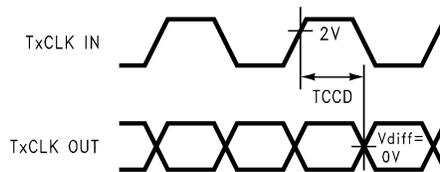


**Figure 12.  DS90CR213 (Transmitter) Clock In to Clock Out Delay**
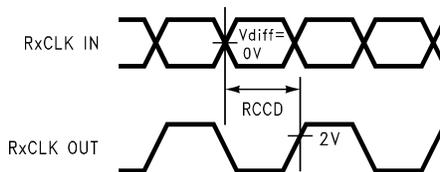


**Figure 13.  DS90CR214 (Receiver) Clock In to Clock Out Delay**
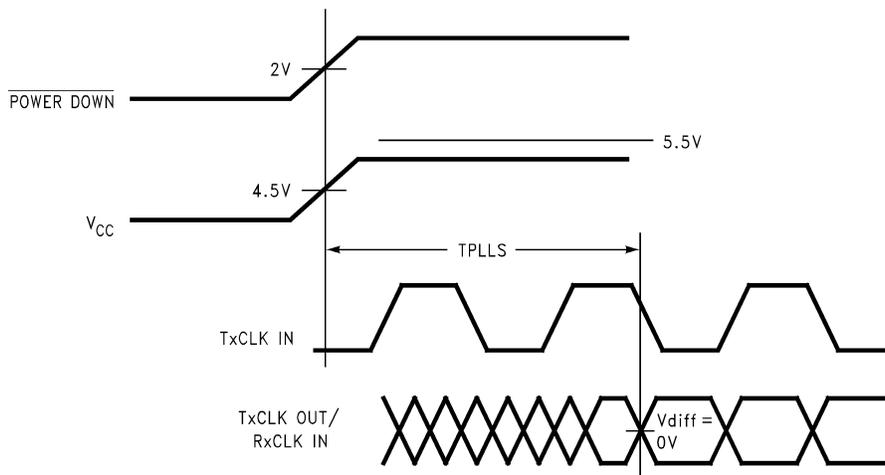


**Figure 14.  DS90CR213 (Transmitter) Phase Lock Loop Set Time**
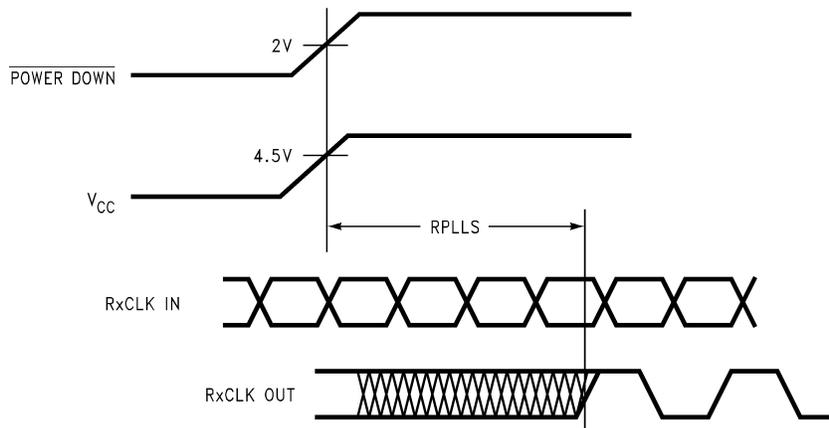
**Figure 15. DS90CR214 (Receiver) Phase Lock Loop Set Time**
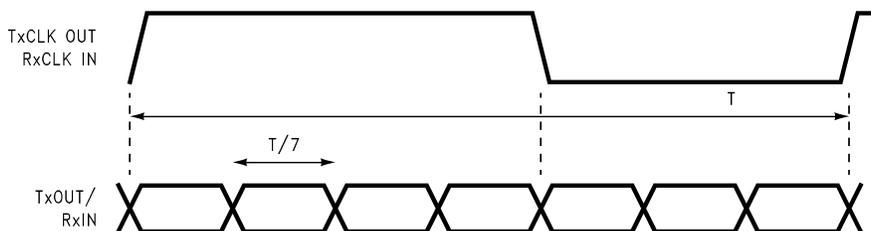


**Figure 16. Seven Bits of LVDS in Once Clock Cycle**
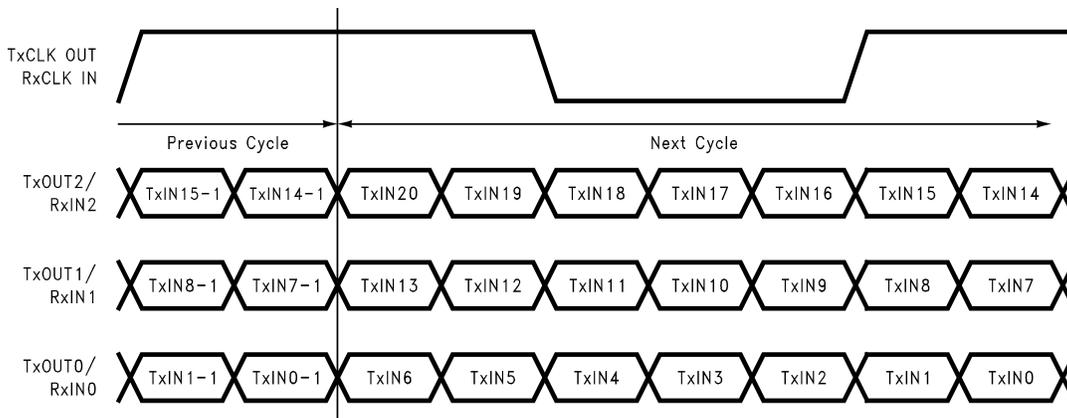


**Figure 17. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs**
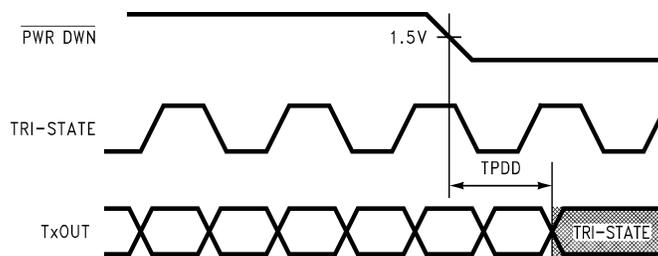


**Figure 18. Transmitter Powerdown Delay**

Product Folder Links: *DS90CR213  DS90CR214*
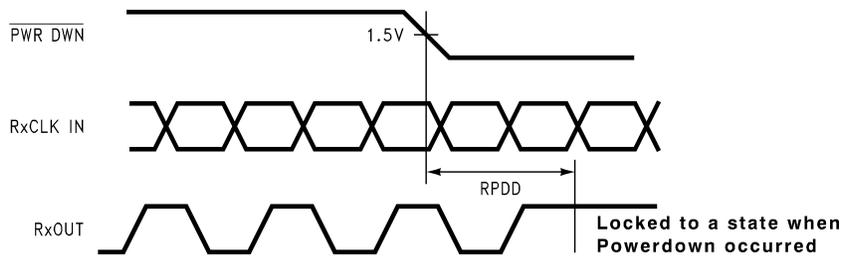
**Figure 19. Receiver Powerdown Delay**
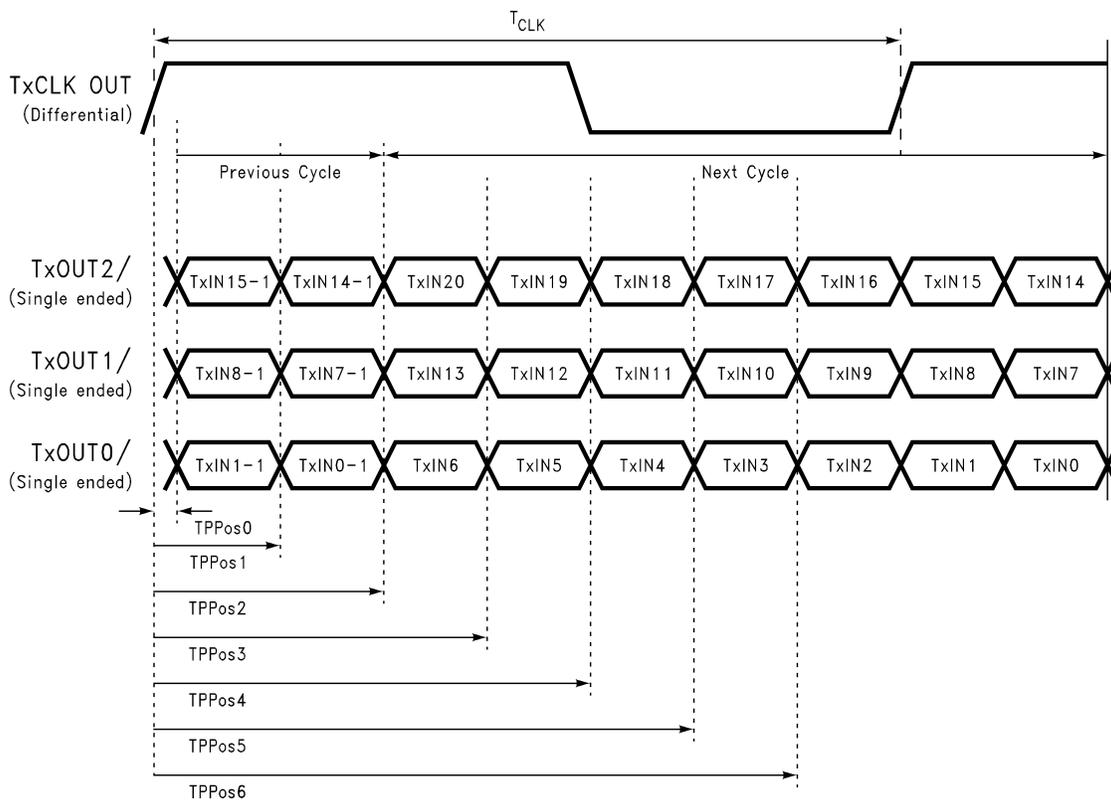


**Figure 20. Transmitter LVDS Output Pulse Position Measurement**
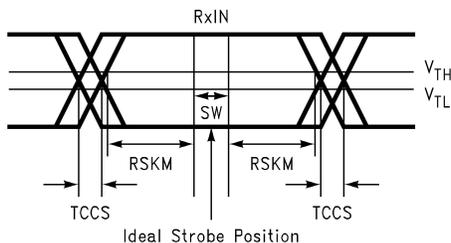


SW—Setup and Hold Time (Internal Data Sampling Window)
TCCS—Transmitter Output Skew
RSKM ≥ Cable Skew (Type, Length) + Source Clock Jitter (Cycle to Cycle)
Cable Skew—Typically 10 ps–40 ps per foot

**Figure 21. Receiver LVDS Input Skew Margin**

**DS90CR213, DS90CR214**

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### DS90CR213 Pin Description—Channel Link Transmitter

| Pin Name | I/O | No. | Description |
|---|---|---|---|
| TxIN | I | 21 | TTL level inputs. |
| TxOUT+ | O | 3 | Positive LVDS differential data output. |
| TxOUT− | O | 3 | Negative LVDS differential data output. |
| TxCLK IN | I | 1 | TTL level clock input. The rising edge acts as data strobe. |
| TxCLK OUT+ | O | 1 | Positive LVDS differential clock output. |
| TxCLK OUT− | O | 1 | Negative LVDS differential clock output. |
| $\overline{\text{PWR DOWN}}$ | I | 1 | TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down. |
| $V_{CC}$ | I | 4 | Power supply pins for TTL inputs. |
| GND | I | 5 | Ground pins for TTL inputs. |
| PLL $V_{CC}$ | I | 1 | Power supply pin for PLL. |
| PLL GND | I | 2 | Ground pins for PLL. |
| LVDS $V_{CC}$ | I | 1 | Power supply pin for LVDS outputs. |
| LVDS GND | I | 3 | Ground pins for LVDS outputs. |

### DS90CR214 Pin Description—Channel Link Receiver

| Pin Name | I/O | No. | Description |
|---|---|---|---|
| RxIN+ | I | 3 | Positive LVDS differential data inputs. |
| RxIN− | I | 3 | Negative LVDS differential data inputs. |
| RxOUT | O | 21 | TTL level outputs. |
| RxCLK IN+ | I | 1 | Positive LVDS differential clock input. |
| RxCLK IN− | I | 1 | Negative LVDS differential clock input. |
| RxCLK OUT | O | 1 | TTL level clock output. The rising edge acts as data strobe. |
| $\overline{\text{PWR DOWN}}$ | I | 1 | TTL level input. Locks the previous receiver output state. |
| $V_{CC}$ | I | 4 | Power supply pins for TTL outputs. |
| GND | I | 5 | Ground pins for TTL outputs. |
| PLL $V_{CC}$ | I | 1 | Power supply for PLL. |
| PLL GND | I | 2 | Ground pin for PLL. |
| LVDS $V_{CC}$ | I | 1 | Power supply pin for LVDS inputs. |
| LVDS GND | I | 3 | Ground pins for LVDS inputs. |

Product Folder Links: *DS90CR213  DS90CR214*

## APPLICATIONS INFORMATION

The Channel Link devices are intended to be used in a wide variety of data transmission applications. Depending upon the application the interconnecting media may vary. For example, for lower data rate (clock rate) and shorter cable lengths (< 2m), the media electrical performance is less critical. For higher speed/long distance applications the media's performance becomes more critical. Certain cable constructions provide tighter skew (matched electrical length between the conductors and pairs). Twin-coax for example, has been demonstrated at distances as great as 5 meters and with the maximum data transfer of 1.38 Gbit/s. Additional applications information can be found in the following National Interface Application Notes:

| AN = #### | Topic |
|---|---|
| AN-1041 | Introduction to Channel Link |
| AN-1035 | PCB Design Guidelines for LVDS and Link Devices |
| AN-806 | Transmission Line Theory |
| AN-905 | Transmission Line Calculations and Differential Impedance |
| AN-916 | Cable Information |

## CABLES

A cable interface between the transmitter and receiver needs to support the differential LVDS pairs. The 21-bit CHANNEL LINK chipset (DS90CR213/214) requires four pairs of signal wires and the 28-bit CHANNEL LINK chipset (DS90CR283/284) requires five pairs of signal wires. The ideal cable/connector interface would have a constant 100Ω differential impedance throughout the path. It is also recommended that cable skew remain below 350 ps (@ 66 MHz clock rate) to maintain a sufficient data sampling window at the receiver.

In addition to the four or five cable pairs that carry data and clock, it is recommended to provide at least one additional conductor (or pair) which connects ground between the transmitter and receiver. This low impedance ground provides a common mode return path for the two devices. Some of the more commonly used cable types for point-to-point applications include flat ribbon, flex, twisted pair and Twin-Coax. All are available in a variety of configurations and options. Flat ribbon cable, flex and twisted pair generally perform well in short point-to-point applications while Twin-Coax is good for short and long applications. When using ribbon cable, it is recommended to place a ground line between each differential pair to act as a barrier to noise coupling between adjacent pairs. For Twin-Coax cable applications, it is recommended to utilize a shield on each cable pair. All extended point-to-point applications should also employ an overall shield surrounding all cable pairs regardless of the cable type. This overall shield results in improved transmission parameters such as faster attainable speeds, longer distances between transmitter and receiver and reduced problems associated with EMS or EMI.

The high-speed transport of LVDS signals has been demonstrated on several types of cables with excellent results. However, the best overall performance has been seen when using Twin-Coax cable. Twin-Coax has very low cable skew and EMI due to its construction and double shielding. All of the design considerations discussed here and listed in the supplemental application notes provide the subsystem communications designer with many useful guidelines. It is recommended that the designer assess the tradeoffs of each application thoroughly to arrive at a reliable and economical cable solution.

## BOARD LAYOUT

To obtain the maximum benefit from the noise and EMI reductions of LVDS, attention should be paid to the layout of differential lines. Lines of a differential pair should always be adjacent to eliminate noise interference from other signals and take full advantage of the noise canceling of the differential signals. The board designer should also try to maintain equal length on signal traces for a given differential pair. As with any high speed design, the impedance discontinuities should be limited (reduce the numbers of vias and no 90 degree angles on traces). Any discontinuities which do occur on one signal line should be mirrored in the other line of the differential pair. Care should be taken to ensure that the differential trace impedance match the differential impedance of the selected physical media (this impedance should also match the value of the termination resistor that is connected across the differential pair at the receiver's input). Finally, the location of the CHANNEL LINK TxOUT/RxIN pins should be as close as possible to the board edge so as to eliminate excessive pcb runs. All of these considerations will limit reflections and crosstalk which adversely effect high frequency performance and EMI.

## UNUSED INPUTS

All unused inputs at the TxIN inputs of the transmitter must be tied to ground. All unused outputs at the RxOUT outputs of the receiver must then be left floating.

## TERMINATION

Use of current mode drivers requires a terminating resistor across the receiver inputs. The CHANNEL LINK chipset will normally require a single 100Ω resistor between the true and complement lines on each differential pair of the receiver input. The actual value of the termination resistor should be selected to match the differential mode characteristic impedance (90Ω to 120Ω typical) of the cable. Figure 22 shows an example. No additional pull-up or pull-down resistors are necessary as with some other differential technologies such as PECL. Surface mount resistors are recommended to avoid the additional inductance that accompanies leaded resistors. These resistors should be placed as close as possible to the receiver input pins to reduce stubs and effectively terminate the differential lines.

## DECOUPLING CAPACITORS

Bypassing capacitors are needed to reduce the impact of switching noise which could limit performance. For a conservative approach three parallel-connected decoupling capacitors (Multi-Layered Ceramic type in surface mount form factor) between each $V_{CC}$ and the ground plane(s) are recommended. The three capacitor values are 0.1 µF, 0.01µF and 0.001 µF. An example is shown in Figure 23. The designer should employ wide traces for power and ground and ensure each capacitor has its own via to the ground plane. If board space is limiting the number of bypass capacitors, the PLL $V_{CC}$ should receive the most filtering/bypassing. Next would be the LVDS $V_{CC}$ pins and finally the logic $V_{CC}$ pins.
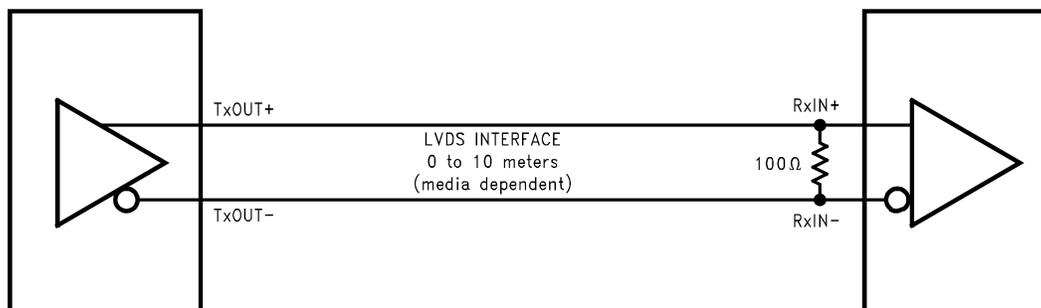


**Figure 22. LVDS Serialized Link Termination**
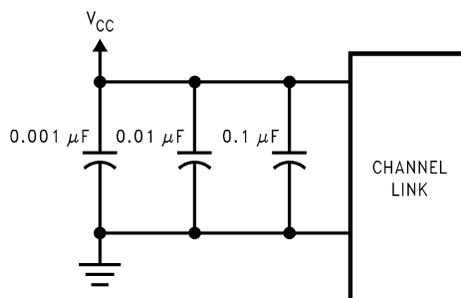


**Figure 23. CHANNEL LINK
Decoupling Configuration**

Product Folder Links: *DS90CR213  DS90CR214*

## CLOCK JITTER

The CHANNEL LINK devices employ a PLL to generate and recover the clock transmitted across the LVDS interface. The width of each bit in the serialized LVDS data stream is one-seventh the clock period. For example, a 66 MHz clock has a period of 15 ns which results in a data bit width of 2.16 ns. Differential skew (Δt within one differential pair), interconnect skew (Δt of one differential pair to another) and clock jitter will all reduce the available window for sampling the LVDS serial data streams. Care must be taken to ensure that the clock input to the transmitter be a clean low noise signal. Individual bypassing of each $V_{CC}$ to ground will minimize the noise passed on to the PLL, thus creating a low jitter LVDS clock. These measures provide more margin for channel-to-channel skew and interconnect skew as a part of the overall jitter/skew budget.

## COMMON MODE vs. DIFFERENTIAL MODE NOISE MARGIN

The typical signal swing for LVDS is 300 mV centered at +1.2V. The CHANNEL LINK receiver supports a 100 mV threshold therefore providing approximately 200 mV of differential noise margin. Common mode protection is of more importance to the system's operation due to the differential data transmission. LVDS supports an input voltage range of Ground to +2.4V. This allows for a ±1.0V shifting of the center point due to ground potential differences and common mode noise.

## POWER SEQUENCING AND POWERDOWN MODE

Outputs of the CHANNEL LINK transmitter remain in TRI-STATE until the power supply reaches 3V. Clock and data outputs will begin to toggle 10 ms after $V_{CC}$ has reached 4.5V and the Powerdown pin is above 2V. Either device may be placed into a powerdown mode at any time by asserting the Powerdown pin (active low). Total power dissipation for each device will decrease to 5 µW (typical).

The CHANNEL LINK chipset is designed to protect itself from accidental loss of power to either the transmitter or receiver. If power to the transmit board is lost, the receiver clocks (input and output) stop. The data outputs (RxOUT) retain the states they were in when the clocks stopped. When the receiver board loses power, the receiver inputs are shorted to $V_{CC}$ through an internal diode. Current is limited (5 mA per input) by the fixed current mode drivers, thus avoiding the potential for latchup when powering the device.
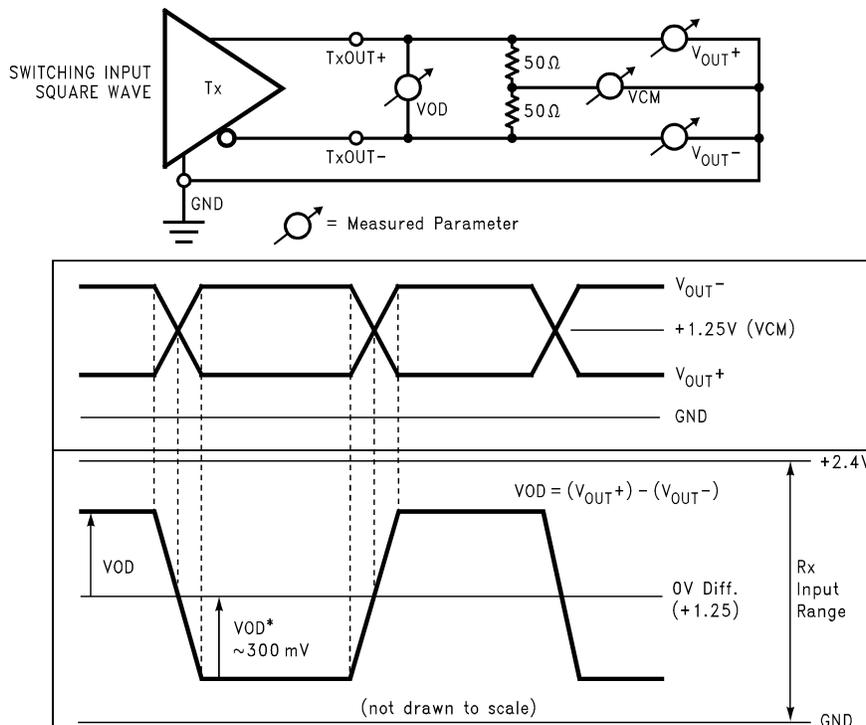


**Figure 24. Single-Ended and Differential Waveforms**

# IMPORTANT NOTICE

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