National Semiconductor

DS75154 Quad Line Receiver

General Description

The DS75154 is a quad monolithic line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. Other applications are in relatively short, single-line, point-to-point data transmission systems and for level translators. Operation is normally from a single 5V supply; however, a built-in option allows operation from a 12V supply without the use of additional components. The output is compatible with most TTL and LS circuits when either supply voltage is used.

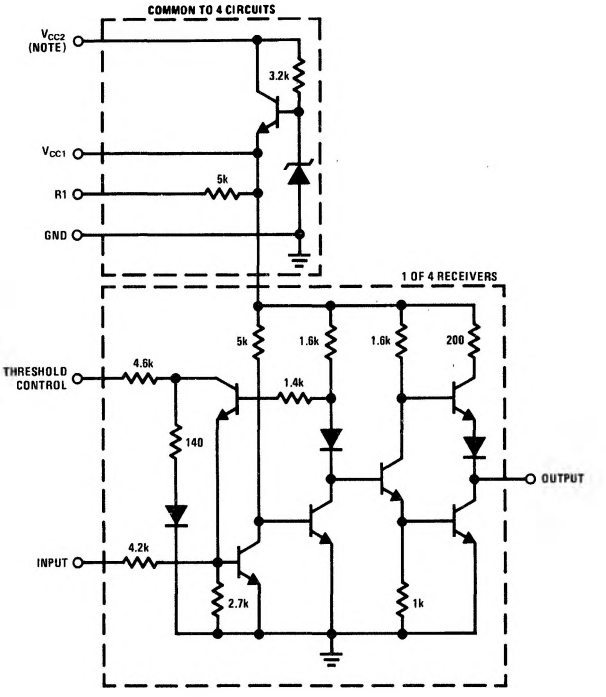
In normal operation, the threshold-control terminals are connected to the V_{CC1} terminal, pin 15, even if power is being supplied via the alternate V_{CC2} terminal, pin 16. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold voltages. In this mode, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

Features

- Input resistance, 3 kΩ to 7 kΩ over full RS-232C voltage range
- Input threshold adjustable to meet "fail-safe" requirements without using external components
- Inverting output compatible with TTL or LS
- Built-in hysteresis for increased noise immunity
- Output with active pull-up for symmetrical switching speeds
- Standard supply voltage—5V or 12V

Schematic Diagram



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Note: When using V_{CC1} (pin 15), V_{CC2} (pin 16) may be left open or shorted to V_{CC1}. When using V_{CC2}, V_{CC1} must be left open or connected to the threshold control pins.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Normal Supply Voltage (Pin 15), (V_{CC1})	7V
Alternate Supply Voltage (Pin 16), (V_{CC2})	14V
Input Voltage	±25V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded DIP Package	1362 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate molded DIP package 10.9 mW/°C above 25°C; derate SO package 8.01 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (Pin 15), (V_{CC1})	4.5	5.5	V
Alternate Supply Voltage (Pin 16), (V_{CC2})	10.8	13.2	V
Input Voltage		±15	V
Temperature, (T_A)	0	+70	°C

Electrical Characteristics (Notes 2, 3 and 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	*(Figure 1)*		3			V
V_{IL}	Low-Level Input Voltage	*(Figure 1)*				−3	V
V_{T+}	Positive-Going Threshold Voltage	*(Figure 1)*	Normal Operation	0.8	2.2	3	V
			Fail-Safe Operation	0.8	2.2	3	V
V_{T-}	Negative-Going Threshold Voltage	*(Figure 1)*	Normal Operation	−3	−1.1	0	V
			Fail-Safe Operation	0.8	1.4	3	V
$V_{T+}-V_{T-}$	Hysteresis	*(Figure 1)*	Normal Operation	0.8	3.3	6	V
			Fail-Safe Operation	0	0.8	2.2	V
V_{OH}	High-Level Output Voltage	$I_{OH}=-400\ \mu A$, *(Figure 1)*		2.4	3.5		V
V_{OL}	Low-Level Output Voltage	$I_{OL}=16$ mA, *(Figure 1)*			0.23	0.4	V
r_I	Input Resistance	*(Figure 2)*	$\Delta V_I=-25V$ to $-14V$	3	5	7	kΩ
			$\Delta V_I=-14V$ to $-3V$	3	5	7	kΩ
			$\Delta V_I=-3V$ to $+3V$	3	6		kΩ
			$\Delta V_I=3V$ to 14V	3	5	7	kΩ
			$\Delta V_I=14V$ to 25V	3	5	7	kΩ
$V_{I(OPEN)}$	Open-Circuit Input Voltage	$I_I=0$, *(Figure 3)*		0	0.2	2	V
I_{OS}	Short-Circuit Output Current (Note 5)	$V_{CC1}=5.5V$, $V_I=-5V$, *(Figure 4)*		−10	−20	−40	mA
I_{CC1}	Supply Current From V_{CC1}	$V_{CC1}=5.5V$, $T_A=25°C$, *(Figure 5)*			20	35	mA
I_{CC2}	Supply Current From V_{CC2}	$V_{CC2}=13.2V$, $T_A=25°C$, *(Figure 5)*			23	40	mA

Switching Characteristics ($V_{CC1}=5V$, $T_A=25°C$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$C_L=50$ pF, $R_L=390\Omega$, *(Figure 6)*		22		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	$C_L=50$ pF, $R_L=390\Omega$, *(Figure 6)*		20		ns
t_{TLH}	Transition Time, Low-to-High Level Output	$C_L=50$ pF, $R_L=390\Omega$, *(Figure 6)*		9		ns
t_{THL}	Transition Time, High-to-Low Level Output	$C_L=50$ pF, $R_L=390\Omega$, *(Figure 6)*		6		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75154. All typical values are for $T_A=25°C$ and $V_{CC1}=5V$.

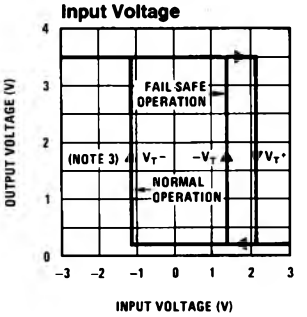
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic and threshold levels only, e.g., when −3V is the maximum, the minimum limit is a more-negative voltage.

Note 5: Only one output at a time should be shorted.

Typical Performance Characteristics

Output Voltage vs Input Voltage



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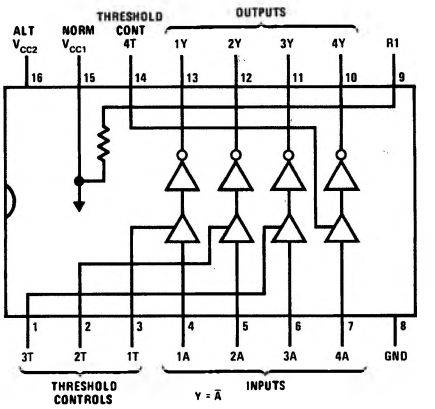
Connection Diagram

Dual-In-Line Package



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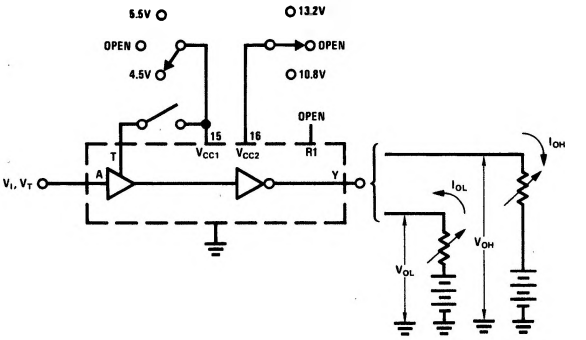
Top View

Order Number DS75154M or DS75154N
See NS Package Number M16A or N16A

DC Test Circuits and Truth Tables



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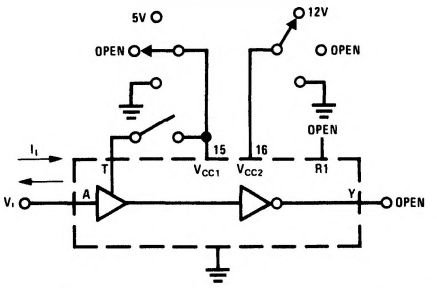
Test	Measure	A	T	Y	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open-Circuit Input (Fail-Safe)	V_{OH} V_{OH}	Open Open	Open Open	I_{OH} I_{OH}	4.5V Open	Open 10.8V
V_{T+} min, V_{T-} (Fail-Safe)	V_{OH} V_{OH}	0.8V 0.8V	Open Open	I_{OH} I_{OH}	5.5V Open	Open 13.2V
V_{T+} min (Normal)	V_{OH} V_{OH}	(Note 1) (Note 1)	Pin 15 Pin 15	I_{OH} I_{OH}	5.5V and T T	Open 13.2V
V_{IL} max, V_{T-} min (Normal)	V_{OH} V_{OH}	−3V −3V	Pin 15 Pin 15	I_{OH} I_{OH}	5.5V and T T	Open 13.2V
V_{IH} min, V_{T+} max, V_{T-} max (Fail-Safe)	V_{OL} V_{OL}	3V 3V	Open Open	I_{OL} I_{OL}	4.5V Open	Open 10.8V
V_{IH} min, V_{T+} max, (Normal)	V_{OL} V_{OL}	3V 3V	Pin 15 Pin 15	I_{OL} I_{OL}	4.5V and T T	Open 10.8V
V_{T-} max (Normal)	V_{OL} V_{OL}	(Note 2) (Note 2)	Pin 15 Pin 15	I_{OL} I_{OL}	5.5V and T T	Open 13.2V

Note 1: Momentarily apply −5V, then 0.8V.

Note 2: Momentarily apply 5V, then ground.

FIGURE 1. V_{IH}, V_{IL}, V_{T+}, V_{T-}, V_{OH}, V_{OL}

DC Test Circuits and Truth Tables (Continued)



$$r_I = \frac{\Delta V_I}{\Delta I_I}$$

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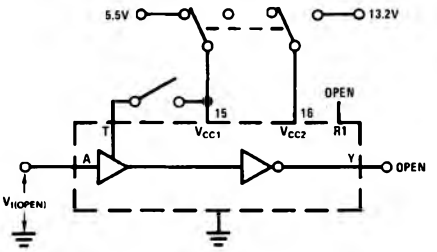
T	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open	5V	Open
Open	Gnd	Open
Open	Open	Open
Pin 15	T and 5V	Open
Gnd	Gnd	Open
Open	Open	12V
Open	Open	Gnd
Pin 15	T	12V
Pin 15	T	Gnd
Pin 15	T	Open

FIGURE 2. r_I



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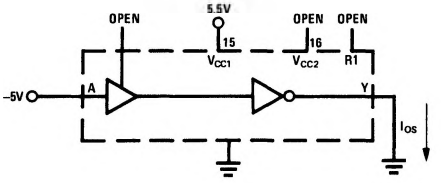
T	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open	5.5V	Open
Pin 15	5.5V	Open
Open	Open	13.2V
Pin 15	T	13.2V

FIGURE 3. $V_{I(OPEN)}$



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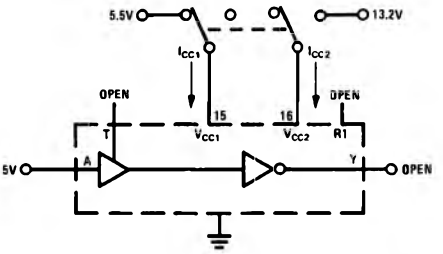
Each output is tested separately.

FIGURE 4. I_{OS}



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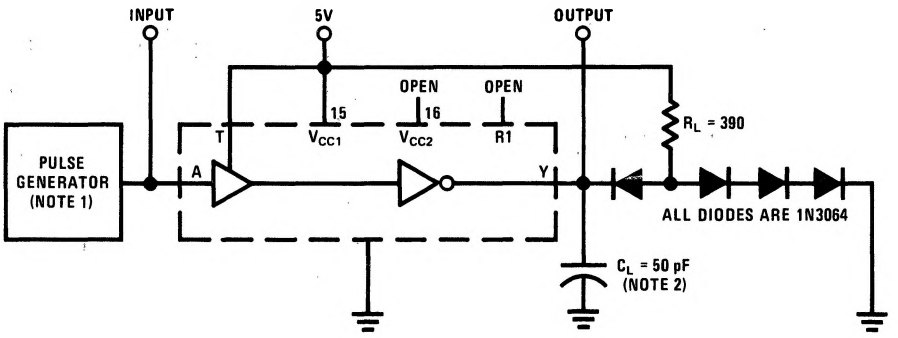
All four line receivers are tested simultaneously.

FIGURE 5. I_{CC}

AC Test Circuit and Switching Time Waveforms



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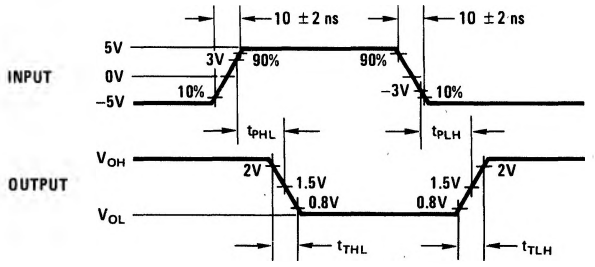

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Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$, $t_W = 200$ ns, duty cycle ≤ 20%.

Note 2: C_L includes probe and jig capacitance.

FIGURE 6