DS21354 (3.3V) and DS21554 (5V) E1 Single Chip Transceivers (SCT)

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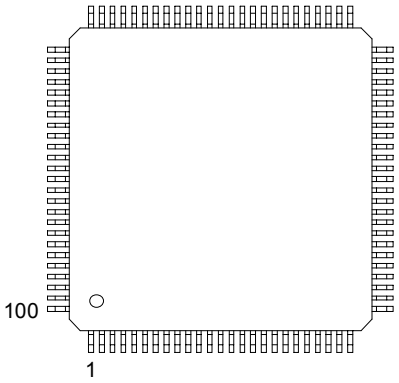
FEATURES

- Complete E1 (CEPT) PCM-30/ISDN-PRI transceiver functionality
- Onboard long and short haul line interface for clock/data recovery and waveshaping
- 32-bit or 128-bit crystal-less jitter attenuator
- Frames to FAS, CAS, CCS, and CRC4 formats
- Integral HDLC controller with 64-byte buffers configurable for Sa Bits, DS0 or sub DS0 operation
- Dual two–frame elastic store slip buffers that can connect to asynchronous backplanes up to 8.192MHz
- Interleaving PCM Bus Operation
- 8–bit parallel control port that can be used directly on either multiplexed or non–multiplexed buses (Intel or Motorola)
- Extracts and inserts CAS signaling
- Detects and generates remote and AIS alarms
- Programmable output clocks for Fractional E1, H0, and H12 applications
- Fully independent transmit and receive functionality
- Full access to Si and Sa bits aligned with CRC-4 multiframe
- Four separate loopback functions for testing functions
- Large counters for bipolar and code violations, CRC4 code word errors, FAS word errors, and E bits
- IEEE 1149.1 JTAG-Boundary Scan Architecture
- Pin compatible with DS2154/52/352/552 SCTs
- 3.3V (DS21354) or 5V (DS21554) supply; low power CMOS
- 100-pin LQFP package (14mm X 14mm)



ORDERING INFORMATION

DS21354L (0^0 C to 70^0 C)
DS21354LN (-40^0 C to +85^0 C)

DS21554L (0^0 C to 70^0 C)
DS21554LN (-40^0 C to +85^0 C)

DESCRIPTION

The DS21354/554 Single-Chip Transceiver (SCT) contains all of the necessary functions for connection to E1 lines. The device is an upward compatible version of the DS2153 and DS2154 SCTs. The onboard clock/data recovery circuitry coverts the AMI/HDB3 E1 waveforms to an NRZ serial stream. The DS21354/554 automatically adjusts to E1 22AWG (0.6 mm) twisted–pair cables from 0 to over 2km in length. The device can generate the necessary G.703 waveshapes for both 75 ohm coax and 120 ohm twisted cables. The onboard jitter attenuator (selectable to either 32 bits or 128 bits) can be placed in either the transmit or receive data paths. The framer locates the frame and multiframe boundaries and monitors the data stream for alarms. It is also used for extracting and inserting signaling data, Si, and Sa bit information. The onboard HDLC controller can be used for Sa bit links or DS0s. The device contains a set of internal registers which the user can access and control the operation of the unit. Quick access via the parallel control port allows a single controller to handle many E1 lines. The device fully meets all of the latest E1 specifications including ITU-T G.703, G.704, G.706, G.823, G.732, and I.431, ETS 300 011, 300 233, and 300 166, as well as CTR12 and CTR4.

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3 INTRODUCTION

The DS21354/554 is a superset version of the popular DS2153 and DS2154 SCTs offering the new features listed below. All of the original features of the DS2153 and DS2154 have been retained and software created for the original devices is transferable into the DS21354/554.

New Features in the DS21354 and DS21554

FEATURE	SECTION
HDLC controller with 64-byte buffers for Sa bits or DS0s or sub DS0s	15
Interleaving PCM bus operation	18
IEEE 1149.1 JTAG-Boundary Scan Architecture	17
3.3V (DS21354 only) supply	2 and 3
Line Interface Support for the G.703 2.048 Synchronization Interface	16
Customer Disconnect Indication (...101010...) Generator	6
Open Drain Line Driver Option	16

New Features in the DS2154 (also in the DS21354 and DS21554)

FEATURE	SECTION
Option for non–multiplexed bus operation	1 and 2
Crystal–less jitter attenuation	12
Additional hardware signaling capability including: Receive signaling reinsertion to a backplane multiframe sync Availability of signaling in a separate PCM data stream Signaling freezing Interrupt generated on change of signaling data	7
Improved receive sensitivity: 0 dB to –43 dB	12
Per–channel code insertion in both transmit and receive paths	8
Expanded access to Sa and Si bits	11
RCL, RLOS, RRA, and RAIS alarms now interrupt on change of state	4
8.192 MHz clock synthesizer	1
Per–channel loopback	8
Addition of hardware pins to indicate carrier loss and signaling freeze	1
Line interface function can be completely decoupled from the framer/formatter to allow: Interface to optical, HDSL, and other NRZ interfaces “tap” the transmit and receive bipolar data streams for monitoring purposes Be able to corrupt data and insert framing errors, CRC errors, etc.	1
Transmit and receive elastic stores now have independent backplane clocks	1
Ability to monitor one DS0 channel in both the transmit and receive paths	6
Access to the data streams in between the framer/formatter and the elastic stores	1
AIS generation in the line interface that is independent of loopbacks	1 and 3
Transmit current limiter to meet the 50 mA short circuit requirement	12
Option to extend carrier loss criteria to a 1 ms period as per ETS 300 233	3
Automatic RAI generation to ETS 300 011 specifications	3

3.1 Functional Description

The analog AMI/HDB3 waveform off of the E1 line is transformer coupled into the RRING and RTIP pins of the DS21354/554. The device recovers clock and data from the analog signal and passes it through the jitter attenuation mux to the receive side framer where the digital serial stream is analyzed to locate the framing/multi-frame pattern. The DS21354/554 contains an active filter that reconstructs the analog received signal for the nonlinear losses that occur in transmission. The device has a usable receive sensitivity of 0 dB to –43 dB which allows the device to operate on cables over 2km in length. The receive side framer locates FAS frame and CRC and CAS multiframe boundaries as well as detects incoming alarms including, carrier loss, loss of synchronization, AIS and Remote Alarm. If needed, the receive side elastic store can be enabled in order to absorb the phase and frequency differences between the recovered E1 data stream and an asynchronous backplane clock which is provided at the RSYSCLK input. The clock applied at the RSYSCLK input can be either a 2.048/4.096/8.192 MHz clock or a 1.544 MHz clock.

The transmit side framer is totally independent from the receive side in both the clock requirements and characteristics. Data off of a backplane can be passed through a transmit side elastic store if necessary. The transmit formatter will provide the necessary frame/multiframe data overhead for E1 transmission.

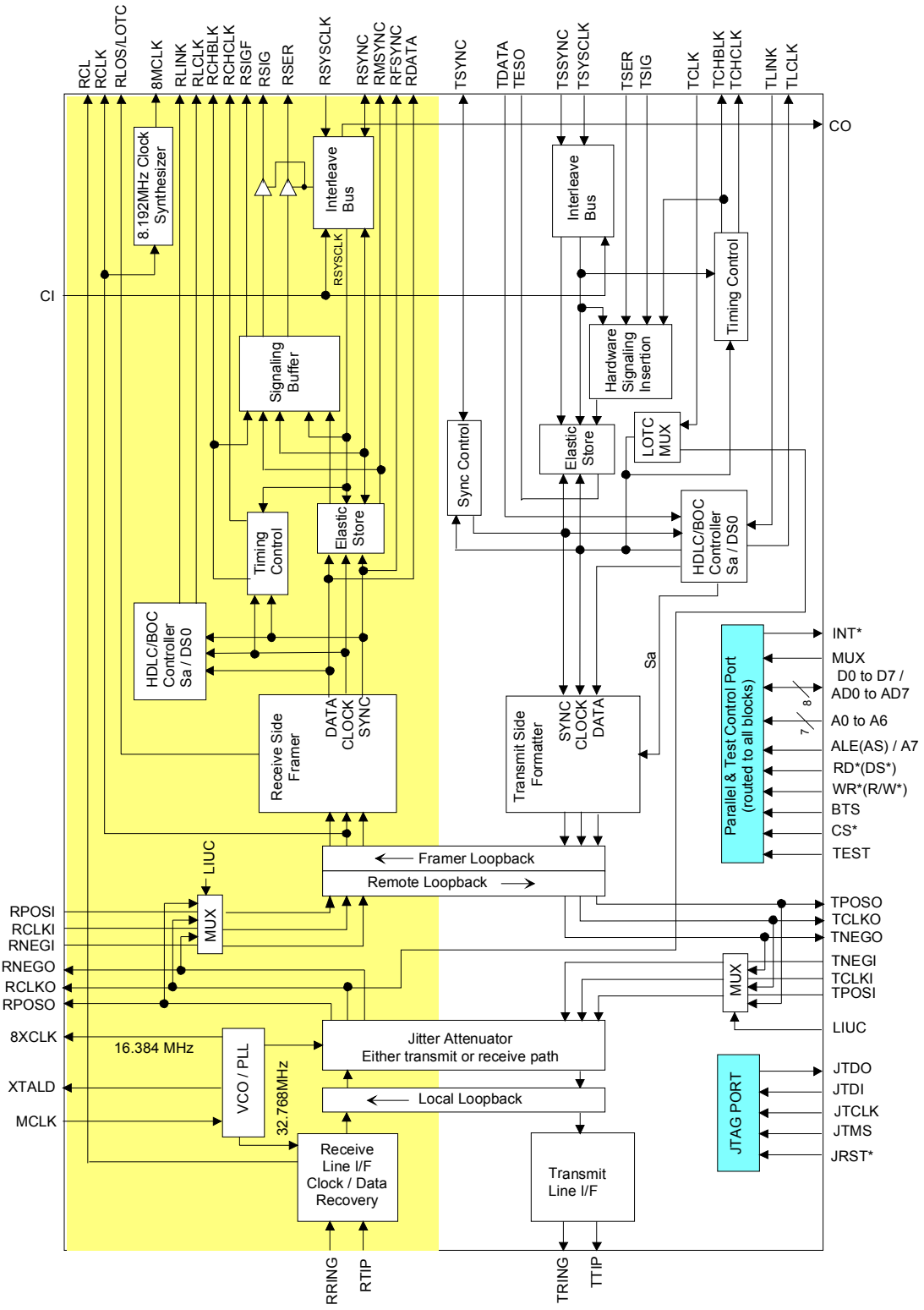
Reader's Note: This data sheet assumes a particular nomenclature of the E1 operating environment. In each 125 us frame, there are 32 eight–bit timeslots numbered 0 to 31. Timeslot 0 is transmitted first and received first. These 32 timeslots are also referred to as channels with a numbering scheme of 1 to 32. Timeslot 0 is identical to channel 1, timeslot 1 is identical to Channel 2, and so on. Each timeslot (or channel) is made up of eight bits which are numbered 1 to 8. Bit number 1 is the MSB and is transmitted first. Bit number 8 is the LSB and is transmitted last. The term "locked" is used to refer to two clock signals that are phase or frequency locked or derived from a common clock (i.e., a 1.544MHz clock may be locked to a 2.048MHz clock if they share the same 8KHz component). Throughout this data sheet, the following abbreviations will be used:

FAS	Frame Alignment Signal
CAS	Channel Associated Signaling
MF	Multiframe
Si	International bits
CRC4	Cyclical Redundancy Check
CCS	Common Channel Signaling
Sa	Additional bits
E-bit	CRC4 Error Bits

3.2 DOCUMENT REVISION HISTORY

Date	Notes
1-27-99	Initial release
1-28-99	Corrected TSYSCLK and RSYSCLK timing and added 4.096 MHz and 8.192 MHz timing
2-3-99	Corrected definition and label of TUDR bit in the THIR register.
2-11-99	Correct address of IBO register in text.
4-1-99	Add Receive Monitor Mode section
4-15-99	Add section on Protected Interfaces
5-7-99	Correct pin # and description of FMS in JTAG section
7-29-99	Add list of tables and figures
9-14-99	Add 10uf cap to interface examples
9-23-99	Correct definition of DS* in pin description.

DS21354/554 BLOCK DIAGRAM Figure 3-1



4 PIN DESCRIPTION

PIN DESCRIPTION SORTED BY PIN NUMBER Table 4-1

PIN	SYMBOL	TYPE	DESCRIPTION
1	RCHBLK	O	Receive Channel Block
2	JTMS	I	IEEE 1149.1 Test Mode Select
3	8MCLK	O	8.192 MHz Clock
4	JTCLK	I	IEEE 1149.1 Test Clock Signal
5	JTRST*	I	IEEE 1149.1 Test Reset
6	RCL	O	Receive Carrier Loss
7	JTDI	I	IEEE 1149.1 Test Data Input
8	NC	–	No Connect (do not connect any signal to this pin)
9	NC	–	No Connect (do not connect any signal to this pin)
10	JTDO	O	IEEE 1149.1 Test Data Output
11	BTS	I	Bus Type Select
12	LIUC	I	Line Interface Connect
13	8XCLK	O	Eight Times Clock
14	TEST	I	Test
15	NC	–	No Connect (do not connect any signal to this pin)
16	RTIP	I	Receive Analog Tip Input
17	RRING	I	Receive Analog Ring Input
18	RVDD	–	Receive Analog Positive Supply
19	RVSS	–	Receive Analog Signal Ground
20	RVSS	–	Receive Analog Signal Ground
21	MCLK	I	Master Clock Input
22	XTALD	O	Quartz Crystal Driver
23	NC	–	No Connect
24	RVSS	–	Receive Analog Signal Ground
25	INT*	O	Interrupt
26	NC	–	No Connect (do not connect any signal to this pin)
27	NC	–	No Connect (do not connect any signal to this pin)
28	NC	–	No Connect (do not connect any signal to this pin)
29	TTIP	O	Transmit Analog Tip Output
30	TVSS	–	Transmit Analog Signal Ground
31	TVDD	–	Transmit Analog Positive Supply
32	TRING	O	Transmit Analog Ring Output
33	TCHBLK	O	Transmit Channel Block
34	TLCLK	O	Transmit Link Clock
35	TLINK	I	Transmit Link Data
36	CI	I	Carry In
37	TSYNC	I/O	Transmit Sync
38	TPOSI	I	Transmit Positive Data Input
39	TNEGI	I	Transmit Negative Data Input
40	TCLKI	I	Transmit Clock Input
41	TCLKO	O	Transmit Clock Output
42	TNEGO	O	Transmit Negative Data Output
43	TPOSO	O	Transmit Positive Data Output

PIN	SYMBOL	TYPE	DESCRIPTION
44	DVDD	–	Digital Positive Supply
45	DVSS	–	Digital Signal Ground
46	TCLK	I	Transmit Clock
47	TSER	I	Transmit Serial Data
48	TSIG	I	Transmit Signaling Input
49	TESO	O	Transmit Elastic Store Output
50	TDATA	I	Transmit Data
51	TSYSCLK	I	Transmit System Clock
52	TSSYNC	I	Transmit System Sync
53	TCHCLK	O	Transmit Channel Clock
54	CO	O	Carry Out
55	MUX	I	Bus Operation
56	D0/AD0	I/O	Data Bus Bit0/ Address/Data Bus Bit 0
57	D1/AD1	I/O	Data Bus Bit1/ Address/Data Bus Bit 1
58	D2/AD2	I/O	Data Bus Bit 2/Address/Data Bus 2
59	D3/AD3	I/O	Data Bus Bit 3/Address/Data Bus Bit 3
60	DVSS	–	Digital Signal Ground
61	DVDD	–	Digital Positive Supply
62	D4/AD4	I/O	Data Bus Bit4/Address/Data Bus Bit 4
63	D5/AD5	I/O	Data Bus Bit 5/Address/Data Bus Bit 5
64	D6/AD6	I/O	Data Bus Bit 6/Address/Data Bus Bit 6
65	D7/AD7	I/O	Data Bus Bit 7/Address/Data Bus Bit 7
66	A0	I	Address Bus Bit 0
67	A1	I	Address Bus Bit 1
68	A2	I	Address Bus Bit 2
69	A3	I	Address Bus Bit 3
70	A4	I	Address Bus Bit 4
71	A5	I	Address Bus Bit 5
72	A6	I	Address Bus Bit 6
73	ALE(AS)/A7	I	Address Latch Enable /Address Bus Bit 7
74	RD*(DS*)	I	Read Input(Data Strobe)
75	CS*	I	Chip Select
76	FMS	I	Framer Mode Select
77	WR*(R/W*)	I	Write Input(Read/Write)
78	RLINK	O	Receive Link Data
79	RLCLK	O	Receive Link Clock
80	DVSS	–	Digital Signal Ground
81	DVDD	–	Digital Positive Supply
82	RCLK	O	Receive Clock
83	DVDD	–	Digital Positive Supply
84	DVSS	–	Digital Signal Ground
85	RDATA	O	Receive Data
86	RPOSI	I	Receive Positive Data Input
87	RNEGI	I	Receive Negative Data Input
88	RCLKI	I	Receive Clock Input
89	RCLKO	O	Receive Clock Output

PIN	SYMBOL	TYPE	DESCRIPTION
90	RNEGO	O	Receive Negative Data Output
91	RPOSO	O	Receive Positive Data Output
92	RCHCLK	O	Receive Channel Clock
93	RSIGF	O	Receive Signaling Freeze Output
94	RSIG	O	Receive Signaling Output
95	RSER	O	Receive Serial Data
96	RMSYNC	O	Receive Multiframe Sync
97	RFSYNC	O	Receive Frame Sync
98	RSYNC	I/O	Receive Sync
99	RLOS/LOTC	O	Receive Loss Of Sync/ Loss Of Transmit Clock
100	RSYSCLK	I	Receive System Clock

PIN DESCRIPTION BY SYMBOL Table 4-2

PIN	SYMBOL	TYPE	DESCRIPTION
3	8MCLK	O	8.192 MHz Clock
13	8XCLK	O	Eight Times Clock
66	A0	I	Address Bus Bit 0
67	A1	I	Address Bus Bit 1
68	A2	I	Address Bus Bit 2
69	A3	I	Address Bus Bit 3
70	A4	I	Address Bus Bit 4
71	A5	I	Address Bus Bit 5
72	A6	I	Address Bus Bit 6
73	ALE(AS)/A7	I	Address Latch Enable/ Address Bus Bit 7
11	BTS	I	Bus Type Select
36	CI	I	Carry In
54	CO	O	Carry Out
75	CS*	I	Chip Select
56	D0/AD0	I/O	Data Bus Bit0/ Address/Data Bus Bit 0
57	D1/AD1	I/O	Data Bus Bit1/ Address/Data Bus Bit 1
58	D2/AD2	I/O	Data Bus Bit 2/Address/Data Bus 2
59	D3/AD3	I/O	Data Bus Bit 3/Address/Data Bus Bit 3
62	D4/AD4	I/O	Data Bus Bit4/Address/Data Bus Bit 4
63	D5/AD5	I/O	Data Bus Bit 5/Address/Data Bus Bit 5
64	D6/AD6	I/O	Data Bus Bit 6/Address/Data Bus Bit 6
65	D7/AD7	I/O	Data Bus Bit 7/Address/Data Bus Bit 7
44	DVDD	–	Digital Positive Supply
81	DVDD	–	Digital Positive Supply
61	DVDD	–	Digital Positive Supply
83	DVDD	–	Digital Positive Supply
45	DVSS	–	Digital Signal Ground
60	DVSS	–	Digital Signal Ground
80	DVSS	–	Digital Signal Ground
84	DVSS	–	Digital Signal Ground
76	FMS	I	Framer Mode Select
25	INT*	O	Interrupt

PIN	SYMBOL	TYPE	DESCRIPTION
4	JTCLK	I	IEEE 1149.1 Test Clock Signal
7	JTDI	I	IEEE 1149.1 Test Data Input
10	JTDO	O	IEEE 1149.1 Test Data Output
2	JTMS	I	IEEE 1149.1 Test Mode Select
5	JTRST*	I	IEEE 1149.1 Test Reset
12	LIUC	I	Line Interface Connect
21	MCLK	I	Master Clock Input
55	MUX	I	Bus Operation
8	NC	–	No Connect (do not connect any signal to this pin)
9	NC	–	No Connect (do not connect any signal to this pin)
15	NC	–	No Connect (do not connect any signal to this pin)
23	NC	–	No Connect (do not connect any signal to this pin)
26	NC	–	No Connect (do not connect any signal to this pin)
27	NC	–	No Connect (do not connect any signal to this pin)
28	NC	–	No Connect (do not connect any signal to this pin)
1	RCHBLK	O	Receive Channel Block
92	RCHCLK	O	Receive Channel Clock
6	RCL	O	Receive Carrier Loss
82	RCLK	O	Receive Clock
88	RCLKI	I	Receive Clock Input
89	RCLKO	O	Receive Clock Output
74	RD*(DS*)	I	Read Input(Data Strobe)
85	RDATA	O	Receive Data
97	RFSYNC	O	Receive Frame Sync
79	RLCLK	O	Receive Link Clock
78	RLINK	O	Receive Link Data
99	RLOS/LOTC	O	Receive Loss Of Sync/ Loss Of Transmit Clock
96	RMSYNC	O	Receive Multiframe Sync
87	RNEGI	I	Receive Negative Data Input
90	RNEGO	O	Receive Negative Data Output
86	RPOSI	I	Receive Positive Data Input
91	RPOSO	O	Receive Positive Data Output
17	RRING	I	Receive Analog Ring Input
95	RSER	O	Receive Serial Data
94	RSIG	O	Receive Signaling Output
93	RSIGF	O	Receive Signaling Freeze Output
98	RSYNC	I/O	Receive Sync
100	RSYSCLK	I	Receive System Clock
16	RTIP	I	Receive Analog Tip Input
18	RVDD	–	Receive Analog Positive Supply
19	RVSS	–	Receive Analog Signal Ground
20	RVSS	–	Receive Analog Signal Ground
24	RVSS	–	Receive Analog Signal Ground
33	TCHBLK	O	Transmit Channel Block
53	TCHCLK	O	Transmit Channel Clock
46	TCLK	I	Transmit Clock

PIN	SYMBOL	TYPE	DESCRIPTION
40	TCLKI	I	Transmit Clock Input
41	TCLKO	O	Transmit Clock Output
50	TDATA	I	Transmit Data
49	TESO	O	Transmit Elastic Store Output
14	TEST	I	Test
34	TLCLK	O	Transmit Link Clock
35	TLINK	I	Transmit Link Data
39	TNEGI	I	Transmit Negative Data Input
42	TNEGO	O	Transmit Negative Data Output
38	TPOSI	I	Transmit Positive Data Input
43	TPOSO	O	Transmit Positive Data Output
32	TRING	O	Transmit Analog Ring Output
47	TSER	I	Transmit Serial Data
48	TSIG	I	Transmit Signaling Input
52	TSSYNC	I	Transmit System Sync
37	TSYNC	I/O	Transmit Sync
51	TSYSCLK	I	Transmit System Clock
29	TTIP	O	Transmit Analog Tip Output
31	TVDD	–	Transmit Analog Positive Supply
30	TVSS	–	Transmit Analog Signal Ground
77	WR*(R/W*)	I	Write Input(Read/Write)
22	XTALD	O	Quartz Crystal Driver

4.1 PIN FUNCTION DESCRIPTION

4.1.1 Transmit Side Pins

Signal Name: **TCLK**
Signal Description: **Transmit Clock**
Signal Type: **Input**
A 2.048 MHz primary clock. Used to clock data through the transmit side formatter.

Signal Name: **TSER**
Signal Description: **Transmit Serial Data**
Signal Type: **Input**
Transmit NRZ serial data. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.

Signal Name: **TCHCLK**
Signal Description: **Transmit Channel Clock**
Signal Type: **Output**
A 256 kHz clock which pulses high during the LSB of each channel. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for parallel to serial conversion of channel data.

Signal Name: **TCHBLK**
Signal Description: **Transmit Channel Block**
Signal Type: **Output**
A user programmable output that can be forced high or low during any of the 32 E1 channels. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all E1 channels are used such as Fractional E1, 384 kbps (H0), 768 kbps or ISDN–PRI . Also useful for locating individual channels in drop–and–insert applications, for external per–channel loopback, and for per–channel conditioning. See Section 12 for details.

Signal Name: **TSYSCLK**
Signal Description: **Transmit System Clock**
Signal Type: **Input**
1.544 MHz , 2.048 MHz , 4.096 MHz or 8.192 MHz clock. Only used when the transmit side elastic store function is enabled. Should be tied low in applications that do not use the transmit side elastic store. See section 18 on page 86 for details on 4.096 MHz and 8.192 MHz operation using the Interleave Bus Option.

Signal Name: **TLCLK**
Signal Description: **Transmit Link Clock**
Signal Type: **Output**
4 kHz to 20 kHz demand clock (Sa bits) for the TLINK input. See Section 18 for details.

Signal Name: **TLINK**
Signal Description: **Transmit Link Data**
Signal Type: **Input**
If enabled, this pin will be sampled on the falling edge of TCLK for data insertion into any combination of the Sa bit positions (Sa4 to Sa8). See Section 14.1 for details.

Signal Name: **TSYNC**
Signal Description: **Transmit Sync**
Signal Type: **Input / Output**
A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Via TCR1.1, the DS21354/554 can be programmed to output either a frame or multiframe pulse at this pin. This pin can also be configured as an input via TCR1.0. See Section 19 for details.

Signal Name: **TSSYNC**
Signal Description: **Transmit System Sync**
Signal Type: **Input**
Only used when the transmit side elastic store is enabled. A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Should be tied low in applications that do not use the transmit side elastic store.

Signal Name: **TSIG**
Signal Description: **Transmit Signaling Input**
Signal Type: **Input**
When enabled, this input will sample signaling bits for insertion into outgoing PCM E1 data stream. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.

Signal Name: **TESO**
Signal Description: **Transmit Elastic Store Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLK with data out of the transmit side elastic store whether the elastic store is enabled or not. This pin is normally tied to TDATA.

Signal Name: **TDATA**
Signal Description: **Transmit Data**
Signal Type: **Input**
Sampled on the falling edge of TCLK with data to be clocked through the transmit side formatter. This pin is normally tied to TESO.

Signal Name: **TPOSO**
Signal Description: **Transmit Positive Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLKO with the bipolar data out of the transmit side formatter. Can be programmed to source NRZ data via the Output Data Format (TCR2.2) control bit. This pin is normally tied to TPOSI.

Signal Name: **TNEGO**
Signal Description: **Transmit Negative Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLKO with the bipolar data out of the transmit side formatter. This pin is normally tied to TNEGI.

Signal Name: **TCLKO**
Signal Description: **Transmit Clock Output**
Signal Type: **Output**
Buffered output of signal that is clocking data through the transmit side formatter. This pin is normally tied to TCLKI.

Signal Name: **TPOSI**
Signal Description: **Transmit Positive Data Input**
Signal Type: **Input**
Sampled on the falling edge of TCLKI for data to be transmitted out onto the T1 line. Can be internally connected to TPOSO by tying the LIUC pin high. TPOSI and TNEGI can be tied together in NRZ applications.

Signal Name: **TNEGI**
Signal Description: **Transmit Negative Data Input**
Signal Type: **Input**
Sampled on the falling edge of TCLKI for data to be transmitted out onto the T1 line. Can be internally connected to TNEGO by tying the LIUC pin high. TPOSI and TNEGI can be tied together in NRZ applications.

Signal Name: **TCLKI**
Signal Description: **Transmit Clock Input**
Signal Type: **Input**
Line interface transmit clock. Can be internally connected to TCLKO by tying the LIUC pin high.

4.1.2 Receive Side Pins

Signal Name: **RLINK**
Signal Description: **Receive Link Data**
Signal Type: **Output**
Updated with the full recovered E1 data stream on the rising edge of RCLK.

Signal Name: **RLCLK**
Signal Description: **Receive Link Clock**
Signal Type: **Output**
4 kHz to 20 kHz clock (Sa bits) for the RLINK output. See Section 15 for details.

Signal Name: **RCLK**
Signal Description: **Receive Clock**
Signal Type: **Output**
2.048 MHz clock that is used to clock data through the receive side framer.

Signal Name: **RCHCLK**
Signal Description: **Receive Channel Clock**
Signal Type: **Output**
A 256 kHz clock which pulses high during the LSB of each channel. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for parallel to serial conversion of channel data.

Signal Name: **RCHBLK**
Signal Description: **Receive Channel Block**
Signal Type: **Output**
A user programmable output that can be forced high or low during any of the 32 E1 channels. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all E1 channels are used such as Fractional E1, 384 kbps service, 768 kbps, or ISDN–PRI. Also useful for locating individual channels in drop–and–insert applications, for external per–channel loopback, and for per–channel conditioning. See Section 12 for details.

Signal Name: **RSER**
Signal Description: **Receive Serial Data**
Signal Type: **Output**
Received NRZ serial data. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive side elastic store is enabled.

Signal Name: **RSYNC**
Signal Description: **Receive Sync**
Signal Type: **Input/Output**
An extracted pulse, one RCLK wide, is output at this pin which identifies either frame or CAS/CRC multiframe boundaries. If the receive side elastic store is enabled, then this pin can be enabled to be an input at which a frame or multiframe boundary pulse synchronous with RSYSCLK is applied.

Signal Name: **RFSYNC**
Signal Description: **Receive Frame Sync**
Signal Type: **Output**
An extracted 8 kHz pulse, one RCLK wide, is output at this pin which identifies frame boundaries.

Signal Name: **RMSYNC**
Signal Description: **Receive Multiframe Sync**
Signal Type: **Output**
If the receive side elastic store is enabled, an extracted pulse, one RSYSCLK wide, is output at this pin which identifies multiframe boundaries. If the receive side elastic store is disabled, then this output will output multiframe boundaries associated with RCLK.

Signal Name: **RDATA**
Signal Description: **Receive Data**
Signal Type: **Output**
Updated on the rising edge of RCLK with the data out of the receive side framer.

Signal Name: **RSYSCLK**
Signal Description: **Receive System Clock**
Signal Type: **Input**
1.544 MHz , 2.048 MHz , 4.096 MHz or 8.192 MHz clock. Only used when the receive side elastic store function is enabled. Should be tied low in applications that do not use the receive side elastic store. See section 18 on page 115 for details on 4.096 MHz and 8.192 MHz operation using the Interleave Bus Option.

Signal Name: **RSIG**
Signal Description: **Receive Signaling Output**
Signal Type: **Output**
Outputs signaling bits in a PCM format. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive side elastic store is enabled.

Signal Name: **RLOS/LOTC**
Signal Description: **Receive Loss of Sync / Loss of Transmit Clock**
Signal Type: **Output**
A dual function output that is controlled by the TCR2.0 control bit. This pin can be programmed to either toggle high when the synchronizer is searching for the frame and multiframe or to toggle high if the TCLK pin has not been toggled for 5 µsec.

Signal Name: **RCL**
Signal Description: **Receive Carrier Loss**
Signal Type: **Output**
Set high when the line interface detects a carrier loss.

Signal Name: **RSIGF**
Signal Description: **Receive Signaling Freeze**
Signal Type: **Output**
Set high when the signaling data is frozen via either automatic or manual intervention. Used to alert downstream equipment of the condition.

Signal Name: **8MCLK**
Signal Description: **8 MHz Clock**
Signal Type: **Output**
An 8.192MHz clock output that is referenced to the clock that is output at the RCLK pin.

Signal Name: **RPOSO**
Signal Description: **Receive Positive Data Input**
Signal Type: **Output**
Updated on the rising edge of RCLKO with bipolar data out of the line interface. This pin is normally tied to RPOSI.

Signal Name: **RNEGO**
Signal Description: **Receive Negative Data Input**
Signal Type: **Output**
Updated on the rising edge of RCLKO with the bipolar data out of the line interface. This pin is normally tied to RPOSI.

Signal Name: **RCLKO**
Signal Description: **Receive Clock Output**
Signal Type: **Output**
Buffered recovered clock from the T1 line. This pin is normally tied to RCLKI.

Signal Name: **RPOSI**
Signal Description: **Receive Positive Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLKI for data to be clocked through the receive side framer. RPOSI and RNEGI can be tied together for a NRZ interface. Can be internally connected to RPOSO by tying the LIUC pin high.

Signal Name: **RNEGI**
Signal Description: **Receive Negative Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLKI for data to be clocked through the receive side framer. RPOSI and RNEGI can be tied together for a NRZ interface. Can be internally connected to RNEGO by tying the LIUC pin high.

Signal Name: **RCLKI**
Signal Description: **Receive Clock Input**
Signal Type: **Input**
Clock used to clock data through the receive side framer. This pin is normally tied to RCLKO. Can be internally connected to RCLKO by tying the LIUC pin high.

4.1.3 Parallel Control Port Pins

Signal Name: **INT***
Signal Description: **Interrupt**
Signal Type: **Output**
Flags host controller during conditions and change of conditions defined in the Status Registers 1 and 2 and the HDLC Status Register. Active low, open drain output

Signal Name: **FMS**
Signal Description: **Framer Mode Select**
Signal Type: **Input**
Selects the DS2154 mode when high or the DS21354/554 mode when low. If high, the JTRST* is internally pulled low. If low, JTRST* has normal JTAG functionality. This pin has a 10k pull up resistor.

Signal Name: **Test**
Signal Description: **3–State Control**
Signal Type: **Input**
Set high to 3–state all output and I/O pins (including the parallel control port). Set low for normal operation. Useful in board level testing.

Signal Name: **MUX**
Signal Description: **Bus Operation**
Signal Type: **Input**
Set low to select non–multiplexed bus operation. Set high to select multiplexed bus operation.

Signal Name: **AD0 to AD7**
Signal Description: **Data Bus [D0 to D7] or Address/Data Bus**
Signal Type: **Input**
In non–multiplexed bus operation (MUX = 0), serves as the data bus. In multiplexed bus operation (MUX = 1), serves as a 8–bit multiplexed address / data bus.

Signal Name: **A0 to A6**
Signal Description: **Address Bus**
Signal Type: **Input**
In non–multiplexed bus operation (MUX = 0), serves as the address bus. In multiplexed bus operation (MUX = 1), these pins are not used and should be tied low.

Signal Name: **BTS**
Signal Description: **Bus Type Select**
Signal Type: **Input**
Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the RD*(DS*), ALE(AS), and WR*(R/W*) pins. If BTS = 1, then these pins assume the function listed in parenthesis ().

Signal Name: **RD*(DS*)**
Signal Description: **Read Input - Data Strobe**
Signal Type: **Input**
RD* and DS* are active low signals. DS active HIGH when MUX = 1. See bus timing diagrams.

Signal Name: **CS***
Signal Description: **Chip Select**
Signal Type: **Input**
Must be low to read or write to the device. CS* is an active low signal.

Signal Name: **ALE(AS)/a7**
Signal Description: **Address Latch Enable(Address Strobe) or A7**
Signal Type: **Input**
In non–multiplexed bus operation (MUX = 0), serves as the upper address bit. In multiplexed bus operation (MUX = 1), serves to de-multiplex the bus on a positive–going edge.

Signal Name: **WR*(R/W*)**
Signal Description: **Write Input(Read/Write)**
Signal Type: **Input**
WR* is an active low signal.

4.1.4 JTAG Test Access Port Pins

Signal Name: **JTRST***
Signal Description: **IEEE 1149.1 Test Reset**
Signal Type: **Input**
This signal is used to asynchronously reset the test access port controller. At power up, JTRST* must be toggled from low to high. This action will set the device into JTAG DEVICE ID mode enabling the test access port features. This pin has a 10k pull up resistor. When FMS=1, this pin is tied low internally. Tie JTRST* low if JTAG is not used and the framer is in DS21354/554 mode (FMS low).

Signal Name: **JTMS**
Signal Description: **IEEE 1149.1 Test Mode Select**
Signal Type: **Input**
This pin is sampled on the rising edge of JTCLK and is used to place the test access port into the various defined IEEE 1149.1 states. This pin has a 10k pull up resistor.

Signal Name: **JTCLK**
Signal Description: **IEEE 1149.1 Test Clock Signal**
Signal Type: **Input**
This signal is used to shift data into JTDI on the rising edge and out of JTDO on the falling edge.

Signal Name: **JTDI**
Signal Description: **IEEE 1149.1 Test Data Input**
Signal Type: **Input**
Test instructions and data are clocked into this pin on the rising edge of JTCLK. This pin has a 10k pull up resistor.

Signal Name: **JTDO**
Signal Description: **IEEE 1149.1 Test Data Output**
Signal Type: **Output**
Test instructions and data are clocked out of this pin on the falling edge of JTCLK. If not used, this pin should be left unconnected.

4.1.5 Interleave Bus Operation Pins

Signal Name: **CI**
Signal Description: **Carry In**
Signal Type: **Input**
A rising edge on this pin causes RSER and RSIG to come out of high Z state and TSER and TSIG to start sampling on the next rising edge of RSYSCLK/TSYSCLK beginning an I/O sequence of 8 or 256 bits of data. This pin has a 10k pull up resistor.

Signal Name: **CO**
Signal Description: **Carry Out**
Signal Type: **Output**
An output that is set high when the last bit of the 8 or 256 IBO output sequence has occurred on RSER and RSIG.

4.1.6 Line Interface Pins

Signal Name: **MCLK**
Signal Description: **Master Clock Input**
Signal Type: **Input**
A 2.048 MHz (+/-50 ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation. A quartz crystal of 2.048 MHz may be applied across MCLK and XTALD instead of the TTL level clock source.

Signal Name: **XTALD**
Signal Description: **Quartz Crystal Driver**
Signal Type: **Output**
A quartz crystal of 2.048 MHz may be applied across MCLK and XTALD instead of a TTL level clock source at MCLK. Leave open circuited if a TTL clock source is applied at MCLK.

Signal Name: **8XCLK**
Signal Description: **Eight Times Clock**
Signal Type: **Output**
A 16.384 MHz clock that is frequency locked to the 2.048 MHz clock provided from the clock/data recovery block (if the jitter attenuator is enabled on the receive side) or from the TCLKI pin (if the jitter attenuator is enabled on the transmit side). Can be internally disabled via TEST2 register if not needed.

Signal Name: **LIUC**
Signal Description: **Line Interface Connect**
Signal Type: **Input**
Tie low to separate the line interface circuitry from the framer/formatter circuitry and activate the TPOSI/TNEGI/TCLKI/RPOSI/RNEGI/RCLKI pins. Tie high to connect the line interface circuitry to the framer/formatter circuitry and deactivate the TPOSI/TNEGI/TCLKI/RPOSI/RNEGI/RCLKI pins. When LIUC is tied high, the TPOSI/TNEGI/TCLKI/ RPOSI/RNEGI/RCLKI pins should be tied low.

Signal Name: **RTIP & RRING**
Signal Description: **Receive Tip and Ring**
Signal Type: **Input**
Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the E1 line. See Section 16 for details.

Signal Name: **TTIP & TRING**

Signal Description: **Transmit Tip and Ring**
Signal Type: **Output**
Analog line driver outputs. These pins connect via a step–up transformer to the E1 line. See Section 0 for details.

4.1.7 Supply Pins

Signal Name: **DVDD**
Signal Description: **Digital Positive Supply**
Signal Type: **Supply**
5.0 volts +/-5% (DS21554) or 3.3 volts +/-5% (DS21354). Should be tied to the RVDD and TVDD pins.

Signal Name: **RVDD**
Signal Description: **Receive Analog Positive Supply**
Signal Type: **Supply**
5.0 volts +/-5% (DS21554) or 3.3 volts +/-5% (DS21354). Should be tied to the DVDD and TVDD pins.

Signal Name: **TVDD**
Signal Description: **Transmit Analog Positive Supply**
Signal Type: **Supply**
5.0 volts +/-5% (DS21554) or 3.3 volts +/-5% (DS21354). Should be tied to the RVDD and DVDD pins.

Signal Name: **DVSS**
Signal Description: **Digital Signal Ground**
Signal Type: **Supply**
0.0 volts. Should be tied to the RVSS and TVSS pins.

Signal Name: **RVSS**
Signal Description: **Receive Analog Signal Ground**
Signal Type: **Supply**
0.0 volts. Should be tied to DVSS and TVSS.

Signal Name: **TVSS**
Signal Description: **Transmit Analog Signal Ground**
Signal Type: **Supply**
0.0 volts. Should be tied to DVSS and RVSS.

5 PARALLEL PORT

The DS21354/554 is controlled via either a non–multiplexed (MUX = 0) or a multiplexed (MUX = 1) bus by an external microcontroller or microprocessor. The device can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parenthesis (). See the timing diagrams in the A.C. Electrical Characteristics in Section 21 for more details.

5.1 REGISTER MAP

REGISTER MAP SORTED BY ADDRESS Table 5-1

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
00	R	BPV or Code Violation Count 1	VCR1
01	R	BPV or Code Violation Count 2	VCR2
02	R	CRC4 Error Count 1 / FAS Error Count 1	CRCCR1
03	R	CRC4 Error Count 2	CRCCR2
04	R	E-Bit Count 1 / FAS Error Count 2	EBCR1
05	R	E-Bit Count 2	EBCR2
06	R/W	Status 1	SR1
07	R/W	Status 2	SR2
08	R/W	Receive Information	RIR
09	–	Not used	(set to 00h)
0A	–	Not used	(set to 00h)
0B	–	Not used	(set to 00h)
0C	–	Not used	(set to 00h)
0D	–	Not used	(set to 00h)
0E	–	Not used	(set to 00h)
0F	R	Device ID	IDR
10	R/W	Receive Control 1	RCR1
11	R/W	Receive Control 2	RCR2
12	R/W	Transmit Control 1	TCR1
13	R/W	Transmit Control 2	TCR2
14	R/W	Common Control 1	CCR1
15	R/W	Test 1	TEST1 (set to 00h)
16	R/W	Interrupt Mask 1	IMR1
17	R/W	Interrupt Mask 2	IMR2
18	R/W	Line Interface Control Register	LICR
19	R/W	Test 2	TEST2 (set to 00h)
1A	R/W	Common Control 2	CCR2
1B	R/W	Common Control 3	CCR3
1C	R/W	Transmit Sa Bit Control	TSaCR
1D	R/W	Common Control 6	CCR6
1E	R	Synchronizer Status	SSR
1F	R	Receive Non-Align Frame	RNAF
20	R/W	Transmit Align Frame	TAF
21	R/W	Transmit Non-Align Frame	TNAF
22	R/W	Transmit Channel Blocking 1	TCBR1
23	R/W	Transmit Channel Blocking 2	TCBR2
24	R/W	Transmit Channel Blocking 3	TCBR3
25	R/W	Transmit Channel Blocking 4	TCBR4
26	R/W	Transmit Idle 1	TIR1
27	R/W	Transmit Idle 2	TIR2
28	R/W	Transmit Idle 3	TIR3
29	R/W	Transmit Idle 4	TIR4

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
2A	R/W	Transmit Idle Definition	TIDR
2B	R/W	Receive Channel Blocking 1	RCBR1
2C	R/W	Receive Channel Blocking 2	RCBR2
2D	R/W	Receive Channel Blocking 3	RCBR3
2E	R/W	Receive Channel Blocking 4	RCBR4
2F	R	Receive Align Frame	RAF
30	R	Receive Signaling 1	RS1
31	R	Receive Signaling 2	RS2
32	R	Receive Signaling 3	RS3
33	R	Receive Signaling 4	RS4
34	R	Receive Signaling 5	RS5
35	R	Receive Signaling 6	RS6
36	R	Receive Signaling 7	RS7
37	R	Receive Signaling 8	RS8
38	R	Receive Signaling 9	RS9
39	R	Receive Signaling 10	RS10
3A	R	Receive Signaling 11	RS11
3B	R	Receive Signaling 12	RS12
3C	R	Receive Signaling 13	RS13
3D	R	Receive Signaling 14	RS14
3E	R	Receive Signaling 15	RS15
3F	R	Receive Signaling 16	RS16
40	R/W	Transmit Signaling 1	TS1
41	R/W	Transmit Signaling 2	TS2
42	R/W	Transmit Signaling 3	TS3
43	R/W	Transmit Signaling 4	TS4
44	R/W	Transmit Signaling 5	TS5
45	R/W	Transmit Signaling 6	TS6
46	R/W	Transmit Signaling 7	TS7
47	R/W	Transmit Signaling 8	TS8
48	R/W	Transmit Signaling 9	TS9
49	R/W	Transmit Signaling 10	TS10
4A	R/W	Transmit Signaling 11	TS11
4B	R/W	Transmit Signaling 12	TS12
4C	R/W	Transmit Signaling 13	TS13
4D	R/W	Transmit Signaling 14	TS14
4E	R/W	Transmit Signaling 15	TS15
4F	R/W	Transmit Signaling 16	TS16
50	R/W	Transmit Si Bits Align Frame	TSiAF
51	R/W	Transmit Si Bits Non-Align Frame	TSiNAF
52	R/W	Transmit Remote Alarm Bits	TRA
53	R/W	Transmit Sa4 Bits	TSa4
54	R/W	Transmit Sa5 Bits	TSa5
55	R/W	Transmit Sa6 Bits	TSa6
56	R/W	Transmit Sa7 Bits	TSa7

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
57	R/W	Transmit Sa8 Bits	TSa8
58	R	Receive Si bits Align Frame	RSiAF
59	R	Receive Si bits Non-Align Frame	RSiNAF
5A	R	Receive Remote Alarm Bits	RRA
5B	R	Receive Sa4 Bits	RSa4
5C	R	Receive Sa5 Bits	RSa5
5D	R	Receive Sa6 Bits	RSa6
5E	R	Receive Sa7 Bits	RSa7
5F	R	Receive Sa8 Bits	RSa8
60	R/W	Transmit Channel 1	TC1
61	R/W	Transmit Channel 2	TC2
62	R/W	Transmit Channel 3	TC3
63	R/W	Transmit Channel 4	TC4
64	R/W	Transmit Channel 5	TC5
65	R/W	Transmit Channel 6	TC6
66	R/W	Transmit Channel 7	TC7
67	R/W	Transmit Channel 8	TC8
68	R/W	Transmit Channel 9	TC9
69	R/W	Transmit Channel 10	TC10
6A	R/W	Transmit Channel 11	TC11
6B	R/W	Transmit Channel 12	TC12
6C	R/W	Transmit Channel 13	TC13
6D	R/W	Transmit Channel 14	TC14
6E	R/W	Transmit Channel 15	TC15
6F	R/W	Transmit Channel 16	TC16
70	R/W	Transmit Channel 17	TC17
71	R/W	Transmit Channel 18	TC18
72	R/W	Transmit Channel 19	TC19
73	R/W	Transmit Channel 20	TC20
74	R/W	Transmit Channel 21	TC21
75	R/W	Transmit Channel 22	TC22
76	R/W	Transmit Channel 23	TC23
77	R/W	Transmit Channel 24	TC24
78	R/W	Transmit Channel 25	TC25
79	R/W	Transmit Channel 26	TC26
7A	R/W	Transmit Channel 27	TC27
7B	R/W	Transmit Channel 28	TC28
7C	R/W	Transmit Channel 29	TC29
7D	R/W	Transmit Channel 30	TC30
7E	R/W	Transmit Channel 31	TC31
7F	R/W	Transmit Channel 32	TC32
80	R/W	Receive Channel 1	RC1
81	R/W	Receive Channel 2	RC2
82	R/W	Receive Channel 3	RC3
83	R/W	Receive Channel 4	RC4

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
84	R/W	Receive Channel 5	RC5
85	R/W	Receive Channel 6	RC6
86	R/W	Receive Channel 7	RC7
87	R/W	Receive Channel 8	RC8
88	R/W	Receive Channel 9	RC9
89	R/W	Receive Channel 10	RC10
8A	R/W	Receive Channel 11	RC11
8B	R/W	Receive Channel 12	RC12
8C	R/W	Receive Channel 13	RC13
8D	R/W	Receive Channel 14	RC14
8E	R/W	Receive Channel 15	RC15
8F	R/W	Receive Channel 16	RC16
90	R/W	Receive Channel 17	RC17
91	R/W	Receive Channel 18	RC18
92	R/W	Receive Channel 19	RC19
93	R/W	Receive Channel 20	RC20
94	R/W	Receive Channel 21	RC21
95	R/W	Receive Channel 22	RC22
96	R/W	Receive Channel 23	RC23
97	R/W	Receive Channel 24	RC24
98	R/W	Receive Channel 25	RC25
99	R/W	Receive Channel 26	RC26
9A	R/W	Receive Channel 27	RC27
9B	R/W	Receive Channel 28	RC28
9C	R/W	Receive Channel 29	RC29
9D	R/W	Receive Channel 30	RC30
9E	R/W	Receive Channel 31	RC31
9F	R/W	Receive Channel 32	RC32
A0	R/W	Transmit Channel Control 1	TCC1
A1	R/W	Transmit Channel Control 2	TCC2
A2	R/W	Transmit Channel Control 3	TCC3
A3	R/W	Transmit Channel Control 4	TCC4
A4	R/W	Receive Channel Control 1	RCC1
A5	R/W	Receive Channel Control 2	RCC2
A6	R/W	Receive Channel Control 3	RCC3
A7	R/W	Receive Channel Control 4	RCC4
A8	R/W	Common Control 4	CCR4
A9	R	Transmit DS0 Monitor	TDS0M
AA	R/W	Common Control 5	CCR5
AB	R	Receive DS0 Monitor	RDS0M
AC	R/W	Test 3	TEST3 (set to 00h)
AD	-	Not used	(set to 00h)
AE	-	Not used	(set to 00h)
AF	-	Not used	(set to 00h)
B0	R/W	HDLC Control Register	HCR

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
B1	R/W	HDLC Status Register	HSR
B2	R/W	HDLC Interrupt Mask Register	HIMR
B3	R/W	Receive HDLC Information Register	RHIR
B4	R/W	Receive HDLC FIFO Register	RHFR
B5	R/W	Interleave Bus Operation Register	IBO
B6	R/W	Transmit HDLC Information Register	THIR
B7	R/W	Transmit HDLC FIFO Register	THFR
B8	R/W	Receive HDLC DS0 Control Register 1	RDC1
B9	R/W	Receive HDLC DS0 Control Register 2	RDC2
BA	R/W	Transmit HDLC DS0 Control Register 1	TDC1
BB	R/W	Transmit HDLC DS0 Control Register 2	TDC2
BC	-	Not used	(set to 00h)
BD	-	Not used	(set to 00h)
BE	-	Not used	(set to 00h)
BF	-	Not used	(set to 00h)

NOTES:

1. Test Registers are used only by the factory; these registers must be cleared (set to all zeros) on power– up initialization to insure proper operation.
2. Register banks Cxh, Dxh, Exh, and Fxh are not accessible.

6 CONTROL, ID, AND TEST REGISTERS

The operation of the DS21354/554 is configured via a set of ten control registers. Typically, the control registers are only accessed when the system is first powered up. Once the device has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two Receive Control Register (RCR1 and RCR2), two Transmit Control Registers (TCR1 and TCR2), and six Common Control Registers (CCR1 to CCR6). Each of the ten registers are described in this section.

There is a device Identification Register (IDR) at address 0Fh. The MSB of this read–only register is fixed to a one indicating that an E1 SCT is present. The next 3 MSBs are used to indicate which E1 device is present; DS2154, DS21354, or DS21554. The T1 pin–for–pin compatible SCTs will have a logic zero in the MSB position with the following 3 MSBs indicating which T1 SCT is present; DS2152, DS21352, or DS21552. Table 4-1 represents the possible variations of these bits and the associated SCT.

DEVICE ID BIT MAP Table 6-1

SCT	T1/E1	bit 6	bit 5	bit 4
DS2152	0	0	0	0
DS21352	0	0	0	1
DS21552	0	0	1	0
DS2154	1	0	0	0
DS21354	1	0	0	1
DS21554	1	0	1	0

The lower four bits of the IDR are used to display the die revision of the chip.

The Test registers at addresses 09, 15, 19, and AC hex are used by the factory in testing the DS21354/554. On power-up, the Test registers should be set to 00h in order for the DS21354/554 to operate properly.

6.1 Power–Up Sequence

On power–up, after the supplies are stable the DS21354/554 should be configured for operation by writing to all of the internal registers (this includes setting the Test Registers to 00h) since the contents of the internal registers cannot be predicted on power–up. The LIRST (CCR5.7) should be toggled from zero to one to reset the line interface circuitry (it will take the device about 40ms to recover from the LIRST bit being toggled). Finally, after the TSYSCLK and RSYSCLK inputs are stable, the ESR bits (CCR6.0 & CCR6.1) should be toggled from a zero to a one (this step can be skipped if the elastic stores are disabled).

IDR: DEVICE IDENTIFICATION REGISTER (Address=0F Hex)

(MSB)							(LSB)
T1E1	Bit 6	Bit 5	Bit 4	ID3	ID2	ID1	ID0

SYMBOL	POSITION	NAME AND DESCRIPTION
T1E1	IDR.7	T1 or E1 Chip Determination Bit. Set to 1. 0=T1 chip 1=E1 chip
Bit 6	IDR.6	Bit 6. See Table 6-1
Bit 5	IDR.5	Bit 5. See Table 6-1
Bit 4	IDR.4	Bit 4. See Table 6-1
ID3	IDR.3	Chip Revision Bit 3. MSB of a decimal code that represents the chip revision.
ID2	IDR.1	Chip Revision Bit 2.
ID1	IDR.2	Chip Revision Bit 1.
ID0	IDR.0	Chip Revision Bit 0. LSB of a decimal code that represents the chip revision.

RCR1: RECEIVE CONTROL REGISTER 1 (Address=10 Hex)

(MSB)							(LSB)
RSMF	RSM	RSIO	–	–	FRC	SYNCE	RESYNC

SYMBOL	POSITION	NAME AND DESCRIPTION
RSMF	RCR1.7	RSYNC Multiframe Function. Only used if the RSYNC pin is programmed in the multiframe mode (RCR1.6=1). 0 = RSYNC outputs CAS multiframe boundaries 1 = RSYNC outputs CRC4 multiframe boundaries
RSM	RCR1.6	RSYNC Mode Select. 0 = frame mode (see the timing in Section 19-1) 1 = multiframe mode (see the timing in Section 19-1)
RSIO	RCR1.5	RSYNC I/O Select. (note: this bit must be set to zero when RCR2.1=0). 0 = RSYNC is an output (depends on RCR1.6) 1 = RSYNC is an input (only valid if elastic store enabled)
–	RCR1.4	Not Assigned. Should be set to zero when written.

SYMBOL	POSITION	NAME AND DESCRIPTION
–	RCR1.3	Not Assigned. Should be set to zero when written.
FRC	RCR1.2	Frame Resync Criteria. 0 = resync if FAS received in error 3 consecutive times 1 = resync if FAS or bit 2 of non–FAS is received in error 3 consecutive times
SYNCE	RCR1.1	Sync Enable. 0 = auto resync enabled 1 = auto resync disabled
RESYNC	RCR1.0	Resync. When toggled from low to high, a resync is initiated. Must be cleared and set again for a subsequent resync.

6.1.1 Synchronization and Re-synchronization

Once synchronization is accomplished there are certain criteria that can cause a re-synchronization. These criteria are detailed in Table 6-2. Also see Figure 19-14 for a flow chart of the synchronization process.

SYNC/RESYNC CRITERIA Table 6-2

FRAME OR MULTIFRAME LEVEL	SYNC CRITERIA	RESYNC CRITERIA	ITU SPEC.
FAS	FAS present in frame N and N + 2, and FAS not present in frame N + 1	Three consecutive incorrect FAS received Alternate (RCR1.2=1) the above criteria is met or three consecutive incorrect bit 2 of non–FAS received	G.706 4.1.1 4.1.2
CRC4	Two valid MF alignment words found within 8 ms	915 or more CRC4 code words out of 1000 received in error	G.706 4.2 and 4.3.2
CAS	Valid MF alignment word found and previous timeslot 16 contains code other than all zeros	Two consecutive MF alignment words received in error	G.732 5.2

RCR2: RECEIVE CONTROL REGISTER 2 (Address=11 Hex)

(MSB)							(LSB)
Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	RBCS	RESE	–

SYMBOL	POSITION	NAME AND DESCRIPTION
Sa8S	RCR2.7	**Sa8 Bit Select.** Set to one to have RLCLK pulse at the Sa8 bit position; set to zero to force RLCLK low during Sa8 bit position. See Section 19.1 for timing details.
Sa7S	RCR2.6	**Sa7 Bit Select.** Set to one to have RLCLK pulse at the Sa7 bit position; set to zero to force RLCLK low during Sa7 bit position. See Section 19.1 for timing details.
Sa6S	RCR2.5	**Sa6 Bit Select.** Set to one to have RLCLK pulse at the Sa6 bit position; set to zero to force RLCLK low during Sa6 bit position. See Section 19.1 for timing details.
Sa5S	RCR2.4	**Sa5 Bit Select.** Set to one to have RLCLK pulse at the Sa5 bit position; set to zero to force RLCLK low during Sa5 bit position. See Section 19.1 for timing details.
Sa4S	RCR2.3	**Sa4 Bit Select.** Set to one to have RLCLK pulse at the Sa4 bit position; set to zero to force RLCLK low during Sa4 bit position. See Section 19.1 for timing details.
RBCS	RCR2.2	**Receive Side Backplane Clock Select.** 0 = if RSYSCLK is 1.544 MHz 1 = if RSYSCLK is 2.048/4.096/8.192 MHz
RESE	RCR2.1	**Receive Side Elastic Store Enable.** 0 = elastic store is bypassed 1 = elastic store is enabled
–	RCR2.0	**Not Assigned.** Should be set to zero when written.

TCR1: TRANSMIT CONTROL REGISTER 1 (Address=12 Hex)

(MSB)							(LSB)
ODF	TFPT	T16S	TUA1	TSiS	TSA1	TSM	TSIO

SYMBOL	POSITION	NAME AND DESCRIPTION
ODF	TCR1.7	**Output Data Format.** 0 = bipolar data at TPOSO and TNEGO 1 = NRZ data at TPOSO; TNEGO=0
TFPT	TCR1.6	**Transmit Timeslot 0 Pass Through.** 0 = FAS bits/Sa bits/Remote Alarm sourced internally from the TAF and TNAF registers 1 = FAS bits/Sa bits/Remote Alarm sourced from TSER
T16S	TCR1.5	**Transmit Timeslot 16 Data Select.** 0 = sample timeslot 16 at TSER pin 1 = source timeslot 16 from TS0 to TS15 registers
TUA1	TCR1.4	**Transmit Unframed All Ones.** 0 = transmit data normally 1 = transmit an unframed all one's code at TPOSO and TNEGO

SYMBOL	POSITION	NAME AND DESCRIPTION
TSiS	TCR1.3	**Transmit International Bit Select.** 0 = sample Si bits at TSER pin 1 = source Si bits from TAF and TNAF registers (in this mode, TCR1.6 must be set to 0)
TSA1	TCR1.2	**Transmit Signaling All Ones.** 0 = normal operation 1 = force timeslot 16 in every frame to all ones
TSM	TCR1.1	**TSYNC Mode Select.** 0 = frame mode (see the timing in Section 19.2) 1 = CAS and CRC4 multiframe mode (see the timing in Section 19.2)
TSIO	TCR1.0	**TSYNC I/O Select.** 0 = TSYNC is an input 1 = TSYNC is an output

NOTE:

See Figure 19-15 for more details about how the Transmit Control Registers affect the operation of the DS21354/554.

TCR2: TRANSMIT CONTROL REGISTER 2 (Address=13 Hex)

(MSB)							(LSB)
Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	ODM	AEBE	PF

SYMBOL	POSITION	NAME AND DESCRIPTION
Sa8S	TCR2.7	**Sa8 Bit Select.** Set to one to source the Sa8 bit from the TLINK pin; set to zero to not source the Sa8 bit. See Section 19.2 for timing details.
Sa7S	TCR2.6	**Sa7 Bit Select.** Set to one to source the Sa7 bit from the TLINK pin; set to zero to not source the Sa7 bit. See Section 19.2 for timing details.
Sa6S	TCR2.5	**Sa6 Bit Select.** Set to one to source the Sa6 bit from the TLINK pin; set to zero to not source the Sa6 bit. See Section 19.2 for timing details.
Sa5S	TCR2.4	**Sa5 Bit Select.** Set to one to source the Sa5 bit from the TLINK pin; set to zero to not source the Sa5 bit. See Section 19.2 for timing details.
Sa4S	TCR2.3	**Sa4 Bit Select.** Set to one to source the Sa4 bit from the TLINK pin; set to zero to not source the Sa4 bit. See Section 19.2 for timing details.
ODM	TCR2.2	**Output Data Mode.** 0 = pulses at TPOSO and TNEGO are one full TCLKO period wide 1 = pulses at TPOSO and TNEGO are 1/2 TCLKO period wide
AEBE	TCR2.1	**Automatic E–Bit Enable.** 0 = E–bits not automatically set in the transmit direction 1 = E–bits automatically set in the transmit direction
PF	TCR2.0	**Function of RLOS/LOTC Pin.** 0 = Receive Loss of Sync (RLOS) 1 = Loss of Transmit Clock (LOTC)

CCR1: COMMON CONTROL REGISTER 1 (Address=14 Hex)

(MSB)							(LSB)
FLB	THDB3	TG802	TCRC4	RSM	RHDB3	RG802	RCRC4

SYMBOL	POSITION	NAME AND DESCRIPTION
FLB	CCR1.7	**Framer Loopback.** 0 = loopback disabled 1 = loopback enabled
THDB3	CCR1.6	**Transmit HDB3 Enable.** 0 = HDB3 disabled 1 = HDB3 enabled
TG802	CCR1.5	**Transmit G.802 Enable.** See Section 19 for details. 0 = do not force TCHBLK high during bit 1 of timeslot 26 1 = force TCHBLK high during bit 1 of timeslot 26
TCRC4	CCR1.4	**Transmit CRC4 Enable.** 0 = CRC4 disabled 1 = CRC4 enabled
RSM	CCR1.3	**Receive Signaling Mode Select.** 0 = CAS signaling mode 1 = CCS signaling mode
RHDB3	CCR1.2	**Receive HDB3 Enable.** 0 = HDB3 disabled 1 = HDB3 enabled
RG802	CCR1.1	**Receive G.802 Enable.** See Section 19 for details. 0 = do not force RCHBLK high during bit 1 of timeslot 26 1=force RCHBLK high during bit 1 of timeslot 26
RCRC4	CCR1.0	**Receive CRC4 Enable.** 0 = CRC4 disabled 1 = CRC4 enabled

6.2 Framer Loopback

When CCR1.7 is set to a one, the DS21354/554 will enter a Framer LoopBack (FLB) mode. See Figure 3-1 for more details. This loopback is useful in testing and debugging applications. In FLB, the SCT will loop data from the transmit side back to the receive side. When FLB is enabled, the following will occur:

1. Data will be transmitted as normal at TPOSO and TNEGO.
2. Data input via RPOSI and RNEGI will be ignored.
3. The RCLK output will be replaced with the TCLK input.

CCR2: COMMON CONTROL REGISTER 2 (Address=1A Hex)

(MSB)							(LSB)
ECUS	VCRFS	AAIS	ARA	RSERC	LOTCMC	RFF	RFE

SYMBOL	POSITION	NAME AND DESCRIPTION
ECUS	CCR2.7	**Error Counter Update Select.** See Section 8 for details. 0 = update error counters once a second 1 = update error counters every 62.5 ms (500 frames)
VCRFS	CCR2.6	**VCR Function Select.** See Section 8.1 for details. 0 = count BiPolar Violations (BPVs) 1 = count Code Violations (CVs)
AAIS	CCR2.5	**Automatic Transmit AIS Generation.** 0 = disabled 1 = enabled
ARA	CCR2.4	**Automatic Remote Alarm Generation.** 0 = disabled 1 = enabled
RSERC	CCR2.3	**RSER Control.** 0 = allow RSER to output data as received under all conditions 1 = force RSER to one under loss of frame alignment conditions
LOTCMC	CCR2.2	**Loss of Transmit Clock Mux Control.** Determines whether the transmit side formatter should switch to the ever present RCLKO if the TCLK should fail to transition (see Figure 3-1). 0 = do not switch to RCLKO if TCLK stops 1 = switch to RCLKO if TCLK stops
RFF	CCR2.1	**Receive Force Freeze.** Freezes receive side signaling at RSIG (and TS16 in RSER if CCR3.3=1); will override Receive Freeze Enable (RFE). See Section 10.2 for details. 0 = do not force a freeze event 1 = force a freeze event
RFE	CCR2.0	**Receive Freeze Enable.** See Section 10.2 for details. 0 = no freezing of receive signaling data will occur 1 = allow freezing of receive signaling data at RSIG (and TS16 in RSER if CCR3.3 = 1).

6.3 Automatic Alarm Generation

The device can be programmed to automatically transmit AIS or Remote Alarm. When automatic AIS generation is enabled (CCR2.5 = 1), the device monitors the receive side framer to determine if any of the following conditions are present: loss of receive frame synchronization, AIS alarm (all one's) reception, or loss of receive carrier (or signal). If any one (or more) of the above conditions is present, then the framer will either force an AIS alarm.

When automatic RAI generation is enabled (CCR2.4 = 1), the framer monitors the receive side to determine if any of the following conditions are present: loss of receive frame synchronization, AIS alarm (all one's) reception, or loss of receive carrier (or signal) or if CRC4 multiframe synchronization cannot be found within 128ms of FAS synchronization (if CRC4 is enabled). If any one (or more) of the above conditions is present, then the framer will either transmit a RAI alarm.

RAI generation conforms to ETS 300 011 specifications and a constant Remote Alarm will be transmitted if the DS21354/554 cannot find CRC4 multiframe synchronization within 400 ms as per G.706.

CCR3: COMMON CONTROL REGISTER 3 (Address=1B Hex)

(MSB)							(LSB)
TESE	TCBFS	TIRFS	–	RSRE	THSE	TBCS	RCLA

SYMBOL	POSITION	NAME AND DESCRIPTION
TESE	CCR3.7	**Transmit Side Elastic Store Enable.** 0 = elastic store is bypassed 1 = elastic store is enabled
TCBFS	CCR3.6	**Transmit Channel Blocking Registers (TCBR) Function Select.** 0 = TCBRs define the operation of the TCHBLK output pin 1 = TCBRs define which signaling bits are to be inserted
TIRFS	CCR3.5	**Transmit Idle Registers (TIR) Function Select.** See Section 11.1 for details. 0 = TIRs define in which channels to insert idle code 1 = TIRs define in which channels to insert data from RSER (i.e., Per=Channel Loopback function)
-	CCR3.4	**Not Assigned.** Should be set to zero when written to.
RSRE	CCR3.3	**Receive Side Signaling Re–Insertion Enable.** See Section 10.2.1 for details. 0 = do not re–insert signaling bits into the data stream presented at the RSER pin 1 = re–insert the signaling bits into data stream presented at the RSER pin
THSE	CCR3.2	**Transmit Side Hardware Signaling Insertion Enable.** See Section 10.2.2 for details. 0 = do not insert signaling from the TSIG pin into the data stream presented at the TSER pin 1 = insert signaling from the TSIG pin into the data stream presented at the TSER pin
TBCS	CCR3.1	**Transmit Side Backplane Clock Select.** 0 = if TSYSCLK is 1.544 MHz 1 = if TSYSCLK is 2.048/4.096/8.192 MHz
RCLA	CCR3.0	**Receive Carrier Loss (RCL) Alternate Criteria.** 0 = RCL declared upon 255 consecutive zeros (125 us) 1 = RCL declared upon 2048 consecutive zeros (1 ms)

CCR4: COMMON CONTROL REGISTER 4 (Address=A8 Hex)

(MSB)							(LSB)
RLB	LLB	LIAIS	TCM4	TCM3	TCM2	TCM1	TCM0

SYMBOL	POSITION	NAME AND DESCRIPTION
RLB	CCR4.7	**Remote Loopback.** 0 = loopback disabled 1 = loopback enabled

SYMBOL	POSITION	NAME AND DESCRIPTION
LLB	CCR4.6	**Local Loopback.** 0 = loopback disabled 1 = loopback enabled
LIAIS	CCR4.5	**Line Interface AIS Generation Enable.** 0 = allow normal data from TPOSI/TNEGI to be transmitted at TTIP and TRING 1 = force unframed all ones to be transmitted at TTIP and TRING at the MCLK rate
TCM4	CCR4.4	**Transmit Channel Monitor Bit 4.** MSB of a channel decode that determines which transmit channel data will appear in the TDS0M register. See Section 9 for details.
TCM3	CCR4.3	**Transmit Channel Monitor Bit 3.**
TCM2	CCR4.2	**Transmit Channel Monitor Bit 2.**
TCM1	CCR4.1	**Transmit Channel Monitor Bit 1.**
TCM0	CCR4.0	**Transmit Channel Monitor Bit 0. LSB of the channel decode.**

6.4 Remote Loopback

When CCR4.7 is set to a one, the SCT will be forced into Remote LoopBack (RLB). In this loopback, data input via the RPOSI and RNEGI pins will be transmitted back to the TPOSO and TNEGO pins. Data will continue to pass through the receive side framer of the SCT as it would normally and the data from the transmit side formatter will be ignored. Please see Figure 3-1 for more details.

6.5 Local Loopback

When CCR4.6 is set to a one, the SCT will be forced into Local LoopBack (LLB). In this loopback, data will continue to be transmitted as normal through the transmit side of the SCT. Data being received at RTIP and RRING will be replaced with the data being transmitted. Data in this loopback will pass through the jitter attenuator. Please see Figure 3-1 for more details.

CCR5: COMMON CONTROL REGISTER 5 (Address=AA Hex)

(MSB)							(LSB)
LIRST	RESA	TESA	RCM4	RCM3	RCM2	RCM1	RCM0

SYMBOL	POSITION	NAME AND DESCRIPTION
LIRST	CCR5.7	**Line Interface Reset.** Setting this bit from a zero to a one will initiate an internal reset that affects the clock recovery state machine and jitter attenuator. Normally this bit is only toggled on power–up. Must be cleared and set again for a subsequent reset.
RESA	CCR5.6	**Receive Elastic Store Align.** Setting this bit from a zero to a one may force the receive elastic store's write/read pointers to a minim separation of half a frame. No action will be taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less then half a frame, the command will be executed and data will be disrupted.

SYMBOL	POSITION	NAME AND DESCRIPTION
		Should be toggled after RSYSCLK has been applied and is stable. Must be cleared and set again for a subsequent align. See Section 13 for details.
TESA	CCR5.5	**Transmit Elastic Store Align.** Setting this bit from a zero to a one may force the transmit elastic store's write/read pointers to a minim separation of half a frame. No action will be taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less then half a frame, the command will be executed and data will be disrupted. Should be toggled after TSYSCLK has been applied and is stable. Must be cleared and set again for a subsequent align. See Section 13 for details.
RCM4	CCR5.4	**Receive Channel Monitor Bit 4**. MSB of a channel decode that determines which receive channel data will appear in the RDS0M register. See Section 9 for details.
RCM3	CCR5.3	**Receive Channel Monitor Bit 3.**
RCM2	CCR5.2	**Receive Channel Monitor Bit 2.**
RCM1	CCR5.1	**Receive Channel Monitor Bit 1.**
RCM0	CCR5.0	**Receive Channel Monitor Bit 0.** LSB of the channel decode.

CCR6: COMMON CONTROL REGISTER 6 (Address=1D Hex)

(MSB)							(LSB)
LIUODO	CDIG	LIUSI	–	–	TCLKSRC	RESR	TESR

SYMBOL	POSITION	NAME AND DESCRIPTION
LIUODO	CCR6.7	**Line Interface Open Drain Option.** This control bit determines whether the TTIP and TRING outputs will be open drain or not. The line driver outputs can be forced open drain to allow 6Vpeak pulses to be generated or to allow the creation of a very low power interface. 0 = allow TTIP and TRING to operate normally 1 = force the TTIP and TRING outputs to be open drain
CDIG	CCR6.6	**Customer Disconnect Indication Generator.** This control bit determines whether the Line Interface will generate an unframed ...1010... pattern at TTIP and TRING instead of the normal data pattern. 0 = generate normal data at TTIP & TRING as input via TPOSI & TNEGI 1 = generate a ...1010... pattern at TTIP and TRING
LIUSI	CCR6.5	**Line Interface G.703 Synchronization Interface Enable.** This control bit determines whether the line receiver should handle a normal E1 signal (Section 6 of G.703) or a 2.048MHz synchronization signal (Section 10 of G.703). This control has no affect on the line interface transmitter. 0 = line receiver configured to support a normal E1 signal 1 = line receiver configured to support a synchronization signal
–	CCR6.4	**Not Assigned.** Should be set to zero when written.

SYMBOL	POSITION	NAME AND DESCRIPTION
–	CCR6.3	**Not Assigned.** Should be set to zero when written.
TCLKSRC	CCR6.2	**Transmit Clock Source Select.** This function allows the user to internally select RCLK as the clock source for the transmit side formatter. 0 = Source of transmit clock determined by CCR2.2 (LOTCMC) 1 = Force transmitter to internally switch to RCLK as source of transmit clock. Signal at TCLK pin is ignored
RESR	CCR6.1	**Receive Elastic Store Reset.** Setting this bit from a zero to a one will force the receive elastic store to a depth of one frame. Receive data is lost during the reset. Should be toggled after RSYSCLK has been applied and is stable. Must be cleared and set again for a subsequent reset.
TESR	CCR6.0	**Transmit Elastic Store Reset.** Setting this bit from a zero to a one will force the transmit elastic store to a depth of one frame. Transmit data is lost during the reset. Should be toggled after TSYSCLK has been applied and is stable. Must be cleared and set again for a subsequent reset.

7 STATUS AND INFORMATION REGISTERS

There is a set of seven registers that contain information on the current real time status of a framer in the DS21354/554, Status Register 1 (SR1), Status Register 2 (SR2), Receive Information Register (RIR), Synchronizer status Register (SSR) and a set of three registers for the onboard HDLC controller. The specific details on the four registers pertaining to the HDLC controller are covered in Section 15 but they operate the same as the other status registers in the device and this operation is described below.

When a particular event has occurred (or is occurring), the appropriate bit in one of these four registers will be set to a one. All of the bits in SR1, SR2, and RIR1 registers operate in a latched fashion. The Synchronizer Status Register contents are not latched. This means that if an event or an alarm occurs and a bit is set to a one in any of the registers, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again (or in the case of the RUA1, RRA, RCL, and RLOS alarms, the bit will remain set if the alarm is still present).

The user will always proceed a read of any of the SR1, SR2 and RIR registers with a write. The byte written to the register will inform the framer which bits the user wishes to read and have cleared. The user will write a byte to one of these registers, with a one in the bit positions he or she wishes to read and a zero in the bit positions he or she does not wish to obtain the latest information on. When a one is written to a bit location, the read register will be updated with the latest information. When a zero is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that bit does indeed clear. This second write step is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. This write–read– write scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS21354/554 with higher–order software languages.

The SSR register operates differently than the other three. It is a read only register and it reports the status of the synchronizer in real time. This register is not latched and it is not necessary to precede a read of this register with a write.

The SR1, SR2, and HSR registers have the unique ability to initiate a hardware interrupt via the INT* output pin. Each of the alarms and events in the SR1, SR2, and HSR can be either masked or unmasked from the interrupt pin via the Interrupt Mask Register 1 (IMR1), Interrupt Mask Register 2 (IMR2), and HDLC Interrupt Mask Register (HIMR) respectively. The HIMR register is covered in Section 15.

The interrupts caused by alarms in SR1 (namely RUA1, RRA, RCL, and RLOS) act differently than the interrupts caused by events in SR1 and SR2 (namely RSA1, RDMA, RSA0, RSLIP, RMF, TMF, SEC, TAF, LOTC, RCMF, and TSLIP). The alarm caused interrupts will force the INT* pin low whenever the alarm changes state (i.e., the alarm goes active or inactive according to the set/clear criteria in Table 7-1). The INT* pin will be allowed to return high (if no other interrupts are present) when the user reads the alarm bit that caused the interrupt to occur even if the alarm is still present.

The event caused interrupts will force the INT* pin low when the event occurs. The INT* pin will be allowed to return high (if no other interrupts are present) when the user reads the event bit that caused the interrupt to occur.

RIR: RECEIVE INFORMATION REGISTER (Address=08 Hex)

(MSB)							(LSB)
TESF	TESE	JALT	RESF	RESE	CRCRC	FASRC	CASRC

SYMBOL	POSITION	NAME AND DESCRIPTION
TESF	RIR.7	**Transmit Side Elastic Store Full.** Set when the transmit side elastic store buffer fills and a frame is deleted.
TESE	RIR.6	**Transmit Side Elastic Store Empty.** Set when the transmit side elastic store buffer empties and a frame is repeated.
JALT	RIR.5	**Jitter Attenuator Limit Trip.** Set when the jitter attenuator FIFO reaches to within 4–bits of its limit; useful for debugging jitter attenuation operation.
RESF	RIR.4	**Receive Side Elastic Store Full.** Set when the receive side elastic store buffer fills and a frame is deleted.
RESE	RIR.3	**Receive Side Elastic Store Empty.** Set when the receive side elastic store buffer empties and a frame is repeated.
CRCRC	RIR.2	**CRC Resync Criteria Met.** Set when 915/1000 code words are received in error.
FASRC	RIR.1	**FAS Resync Criteria Met.** Set when 3 consecutive FAS words are received in error.
CASRC	RIR.0	**CAS Resync Criteria Met.** Set when 2 consecutive CAS MF alignment words are received in error.

SSR: SYNCHRONIZER STATUS REGISTER (Address=1E Hex)

(MSB)							(LSB)
CSC5	CSC4	CSC3	CSC2	CSC0	FASSA	CASSA	CRC4SA

SYMBOL	POSITION	NAME AND DESCRIPTION
CSC5	SSR.7	**CRC4 Sync Counter Bit 5.** MSB of the 6–bit counter.
CSC4	SSR.6	**CRC4 Sync Counter Bit 4.**
CSC3	SSR.5	**CRC4 Sync Counter Bit 3.**
CSC2	SSR.4	**CRC4 Sync Counter Bit 2.**
CSC0	SSR.3	**CRC4 Sync Counter Bit 0.** LSB of the 6–bit counter. The next to LSB is not accessible.
FASSA	SSR.2	**FAS Sync Active.** Set while the synchronizer is searching for alignment at the FAS level.
CASSA	SSR.1	**CAS MF Sync Active.** Set while the synchronizer is searching for the CAS MF alignment word.
CRC4SA	SSR.0	**CRC4 MF Sync Active.** Set while the synchronizer is searching for the CRC4 MF alignment word.

7.1 CRC4 Sync Counter

The CRC4 Sync Counter increments each time the 8 ms CRC4 multiframe search times out. The counter is cleared when the framer has successfully obtained synchronization at the CRC4 level. The counter can also be cleared by disabling the CRC4 mode (CCR1.0=0). This counter is useful for determining the amount of time the framer has been searching for synchronization at the CRC4 level. ITU G.706 suggests that if synchronization at the CRC4 level cannot be obtained within 400 ms, then the search should be abandoned and proper action taken. The CRC4 Sync Counter will rollover.

SR1: STATUS REGISTER 1 (Address=06 Hex)

(MSB)							(LSB)
RSA1	RDMA	RSA0	RSLIP	RUA1	RRA	RCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
RSA1	SR1.7	**Receive Signaling All Ones / Signaling Change.** Set when the contents of timeslot 16 contains less than three zeros over 16 consecutive frames. This alarm is not disabled in the CCS signaling mode. Both RSA1 and RSA0 will be set if a change in signaling is detected.
RDMA	SR1.6	**Receive Distant MF Alarm.** Set when bit–6 of timeslot 16 in frame 0 has been set for two consecutive multiframes. This alarm is not disabled in the CCS signaling mode.
RSA0	SR1.5	**Receive Signaling All Zeros / Signaling Change.** Set when over a full MF, timeslot 16 contains all zeros. Both RSA1 and RSA0 will be set if a change in signaling is detected.
RSLIP	SR1.4	**Receive Side Elastic Store Slip.** Set when the elastic store has either repeated or deleted a frame of data.
RUA1	SR1.3	Receive Unframed All Ones. Set when an unframed all ones code is received at RPOSI and RNEGI.
RRA	SR1.2	**Receive Remote Alarm.** Set when a remote alarm is received at RPOSI and RNEGI.

SYMBOL	POSITION	NAME AND DESCRIPTION
RCL	SR1.1	**Receive Carrier Loss.** Set when 255 (or 2048 if CCR3.0=1) consecutive zeros have been detected at RTIP and RRING. (note: a receiver carrier loss based on data received at RPOSI and RNEGI is available in the HSR register)
RLOS	SR1.0	**Receive Loss of Sync.** Set when the device is not synchronized to the receive E1 stream.

ALARM CRITERIA Table 7-1

ALARM	SET CRITERIA	CLEAR CRITERIA	ITU SPEC.
RSA1 (receive signaling all ones)	over 16 consecutive frames (one full MF) timeslot 16 contains less than three zeros	over 16 consecutive frames (one full MF) timeslot 16 contains three or more zeros	G.732 4.2
RSA0 (receive signaling all zeros)	over 16 consecutive frames (one full MF) timeslot 16 contains all zeros	over 16 consecutive frames (one full MF) timeslot 16 contains at least a single one	G.732 5.2
RDMA (receive distant multiframe alarm)	bit 6 in timeslot 16 of frame 0 set to one for two consecutive MF	bit 6 in timeslot 16 of frame 0 set to zero for two consecutive MF	O.162 2.1.5
RUA1 (receive unframed all ones)	less than three zeros in two frames (512–bits)	more than two zeros in two frames (512–bits)	O.162 1.6.1.2
RRA (receive remote alarm)	bit 3 of non–align frame set to one for three consecutive occasions	bit 3 of non–align frame set to zero for three consecutive occasions	O.162 2.1.4
RCL (receive carrier loss)	255 (or 2048) consecutive zeros received	in 255–bit times, at least 32 ones are received	G.775 / G.962

SR2: STATUS REGISTER 2 (Address=07 Hex)

(MSB)							(LSB)
RMF	RAF	TMF	SEC	TAF	LOTC	RCMF	TSLIP

SYMBOL	POSITION	NAME AND DESCRIPTION
RMF	SR2.7	**Receive CAS Multiframe.** Set every 2 ms (regardless if CAS signaling is enabled or not) on receive multiframe boundaries. Used to alert the host that signaling data is available.
RAF	SR2.6	**Receive Align Frame.** Set every 250 ns at the beginning of align frames. Used to alert the host that Si and Sa bits are available in the RAF and RNAF registers.
TMF	SR2.5	**Transmit Multiframe.** Set every 2 ms (regardless if CRC4 is enabled) on transmit multiframe boundaries. Used to alert the host that signaling data needs to be updated.
SEC	SR2.4	**One Second Timer.** Set on increments of one second based on RCLK. If CCR2.7=1, then this bit will be set every 62.5 ms instead of once a second.

SYMBOL	POSITION	NAME AND DESCRIPTION
TAF	SR2.3	**Transmit Align Frame.** Set every 250 ns at the beginning of align frames. Used to alert the host that the TAF and TNAF registers need to be updated.
LOTC	SR2.2	**Loss of Transmit Clock.** Set when the TCLK pin has not transitioned for one channel time (or 3.9 ns). Will force the LOTC pin high if enabled via TCR2.0.
RCMF	SR2.1	**Receive CRC4 Multiframe.** Set on CRC4 multiframe boundaries; will continue to be set every 2 ms on an arbitrary boundary if CRC4 is disabled.
TSLIP	SR2.0	**Transmit Elastic Store Slip.** Set when the elastic store has either repeated or deleted a frame of data.

IMR1: INTERRUPT MASK REGISTER 1 (Address=16 Hex)

(MSB)							(LSB)
RSA1	RDMA	RSA0	RSLIP	RUA1	RRA	RCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
RSA1	IMR1.7	**Receive Signaling All Ones / Signaling Change.** 0 = interrupt masked 1 = interrupt enabled
RDMA	IMR1.6	**Receive Distant MF Alarm.** 0 = interrupt masked 1 = interrupt enabled
RSA0	IMR1.5	**Receive Signaling All Zeros / Signaling Change.** 0 = interrupt masked 1 = interrupt enabled
RSLIP	IMR1.4	**Receive Elastic Store Slip Occurrence.** 0 = interrupt masked 1 = interrupt enabled
RUA1	IMR1.3	**Receive Unframed All Ones.** 0 = interrupt masked 1 = interrupt enabled
RRA	IMR1.2	**Receive Remote Alarm.** 0 = interrupt masked 1 = interrupt enabled
RCL	IMR1.1	**Receive Carrier Loss.** 0 = interrupt masked 1 = interrupt enabled
RLOS	IMR1.0	**Receive Loss of Sync.** 0 = interrupt masked 1 = interrupt enabled

IMR2: INTERRUPT MASK REGISTER 2 (Address=17 Hex)

(MSB)							(LSB)
RMF	RAF	TMF	SEC	TAF	LOTC	RCMF	TSLIP

SYMBOL	POSITION	NAME AND DESCRIPTION
RMF	IMR2.7	**Receive CAS Multiframe.** 0 = interrupt masked 1 = interrupt enabled
RAF	IMR2.6	**Receive Align Frame.** 0 = interrupt masked 1 = interrupt enabled
TMF	IMR2.5	**Transmit Multiframe.** 0 = interrupt masked 1 = interrupt enabled
SEC	IMR2.4	**One Second Timer.** 0 = interrupt masked 1 = interrupt enabled
TAF	IMR2.3	**Transmit Align Frame.** 0 = interrupt masked 1 = interrupt enabled
LOTC	IMR2.2	**Loss Of Transmit Clock.** 0 = interrupt masked 1 = interrupt enabled
RCMF	IMR2.1	**Receive CRC4 Multiframe.** 0 = interrupt masked 1 = interrupt enabled
TSLIP	IMR2.0	**Transmit Side Elastic Store Slip Occurrence.** 0 = interrupt masked 1 = interrupt enabled

8 ERROR COUNT REGISTERS

There are a set of four counters in the DS21354/554 that record bipolar or code violations, errors in the CRC4 SMF code words, E bits as reported by the far end, and word errors in the FAS. Each of these four counters are automatically updated on either one second boundaries (CCR2.7 = 0) or every 62.5 ms (CCR2.7 = 1) as determined by the timer in Status Register 2 (SR2.4). Hence, these registers contain performance data from either the previous second or the previous 62.5 ms. The user can use the interrupt from the one second timer to determine when to read these registers. The user has a full second (or 62.5 ms) to read the counters before the data is lost. All four counters will saturate at their respective maximum counts and they will not rollover.

8.1 BPV or Code Violation Counter

Violation Count Register 1 (VCR1) is the most significant word and VCR2 is the least significant word of a 16–bit counter that records either BiPolar Violations (BPVs) or Code Violations (CVs). If CCR2.6 = 0, then the VCR counts bipolar violations. Bipolar violations are defined as consecutive marks of the same polarity. In this mode, if the HDB3 mode is set for the receive side via CCR1.2, then HDB3 code words are not counted as BPVs. If CCR2.6 = 1, then the VCR counts code violations as defined in ITU O.161. Code violations are defined as consecutive bipolar violations of the same polarity.

In most applications, the framer should be programmed to count BPVs when receiving AMI code and to count CVs when receiving HDB3 code. This counter increments at all times and is not disabled by loss of sync conditions. The counter saturates at 65,535 and will not rollover. The bit error rate on an E1 line would have to be greater than 10**–2 before the VCR would saturate.

VCR1: UPPER BIPOLAR VIOLATION COUNT REGISTER 1 (Address=00 Hex)
VCR2: LOWER BIPOLAR VIOLATION COUNT REGISTER 2 (Address=01 Hex)

(MSB)							(LSB)	
V15	V14	V13	V12	V11	V10	V9	V8	VCR1
V7	V6	V5	V4	V3	V2	V1	V0	VCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
V15	VCR1.7	**MSB of the 16–bit code violation count**
V0	VCR2.0	**LSB of the 16–bit code violation count**

8.2 CRC4 Error Counter

CRC4 Count Register 1 (CRCCR1) is the most significant word and CRCCR2 is the least significant word of a 10–bit counter that records word errors in the Cyclic Redundancy Check 4 (CRC4). Since the maximum CRC4 count in a one second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of multiframe sync occurs at the CAS level.

CRCCR1: CRC4 COUNT REGISTER 1 (Address=02 Hex)
CRCCR2: CRC4 COUNT REGISTER 2 (Address=03 Hex)

(MSB)							(LSB)	
(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	CRC9	CRC8	CRCCR1
CRC7	CRC6	CRC5	CRC4	CRC/3	CRC2	CRC1	CRC0	CRCCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
CRC9	CRCCR1.1	**MSB of the 10–Bit CRC4 error count**
CRC0	CRCCR2.0	**LSB of the 10–Bit CRC4 error count**

NOTE:

The upper six bits of CRCCR1 at address 02 are the most significant bits of the 12–bit FAS error counter.

8.3 E–Bit Counter

E–bit Count Register 1 (EBCR1) is the most significant word and EBCR2 is the least significant word of a 10–bit counter that records Far End Block Errors (FEBE) as reported in the first bit of frames 13 and 15 on E1 lines running with CRC4 multiframe. These count registers will increment once each time the received E–bit is set to zero. Since the maximum E–bit count in a one second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of multiframe sync occurs at the CAS level.

EBCR1: E–BIT COUNT REGISTER 1 (Address=04 Hex)
EBCR2: E–BIT COUNT REGISTER 2 (Address=05 Hex)

(MSB)							(LSB)	
(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	EB9	EB8	EBCR1
EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0	EBCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
EB9	EBCR1.1	**MSB of the 10–Bit E–Bit Error Count**
EB0	EBCR2.0	**LSB of the 10–Bit E–Bit Error Count**

NOTE:
The upper six bits of EBCR1 at address 04 are the least significant bits of the 12–bit FAS error counter.

8.4 FAS Error Counter
FAS Count Register 1 (FASCR1) is the most significant word and FASCR2 is the least significant word of a 12–bit counter that records word errors in the Frame Alignment Signal in timeslot 0. This counter is disabled when RLOS is high. FAS errors will not be counted when the framer is searching for FAS alignment and/or synchronization at either the CAS or CRC4 multiframe level. Since the maximum FAS word error count in a one second period is 4000, this counter cannot saturate.

FASCR1: FAS ERROR COUNT REGISTER 1 (Address=02 Hex)
FASCR2: FAS ERROR COUNT REGISTER 2 (Address=04 Hex)

(MSB)							(LSB)	
FAS11	FAS10	FAS9	FAS8	FAS7	FAS6	(note 2)	(note 2)	FASCR1
FAS5	FAS4	FAS3	FAS2	FAS1	FAS0	(note 1)	(note 1)	FASCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
FAS11	FASCR1.7	**MSB of the 12–Bit FAS Error Count**
FAS0	FASCR2.2	**LSB of the 12–Bit FAS Error Count**

NOTES:
1. The lower two bits of FASCR1 at address 02 are the most significant bits of the 10–bit CRC4 error counter.
2. The lower two bits of FASCR2 at address 04 are the most significant bits of the 10–bit E–Bit counter.

9 DS0 MONITORING FUNCTION
Each framer in the DS21354/554 has the ability to monitor one DS0 (64kbps) channel in the transmit direction and one DS0 channel in the receive direction at the same time. In the transmit direction the user will determine which channel is to be monitored by properly setting the TCM0 to TCM4 bits in the CCR4 register. In the receive direction, the RCM0 to RCM4 bits in the CCR5 register need to be properly set. The DS0 channel pointed to by the TCM0 to TCM4 bits will appear in the Transmit DS0 Monitor (TDS0M) register and the DS0 channel pointed to by the RCM0 to RCM4 bits will appear in the Receive DS0 (RDS0M) register. The TCM4 to TCM0 and RCM4 to RCM0 bits should be programmed with the decimal decode of the appropriate E1 channel.

For example, if DS0 channel 6 in the transmit direction and DS0 channel 15 in the receive direction needed to be monitored, then the following values would be programmed into CCR5 and CCR6:

TCM4 = 0 RCM4 = 0
TCM3 = 0 RCM3 = 1
TCM2 = 1 RCM2 = 1
TCM1 = 0 RCM1 = 1
TCM0 = 1 RCM0 = 0

CCR4: COMMON CONTROL REGISTER 4 (Address=A8 Hex)

[Repeated here from section 6 for convenience]

(MSB)							(LSB)
RLB	LLB	LIAIS	TCM4	TCM3	TCM2	TCM1	TCM0

SYMBOL	POSITION	NAME AND DESCRIPTION
RLB	CCR4.7	**Remote Loopback.**
LLB	CCR4.6	**Local Loopback.**
LIAIS	CCR4.5	**Line Interface AIS Generation Enable.**
TCM4	CCR4.4	**Transmit Channel Monitor Bit 4.** MSB of a channel decode that determines which transmit channel data will appear in the TDS0M register. See Section 9 for details.
TCM3	CCR4.3	**Transmit Channel Monitor Bit 3.**
TCM2	CCR4.2	**Transmit Channel Monitor Bit 2.**
TCM1	CCR4.1	**Transmit Channel Monitor Bit 1.**
TCM0	CCR4.0	**Transmit Channel Monitor Bit 0.** LSB of the channel decode.

TDS0M: TRANSMIT DS0 MONITOR REGISTER (Address=A9 Hex)

(MSB)							(LSB)
B1	B2	B3	B4	B5	B6	B7	B8

SYMBOL	POSITION	NAME AND DESCRIPTION
B1	TDS0M.7	**Transmit DS0 Channel Bit 1.** MSB of the DS0 channel (first bit to be transmitted).
B2	TDS0M.6	**Transmit DS0 Channel Bit 2.**
B3	TDS0M.5	**Transmit DS0 Channel Bit 3.**
B4	TDS0M.4	**Transmit DS0 Channel Bit 4.**
B5	TDS0M.3	**Transmit DS0 Channel Bit 5.**
B6	TDS0M.2	**Transmit DS0 Channel Bit 6.**
B7	TDS0M.1	Transmit DS0 Channel Bit 7.
B8	TDS0M.0	**Transmit DS0 Channel Bit 8.** LSB of the DS0 channel (last bit to be transmitted).

CCR5: COMMON CONTROL REGISTER 5 (Address=AA Hex)

[Repeated here from section 6 for convenience]

(MSB)							(LSB)
LIRST	RESALGN	TESALGN	RCM4	RCM3	RCM2	RCM1	RCM0

SYMBOL	POSITION	NAME AND DESCRIPTION
LIRST	CCR5.7	**Line Interface Reset.**
RESALGN	CCR5.6	**Receive Elastic Store Align.**
TESALGN	CCR5.5	**Transmit Elastic Store Align.**
RCM4	CCR5.4	**Receive Channel Monitor Bit 4.** MSB of a channel decode that determines which receive channel data will appear in the RDS0M register. See Section 9 for details.
RCM3	CCR5.3	**Receive Channel Monitor Bit 3.**
RCM2	CCR5.2	**Receive Channel Monitor Bit 2.**
RCM1	CCR5.1	**Receive Channel Monitor Bit 1.**
RCM0	CCR5.0	**Receive Channel Monitor Bit 0.** LSB of the channel decode.

RDS0M: RECEIVE DS0 MONITOR REGISTER (Address=AB Hex)

(MSB)							(LSB)
B1	B2	B3	B4	B5	B6	B7	B8

SYMBOL	POSITION	NAME AND DESCRIPTION
B1	RDS0M.7	**Receive DS0 Channel Bit 1.** MSB of the DS0 channel (first bit received).
B2	RDS0M.6	**Receive DS0 Channel Bit 2.**
B3	RDS0M.5	**Receive DS0 Channel Bit 3.**
B4	RDS0M.4	**Receive DS0 Channel Bit 4.**
B5	RDS0M.3	**Receive DS0 Channel Bit 5.**
B6	RDS0M.2	**Receive DS0 Channel Bit 6.**
B7	RDS0M.1	**Receive DS0 Channel Bit 7.**
B8	RDS0M.0	**Receive DS0 Channel Bit 8.** LSB of the DS0 channel (last bit received).

10 SIGNALING OPERATION

The DS21354/554 contains provisions for both processor based (i.e., software based) signaling bit access and for hardware based access. Both the processor based access and the hardware based access can be used simultaneously if necessary. The processor based signaling is covered in Section 10.1 and the hardware based signaling is covered in Section 10.2. When referring to signaling, the Voice Channel numbering scheme is used.

10.1 Processor Based Signaling

The Channel Associated Signaling (CAS) bits embedded in the E1 stream can be extracted from the receive stream and inserted into the transmit stream by the framer. Each of the 30 voice channels has four signaling bits (A/B/C/D) associated with it. The numbers in parenthesis () are the voice channel associated with a particular signaling bit. The voice channel numbers have been assigned as described in the ITU documents. Please note that this is different than the channel numbering scheme (1 to 32) that is used in the rest of the data sheet.

For example, voice channel 1 is associated with timeslot 1 (Channel 2) and voice channel 30 is associated with timeslot 31 (Channel 32). There is a set of 16 registers for the receive side (RS1 to RS16) and 16 registers on the transmit side (TS1 to TS16). The signaling registers are detailed below.

RS1 TO RS16: RECEIVE SIGNALING REGISTERS (Address=30 to 3F Hex)

(MSB)							(LSB)	
0	0	0	0	X	Y	X	X	RS1 (30)
A(1)	B(1)	C(1)	D(1)	A(16)	B(16)	C(16)	D(16)	RS2 (31)
A(2)	B(2)	C(2)	D(2)	A(17)	B(17)	C(17)	D(17)	RS3 (32)
A(3)	B(3)	C(3)	D(3)	A(18)	B(18)	C(18)	D(18)	RS3 (33)
A(4)	B(4)	C(4)	D(4)	A(19)	B(19)	C(19)	D(19)	RS5 (34)
A(5)	B(5)	C(5)	D(5)	A(20)	B(20)	C(20)	D(20)	RS6 (35)
A(6)	B(6)	C(6)	D(6)	A(21)	B(21)	C(21)	D(21)	RS7 (36)
A(7)	B(7)	B(7)	B(7)	B(22)	B(22)	B(22)	B(22)	RS8 (37)
A(8)	B(8)	C(8)	D(8)	A(23)	B(23)	C(23)	D(23)	RS9 (38)
A(9)	B(9)	C(9)	D(9)	A(24)	B(24)	C(24)	D(24)	RS10 (39)
A(10)	B(10)	C(10)	D(10)	A(25)	B(25)	C(25)	D(25)	RS11 (3A)
A(11)	B(11)	C(11)	D(11)	A(26)	B(26)	C(26)	D(26)	RS12 (3B)
A(12)	B(12)	C(12)	D(12)	A(27)	B(27)	C(27)	D(27)	RS13 (3C)
A(13)	B(13)	C(13)	D(13)	A(28)	B(28)	C(28)	D(28)	RS14 (3D)
A(14)	B(14)	C(14)	D(14)	A(29)	B(29)	C(29)	D(29)	RS15 (3E)
A(15)	B(15)	C(15)	D(15)	A(30)	B(30)	C(30)	D(30)	RS16 (3F)

SYMBOL	POSITION	NAME AND DESCRIPTION
X	RS1.0/1/3	Spare Bits.
Y	RS1.2	Remote Alarm Bit (integrated and reported in SR1.6).
A(1)	RS2.7 1.	Signaling Bit A for Channel 1
D(30)	RS16.0	Signaling Bit D for Channel 30.

Each Receive Signaling Register (RS1 to RS16) reports the incoming signaling from two timeslots. The bits in the Receive Signaling Registers are updated on multiframe boundaries so the user can utilize the Receive Multiframe Interrupt in the Receive Status Register 2 (SR2.7) to know when to retrieve the signaling bits. The user has a full 2 ms to retrieve the signaling bits before the data is lost. The RS registers are updated under all conditions. Their validity should be qualified by checking for synchronization at the CAS level. In CCS signaling mode, RS1 to RS16 can also be used to extract signaling information. Via the SR2.7 bit, the user will be informed when the signaling registers have been loaded with data. The user has 2 ms to retrieve the data before it is lost. The signaling data reported in RS1 to RS16 is also available at the RSIG and RSER pins.

A change in the signaling bits from one multiframe to the next will cause the RSA1 (SR1.7) and RSA0 (SR1.5) status bits to be set at the same time. The user can enable the INT* pin to toggle low upon detection of a change in signaling by setting either the IMR1.7 or IMR1.5 bit. Once a signaling change has been detected, the user has at least 1.75 ms to read the data out of the RS1 to RS16 registers before the data will be lost.

TS1 TO TS16: TRANSMIT SIGNALING REGISTERS (Address=40 to 4F Hex)

(MSB)							(LSB)	
0	0	0	0	X	Y	X	X	TS1 (40)
A(1)	B(1)	C(1)	D(1)	A(16)	B(16)	C(16)	D(16)	TS2 (41)
A(2)	B(2)	C(2)	D(2)	A(17)	B(17)	C(17)	D(17)	TS3 (42)
A(3)	B(3)	C(3)	D(3)	A(18)	B(18)	C(18)	D(18)	TS4 (43)
A(4)	B(4)	C(4)	D(4)	A(19)	B(19)	C(19)	D(19)	TS5 (44)
A(5)	B(5)	C(5)	D(5)	A(20)	B(20)	C(20)	D(20)	TS6 (45)
A(6)	B(6)	C(6)	D(6)	A(21)	B(21)	C(21)	D(21)	TS7 (46)
A(7)	B(7)	B(7)	B(7)	B(22)	B(22)	B(22)	B(22)	TS8 (47)
A(8)	B(8)	C(8)	D(8)	A(23)	B(23)	C(23)	D(23)	TS9 (48)
A(9)	B(9)	C(9)	D(9)	A(24)	B(24)	C(24)	D(24)	TS10 (49)
A(10)	B(10)	C(10)	D(10)	A(25)	B(25)	C(25)	D(25)	TS11 (4A)
A(11)	B(11)	C(11)	D(11)	A(26)	B(26)	C(26)	D(26)	TS12 (4B)
A(12)	B(12)	C(12)	D(12)	A(27)	B(27)	C(27)	D(27)	TS13 (4C)
A(13)	B(13)	C(13)	D(13)	A(28)	B(28)	C(28)	D(28)	TS14 (4D)
A(14)	B(14)	C(14)	D(14)	A(29)	B(29)	C(29)	D(29)	TS15 (4E)
A(15)	B(15)	C(15)	D(15)	A(30)	B(30)	C(30)	D(30)	TS16 (4F)

SYMBOL	POSITION	NAME AND DESCRIPTION
X	TS1.0/1/3	Spare Bits.
Y	TS1.2	Remote Alarm Bit (integrated and reported in SR1.6).
A(1)	TS2.7 1.	Signaling Bit A for Channel 1
D(30)	TS16.0	Signaling Bit D for Channel 30.

Each Transmit Signaling Register (TS1 to TS16) contains the CAS bits for two timeslots that will be inserted into the outgoing stream if enabled to do so via TCR1.5. On multiframe boundaries, the framer will load the values present in the Transmit Signaling Register into an outgoing signaling shift register that is internal to the device. The user can utilize the Transmit Multiframe bit in Status Register 2 (SR2.5) to know when to update the signaling bits. The bit will be set every 2 ms and the user has 2 ms to update the TSR's before the old data will be retransmitted. ITU specifications recommend that the ABCD signaling not be set to all zeros because they will emulate a CAS multiframe alignment word.

The TS1 register is special because it contains the CAS multiframe alignment word in its upper nibble. The upper nibble must always be set to 0000 or else the terminal at the far end will lose multiframe synchronization. If the user wishes to transmit a multiframe alarm to the far end, then the TS1.2 bit should be set to a one. If no alarm is to be transmitted, then the TS1.2 bit should be cleared. The three remaining bits in TS1 are the spare bits. If they are not used, they should be set to one. In CCS signaling mode, TS1 to TS16 can also be used to insert signaling information. Via the SR2.5 bit, the user will be informed when the signaling registers need to be loaded with data. The user has 2 ms to load the data before the old data will be retransmitted.

Via the CCR3.6 bit, the user has the option to use the Transmit Channel Blocking Registers (TCBRs) to determine on a channel by channel basis, which signaling bits are to be inserted via the TSRs (the corresponding bit in the TCBRs = 1) and which are to be sourced from the TSER or TSIG pin (the corresponding bit in the TCBRs = 0). See Figure 19-15 for more details.

10.2 Hardware Based Signaling

10.2.1 Receive Side

In the receive side of the hardware based signaling, there are two operating modes for the signaling buffer; signaling extraction and signaling re–insertion. Signaling extraction involves pulling the signaling bits from the receive data stream and buffering them over a four multiframe buffer and outputting them in a serial PCM fashion on a channel–by–channel basis at the RSIG output. This mode is always enabled. In this mode, the receive elastic store may be enabled or disabled. If the receive elastic store is enabled, then the backplane clock (RSYSCLK) must be 2.048/4.096/8.192 MHz. The ABCD signaling bits are output on RSIG in the lower nibble of each channel. The RSIG data is updated once a multiframe (2 ms) unless a freeze is in effect. See the timing diagrams in Section 19.1 for some examples.

The other hardware based signaling operating mode called signaling re–insertion can be invoked by setting the RSRE control bit high (CCR3.3 = 1). In this mode, the user will provide a multiframe sync at the RSYNC pin and the signaling data be re–aligned at the RSER output according to this applied multiframe boundary. in this mode, the elastic store must be enabled the backplane clock must be 2.048/4.096/8.192 MHz.

The signaling data in the two multiframe buffer will be frozen in a known good state upon either a loss of synchronization (OOF event), carrier loss, or frame slip. To allow this freeze action to occur, the RFE control bit (CCR2.0) should be set high. The user can force a freeze by setting the RFF control bit (CCR2.1) high. Setting the RFF bit high causes the same freezing action as if a loss of synchronization, carrier loss, or slip has occurred.

The 2 multiframe buffer provides an approximate 1 multiframe delay in the signaling bits provided at the RSIG pin (and at the RSER pin if RSRE = 1 via CCR3.3). When freezing is enabled (RFE = 1), the signaling data will be held in the last known good state until the corrupting error condition subsides. When the error condition sub-sides, the signaling data will be held in the old state for an additional 3 ms to 5 ms before being allowed to be updated with new signaling data.

10.2.2 Transmit Side

Via the THSE control bit (CCR3.2), the DS21354/554 can be set up to take the signaling data presented at the TSIG pin and insert the signaling data into the PCM data stream that is being input at the TSER pin. The hardware signaling insertion capabilities of each framer are available whether the transmit side elastic store is enabled or disabled. If the transmit side elastic store is enabled, the backplane clock (TSYSCLK) must be 2.048/4.096/8.192 MHz.

When hardware signaling insertion is enabled on a framer (THSE = 1), then the user must enable the Transmit Channel Blocking Register Function Select (TCBFS) control bit (CCR3.6 = 1). This is needed so that the CAS multiframe alignment word, multiframe remote alarm, and spare bits can be added to timeslot 16 in frame 0 of the multiframe. The TS1 register should be programmed with the proper information. If CCR3.6 = 1, then a zero in the TCBRs implies that signaling data is to be sourced from TSER (or TSIG if CCR3.2 = 1) and a one implies that signaling data for that channel is to be sourced from the Transmit Signaling (TS) registers. See definition below.

TCBR1/TCBR2/TCBR3/TCBR4: DEFINITION WHEN CCR3.6=1

(MSB)							(LSB)	
CH18	CH3	CH17	CH2	CH16	CH1	1*	1*	TCBR1(22)
CH22	CH7	CH21	CH6	CH20	CH5	CH19	CH4	TCBR2(23)
CH26	CH11	CH25	CH10	CH24	CH9	CH23	CH8	TCBR3(24)
CH30	CH15	CH29	CH14	CH28	CH13	CH27	CH12	TCBR4(25)

* these bits should be set to one to allow the internal TS1 register to create the CAS Multiframe Alignment Word and Spare/Remote Alarm bits.

The user can also take advantage of this functionality to intermix signaling data from the TSIG pin and from the internal Transmit Signaling Registers (TS1 to TS16). As an example, assume that the user wishes to source all the signaling data except for voice channels 5 and 10 from the TSIG pin. In this application, the following bits and registers would be programmed as follows:

CONTROL BITS	REGISTER VALUES
THSE = 1 (CCR3.2)	TS1 = 0Bh (MF alignment word, remote alarm etc.)
TCBFS = 1 (CCR3.6)	TCBR1 = 03h (source timeslot 16, frame 1 data)
T16S = 0 (TCR1.5)	TCBR2 = 01h (source voice Channel 5 signaling data from TS6)
	CBR3 = 04h (source voice Channel 10 signaling data from TS11)
	TCBR4 = 00h

11 PER–CHANNEL CODE GENERATION AND LOOPBACK

The DS21354/554 can replace data on a channel–by–channel basis in both the transmit and receive directions. The transmit direction is from the backplane to the E1 line and is covered in Section 11.1. The receive direction is from the E1 line to the backplane and is covered in Section 11.2.

11.1 Transmit Side Code Generation

In the transmit direction there are two methods by which channel data from the backplane can be overwritten with data generated by the framer. The first method which is covered in Section 11.1.1 was a feature contained in the original DS2153 while the second method which is covered in 11.1.2 is a new feature of the DS2154/354/554.

11.1.1 Simple Idle Code Insertion and Per–Channel Loopback

The first method involves using the Transmit Idle Registers (TIR1/2/3/4) to determine which of the 32 E1 channels should be overwritten with the code placed in the Transmit Idle Definition Register (TIDR). This method allows the same 8–bit code to be placed into any of the 32 E1 channels. If this method is used, then the CCR3.5 control bit must be set to zero.

Each of the bit position in the Transmit Idle Registers (TIR1/TIR2/TIR3/TIR4) represent a DS0 channel in the outgoing frame. When these bits are set to a one, the corresponding channel will transmit the Idle Code contained in the Transmit Idle Definition Register (TIDR).

The Transmit Idle Registers (TIRs) have an alternate function that allow them to define a Per–Channel LoopBack (PCLB). If the TIRFS control bit (CCR3.5) is set to one, then the TIRs will determine which channels (if any) from the backplane should be replaced with the data from the receive side or in other words, off of the E1 line. If this mode is enabled, then transmit and receive clocks and frame syncs must be synchronized.

One method to accomplish this would be to tie RCLK to TCLK and RFSYNC to TSYNC. There are no restrictions on which channels can be looped back or on how many channels can be looped back.

TIR1/TIR2/TIR3: TRANSMIT IDLE REGISTERS (Address=26 to 29 Hex)

[Also used for Per–Channel Loopback]

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1 (26)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2 (27)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3 (28)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	TIR4 (29)

SYMBOLS	POSITIONS	NAME AND DESCRIPTION
CH1 - 32	TIR1.0 - 4.7	**Transmit Idle Code Insertion Control Bits.** 0 = do not insert the Idle Code in the TIDR into this channel 1 = insert the Idle Code in the TIDR into this channel

NOTE:

If CCR3.5 = 1, then a zero in the TIRs implies that channel data is to be sourced from TSER and a one implies that channel data is to be sourced from the output of the receive side framer (i.e., Per–Channel Loopback; see Figure 3-1).

TIDR: TRANSMIT IDLE DEFINITION REGISTER (Address=2A Hex)

(MSB)							(LSB)
TIDR7	TIDR6	TIDR5	TIDR4	TIDR3	TIDR2	TIDR1	TIDR0

SYMBOL	POSITION	NAME AND DESCRIPTION
TIDR7	TIDR.7	MSB of the Idle Code (this bit is transmitted first)
TIDR0	TIDR.0	LSB of the Idle Code (this bit is transmitted last)

11.1.2 Per–Channel Code Insertion

The second method involves using the Transmit Channel Control Registers (TCC1/2/3/4) to determine which of the 32 E1 channels should be overwritten with the code placed in the Transmit Channel Registers (TC1 to TC32). This method is more flexible than the first in that it allows a different 8–bit code to be placed into each of the 32 E1 channels.

TC1 TO TC32: TRANSMIT CHANNEL REGISTERS (Address=60 to 7F Hex)

(for brevity, only channel one is shown; see for other register address)

(MSB)							(LSB)	
C7	C6	C5	C4	C3	C2	C1	C0	TC1 (60)

SYMBOL	POSITION	NAME AND DESCRIPTION
C7	TC1.7	MSB of the Code (this bit is transmitted first)
C0	TC1.0	LSB of the Code (this bit is transmitted last)

TCC1/TCC2/TCC3/TCC4: TRANSMIT CHANNEL CONTROL REGISTER

(Address=A0 to A3 Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCC1 (A0)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCC2 (A1)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCC3 (A2)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	TCC4 (A3)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH 1 - 32	TCC1.0 - 4.7	**Transmit Channel Code Insertion Control Bits** 0 = do not insert data from the TC register into the transmit data stream 1 = insert data from the TC register into the transmit data stream

11.2 Receive Side Code Generation

On the receive side, the Receive Channel Control Registers (RCC1/2/3/4) are used to determine which of the 32 E1 channels off of the E1 line and going to the backplane should be overwritten with the code placed in the Receive Channel Registers (RC1 to RC32). This method allows a different 8–bit code to be placed into each of the 32 E1 channels.

RC1 TO RC32: RECEIVE CHANNEL REGISTERS (Address = 80 to 9F Hex)

(for brevity, only channel one is shown; see Table 5-1 for other register address)

(MSB)							(LSB)	
C7	C6	C5	C4	C3	C2	C1	C0	RC1 (80)

SYMBOL	POSITION	NAME AND DESCRIPTION
C7	RC1.7	MSB of the Code (this bit is sent first to the backplane)
C0	RC1.0	LSB of the Code (this bit is sent last to the backplane)

RCC1/RCC2/RCC3/RCC4: RECEIVE CHANNEL CONTROL REGISTER

(Address = A4 to A7 Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCC1 (A4)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCC2 (A5)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCC3 (A6)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	RCC4 (A7)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH1 - 32	RCC1.0 – 4.7	**Receive Channel Code Insertion Control Bits** 0 = do not insert data from the RC1 register into the receive data stream 1 = insert data from the RC1 register into the receive data stream

12 CLOCK BLOCKING REGISTERS

The Receive Channel blocking Registers (RCBR1 / RCBR2 / RCBR3 / RCBR4) and the Transmit Channel Blocking Registers (TCBR1 / TCBR2 / TCBR3 / TCBR4) control RCHBLK and TCHBLK pins respectively. (The RCHBLK and TCHBLK pins are user programmable outputs that can be forced either high or low during individual channels). These outputs can be used to block clocks to a USART or LAPD controller in ISDN–PRI applications.

When the appropriate bits are set to a one, the RCHBLK and TCHBLK pin will be held high during the entire corresponding channel time. See the timing in Section 19 for an example. The TCBRs have alternate mode of use. Via the CCR3.6 bit, the user has the option to use the TCBRs to determine on a channel by channel basis, which signaling bits are to be inserted via the TSRs (the corresponding bit in the TCBRs = 1) and which are to be sourced from the TSER or TSIG pins (the corresponding bit in the TCBR = 0). See the timing in Section 19.2 for an example.

RCBR1/RCBR2/RCBR3/RCBR4: RECEIVE CHANNEL BLOCKING REGISTERS (Address=2B to 2E Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCBR1 (2B)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCBR2 (2C)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCBR3 (2D)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	RCBR4 (2E)

SYMBOLS	POSITIONS	NAME AND DESCRIPTION
CH1 - 32	RCBR1.0 - 4.7	**Receive Channel Blocking Control Bits.** 0 = force the RCHBLK pin to remain low during this channel time 1 = force the RCHBLK pin high during this channel time

TCBR1/TCBR2/TCBR3/TCBR4: TRANSMIT CHANNEL BLOCKING REGISTERS (Address=22 to 25 Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCBR1 (22)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCBR2 (23)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCBR3 (24)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	TCBR4 (25)

SYMBOLS	POSITIONS	NAME AND DESCRIPTION
CH1 - 32	TCBR1.0 - 4.7	**Transmit Channel Blocking Control Bits.** 0 = force the TCHBLK pin to remain low during this channel time 1 = force the TCHBLK pin high during this channel time

NOTE:

If CCR3.6 = 1, then a zero in the TCBRs implies that signaling data is to be sourced from TSER (or TSIG if CCR3.2 = 1) and a one implies that signaling data for that channel is to be sourced from the Transmit Signaling (TS) registers. In this mode, the Voice Channel numbering scheme (CH1 – CH30) is used. See definition below.

TCBR1/TCBR2/TCBR3/TCBR4: DEFINITION WHEN CCR3.6=1

(MSB)							(LSB)	
CH18	CH3	CH17	CH2	CH16	CH1	1*	1*	TCBR1(22)
CH22	CH7	CH21	CH6	CH20	CH5	CH19	CH4	TCBR2(23)
CH26	CH11	CH25	CH10	CH24	CH9	CH23	CH8	TCBR3(24)
CH30	CH15	CH29	CH14	CH28	CH13	CH27	CH12	TCBR4(25)

* these bits should be set to one to allow the internal TS1 register to create the CAS Multiframe Alignment Word and Spare/Remote Alarm bits.

13 ELASTIC STORES OPERATION

The DS21354/554 contains dual two–frame (512 bits) elastic stores, one for the receive direction, and one for the transmit direction. These elastic stores have two main purposes. First, they can be used to rate convert the E1 data stream to 1.544 Mbps (or a multiple of 1.544 Mbps) which is the T1 rate. Secondly, they can be used to absorb the differences in frequency and phase between the E1 data stream and an asynchronous (i.e., not frequency locked) backplane clock which can be 1.544 MHz or 2.048/4.096/8.192 MHz. The backplane clock can burst at rates up to 8.192 MHz. Both elastic stores contain full controlled slip capability which is necessary for this second purpose. The elastic stores can be forced to a known depth via the Elastic Store Reset bits (CCR6.0 & CCR6.1). Toggling these bits forces the read and write pointers into opposite frames. Both elastic stores within a framer are fully independent and no restrictions apply to the sourcing of the various clocks that are applied to them. The transmit side elastic store can be enabled whether the receive elastic store is enabled or disabled and vice versa. Also, each elastic store can interface to either a 1.544 MHz or 2.048/4.096/8.192 MHz backplane without regard to the backplane rate the other elastic store is interfacing.

13.1 Receive Side

If the receive side elastic store is enabled (RCR2.1=1), then the user must provide either a 1.544 MHz (RCR2.2 =0) or 2.048/4.096/8.192 MHz (RCR2.2 = 1) clock at the RSYSCLK pin. The user has the option of either providing a frame/multiframe sync at the RSYNC pin (RCR1.5 = 1) or having the RSYNC pin provide a pulse on frame/multiframe boundaries (RCR1.5 = 0). If the user wishes to obtain pulses at the frame boundary, then RCR1.6 must be set to zero and if the user wishes to have pulses occur at the multiframe boundary, then RCR1.6 must be set to one. The DS21354/554 will always indicate frame boundaries via the RFSYNC output whether the elastic store is enabled or not. If the elastic store is enabled, then either CAS (RCR1.7 = 0) or CRC4 (RCR1.7 = 1) multiframe boundaries will be indicated via the RMSYNC output. If the user selects to apply a 1.544 MHz clock to the RSYSCLK pin, then every fourth channel of the received E1 data will be deleted and a F–bit position (which will be forced to one) will be inserted. Hence Channels 1, 5, 9, 13, 17, 21, 25, and 29 (timeslots 0, 4, 8, 12, 16, 20, 24, and 28) will be deleted from the received E1 data stream. Also, in 1.544 MHz applications, the RCHBLK output will not be active in Channels 25 through 32 (or in other words, RCBR4 is not active). See Section 19.1 for timing details. If the 512–bit elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data (256–bits) will be repeated at RSER and the SR1.4 and RIR.3 bits will be set to a one. If the buffer fills, then a full frame of data will be deleted and the SR1.4 and RIR.4 bits will be set to a one.

13.2 Transmit Side

The operation of the transmit elastic store is very similar to the receive side. The transmit side elastic store is enabled via CCR3.7. A 1.544 MHz (CCR3.1 = 0) or 2.048/4.096/8.192 MHz (CCR3.1 = 1) clock can be applied to the TSYSCLK input. The TSYSCLK can be a bursty clock with rates up to 8.192 MHz. The user must supply either an 8 kHz frame sync pulse or a multiframe sync pulse to the TSSYNC input. See Section 19.2 for timing details. Controlled slips in the transmit elastic store are reported in the SR2.0 bit and the direction of the slip is reported in the RIR.6 and RIR.7 bits.

14 ADDITIONAL (Sa) AND INTERNATIONAL (Si) BIT OPERATION

The DS21354/554 provides for access to both the Sa and the Si bits via three different methods. The first is via a hardware scheme using the RLINK/RLCLK and TLINK/ TLCLK pins. The first method is discussed in Section 14.1. The second involves using the internal RAF/RNAF and TAF/TNAF registers and is discussed in Section 14.2 The third method which is covered in Section 14.3 involves an expanded version of the second method and is one of the features added to the DS2154/354/554 from the original DS2153 definition.

14.1 Hardware Scheme

On the receive side, all of the received data is reported at the RLINK pin. Via RCR2, the user can control the RLCLK pin to pulse during any combination of Sa bits. This allows the user to create a clock that can be used to capture the needed Sa bits. If RSYNC is programmed to output a frame boundary, it will identify the Si bits. See Section 19.1 for detailed timing.

On the transmit side, the individual Sa bits can be either sourced from the internal TNAF register (see Section 14.2 for details) or from the external TLINK pin. Via TCR2, the framer can be programmed to source any combination of the additional bits from the TLINK pin. If the user wishes to pass the Sa bits through the framer without them being altered, then the device should be set up to source all five Sa bits via the TLINK pin and the TLINK pin should be tied to the TSER pin. Si bits can be inserted through the TSER pin via the clearing of the TCR1.3 bit. Please see the timing diagrams and the transmit data flow diagram in Section 19.2 for examples.

14.2 Internal Register Scheme Based On Double–Frame

On the receive side, the RAF and RNAF registers will always report the data as it received in the Additional and International bit locations. The RAF and RNAF registers are updated with the setting of the Receive Align Frame bit in Status Register 2 (SR2.6). The host can use the SR2.6 bit to know when to read the RAF and RNAF registers. It has 250 us to retrieve the data before it is lost.

On the transmit side, data is sampled from the TAF and TNAF registers with the setting of the Transmit Align Frame bit in Status Register 2 (SR2.3). The host can use the SR2.3 bit to know when to update the TAF and TNAF registers. It has 250 us to update the data or else the old data will be retransmitted. Data in the Si bit position will be overwritten if either the framer is programmed: (1) to source the Si bits from the TSER pin, (2) in the CRC4 mode, or (3) have automatic E–bit insertion enabled. Data in the Sa bit position will be overwritten if any of the TCR2.3 to TCR2.7 bits are set to one (please see Section 14.1 for details). Please see the register descriptions for TCR1 and TCR2 and Figure 19-15 for more details.

RAF: RECEIVE ALIGN FRAME REGISTER (Address=2F Hex)

(MSB)							(LSB)
Si	0	0	1	1	0	1	1

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	RAF.7	**International Bit.**
0	RAF.6	**Frame Alignment Signal Bit.**
0	RAF.5	**Frame Alignment Signal Bit.**
1	RAF.4	**Frame Alignment Signal Bit.**
1	RAF.3	**Frame Alignment Signal Bit.**
0	RAF.2	**Frame Alignment Signal Bit.**
1	RAF.1	**Frame Alignment Signal Bit.**
1	RAF.0	**Frame Alignment Signal Bit.**

RNAF: RECEIVE NON–ALIGN FRAME REGISTER (Address=1F Hex)

(MSB)							(LSB)
Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	RNAF.7	**International Bit.**
1	RNAF.6	**Frame Non–Alignment Signal Bit.**
A	RNAF.5	**Remote Alarm.**
Sa4	RNAF.4	**Additional Bit 4.**
Sa5	RNAF.3	**Additional Bit 5.**
Sa6	RNAF.2	**Additional Bit 6.**
Sa7	RNAF.1	**Additional Bit 7.**
Sa8	RNAF.0	**Additional Bit 8.**

TAF: TRANSMIT ALIGN FRAME REGISTER (Address=20 Hex)

(MSB)							(LSB)
Si	0	0	1	1	0	1	1

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	TAF.7	**International Bit.**
0	TAF.6	**Frame Alignment Signal Bit.**
0	TAF.5	**Frame Alignment Signal Bit.**
1	TAF.4	**Frame Alignment Signal Bit.**
1	TAF.3	**Frame Alignment Signal Bit.**
0	TAF.2	**Frame Alignment Signal Bit.**
1	TAF.1	**Frame Alignment Signal Bit.**
1	TAF.0	**Frame Alignment Signal Bit.**

Note:

The TAF register must be programmed with the seven bit FAS word; the DS21354/554 does not automatically set these bits

TNAF: TRANSMIT NON–ALIGN FRAME REGISTER (Address=21 Hex)

(MSB)							(LSB)
Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	TNAF.7	**International Bit.**
1	TNAF.6	**Frame Non–Alignment Signal Bit.**
A	TNAF.5	**Remote Alarm (used to transmit the alarm).**
Sa4	TNAF.4	**Additional Bit 4.**
Sa5	TNAF.3	**Additional Bit 5.**
Sa6	TNAF.2	**Additional Bit 6.**
Sa7	TNAF.1	**Additional Bit 7.**
Sa8	TNAF.0	**Additional Bit 8.**

Note:
Bit 2 of the TNAF register must be programmed to one; the DS21354/554 does not automatically set this bit

14.3 Internal Register Scheme Based On CRC4 Multiframe

On the receive side, there is a set of eight registers (RSiAF, RSiNAF, RRA, RSa4 to RSa8) that report the Si and Sa bits as they are received. These registers are updated with the setting of the Receive CRC4 Multiframe bit in Status Register 2 (SR2.1). The host can use the SR2.1 bit to know when to read these registers. The user has 2 ms to retrieve the data before it is lost. The MSB of each register is the first received. Please see the register descriptions below for more details.

On the transmit side, there is also a set of eight registers (TSiAF, TSiNAF, TRA, TSa4 to TSa8) that via the Transmit Sa Bit Control Register (TSaCR), can be programmed to insert both Si and Sa data. Data is sampled from these registers with the setting of the Transmit Multiframe bit in Status Register 2 (SR2.5). The host can use the SR2.5 bit to know when to update these registers. It has 2 ms to update the data or else the old data will be retransmitted. The MSB of each register is the first bit transmitted. Please see the register descriptions below and Figure 19-15 for more details.

REGISTER	ADDRESS (HEX)	FUNCTION
RSiAF	58	The eight Si bits in the align frame
RSiNAF	59	The eight Si bits in the non–align frame
RRA	5A	The eight reportings of the receive remote alarm (RA)
RSa4	5B	The eight Sa4 reported in each CRC4 multiframe
RSa5	5C	The eight Sa5 reported in each CRC4 multiframe
RSa6	5D	The eight Sa6 reported in each CRC4 multiframe
RSa7	5E	The eight Sa7 reported in each CRC4 multiframe
RSa8	5F	The eight Sa8 reported in each CRC4 multiframe
TSiAF	50	The eight Si bits to be inserted into the align frame
TSiNAF	51	The eight Si bits to be inserted into the non–align frame
TRA	52	The eight settings of remote alarm (RA)
TSa4	53	The eight Sa4 settings in each CRC4 multiframe
TSa5	54	The eight Sa5 settings in each CRC4 multiframe
TSa6	55	The eight Sa6 settings in each CRC4 multiframe
TSa7	56	The eight Sa7 settings in each CRC4 multiframe
TSa8	57	The eight Sa8 settings in each CRC4 multiframe

TSaCR: TRANSMIT Sa BIT CONTROL REGISTER (Address=1C Hex)

(MSB)							(LSB)
SiAF	SiNAF	RA	Sa4	Sa5	Sa6	Sa7	Sa8

SYMBOL	POSITION	NAME AND DESCRIPTION
SiAF	TSaCR.7	**International Bit in Align Frame Insertion Control Bit.** 0 = do not insert data from the TSiAF register into the transmit data stream 1 = insert data from the TSiAF register into the transmit data stream

SYMBOL	POSITION	NAME AND DESCRIPTION
SiNAF	TSaCR.6	**International Bit in Non–Align Frame Insertion Control Bit.** 0 = do not insert data from the TSiNAF register into the transmit data stream 1 = insert data from the TSiNAF register into the transmit data stream
RA	TSaCR.5	**Remote Alarm Insertion Control Bit.** 0 = do not insert data from the TRA register into the transmit data stream 1 = insert data from the TRA register into the transmit data stream
Sa4	TSaCR.4	**Additional Bit 4 Insertion Control Bit.** 0 = do not insert data from the TSa4 register into the transmit data stream 1 = insert data from the TSa4 register into the transmit data stream
Sa5	TSaCR.3	**Additional Bit 5 Insertion Control Bit.** 0 = do not insert data from the TSa5 register into the transmit data stream 1 = insert data from the TSa5 register into the transmit data stream
Sa6	TSaCR.2	**Additional Bit 6 Insertion Control Bit.** 0 = do not insert data from the TSa6 register into the transmit data stream 1 = insert data from the TSa6 register into the transmit data stream
Sa7	TSaCR.1	**Additional Bit 7 Insertion Control Bit.** 0 = do not insert data from the TSa7 register into the transmit data stream 1 = insert data from the TSa7 register into the transmit data stream
Sa8	TSaCR.0	**Additional Bit 8 Insertion Control Bit.** 0 = do not insert data from the TSa8 register into the transmit data stream 1 = insert data from the TSa8 register into the transmit data stream

15 HDLC CONTROLLER FOR THE Sa BITS OR DS0

The DS21354/554 has the ability to extract/insert data from/into the Sa bit positions (Sa4 to Sa8) or from/to any multiple of DS0 or sub DS0 channels. The SCT contains a complete HDLC controller and this operation is covered in Section 15.1.

15.1 General Overview

The DS21354/554 contains a complete HDLC controller with 64–byte buffers in both the transmit and receive directions The HDLC controller performs all the necessary overhead for generating and receiving an HDLC formatted message.

The HDLC controller automatically generates and detects flags, generates and checks the CRC check sum, generates and detects abort sequences, stuffs and destuffs zeros (for transparency), and byte aligns to the HDLC data stream.

There are eleven registers that the host will use to operate and control the operation of the HDLC controller. A brief description of the registers is shown in Table 15.1.

HDLC CONTROLLER REGISTER LIST Table 15-1

NAME	FUNCTION
HDLC Control Register (HCR) HDLC Status Register (HSR) HIMR Interrupt Mask Register (HIMR)	general control over the HDLC controller key status information for both transmit and receive directions allows/stops status bits to/from causing an interrupt
Receive HDLC Information register (RHIR) Receive HDLC FIFO Register (RHFR) Receive HDLC DS0 Control Register 1 (RDC1) Receive HDLC DS0 Control Register 2 (RDC2)	status information on receive HDLC controller access to 64–byte HDLC FIFO in receive direction controls the HDLC function when used on DS0 channels controls the HDLC function when used on DS0 channels
Transmit HDLC Information register (THIR) Transmit HDLC FIFO Register (THFR) Transmit HDLC DS0 Control Register 1 (TDC1) Transmit HDLC DS0 Control Register 2 (TDC2)	status information on transmit HDLC controller access to 64–byte HDLC FIFO in transmit direction controls the HDLC function when used on DS0 channels controls the HDLC function when used on DS0 channels

15.2 HDLC Status Registers

Three of the HDLC controller registers (HSR, RHIR, and THIR) provide status information. When a particular event has occurred (or is occurring), the appropriate bit in one of these three registers will be set to a one. Some of the bits in these three status registers are latched and some are real time bits that are not latched. Section 15.4 contains register descriptions that list which bits are latched and which are not. With the latched bits, when an event occurs and a bit is set to a one, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again. The real time bits report the current instantaneous conditions that are occurring and the history of these bits is not latched.

Like the other status registers in the framer, the user will always proceed a read of any of the three registers with a write. The byte written to the register will inform the framer which of the latched bits the user wishes to read and have cleared (the real time bits are not affected by writing to the status register). The user will write a byte to one of these registers, with a one in the bit positions he or she wishes to read and a zero in the bit positions he or she does not wish to obtain the latest information on. When a one is written to a bit location, the read register will be updated with current value and it will be cleared. When a zero is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that bit does indeed clear. This second write step is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. This write–read–write (for polled driven access) or write–read (for interrupt driven access) scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS21354/554 with higher–order software languages.

Like the SR1 and SR2 status registers, the HSR register has the unique ability to initiate a hardware interrupt via the INT* output pin. Each of the events in the HSR can be either masked or unmasked from the interrupt pin via the HDLC Interrupt Mask Register (HIMR). Interrupts will force the INT* pin low when the event occurs. The INT pin will be allowed to return high (if no other interrupts are present) when the user reads the event bit that caused the interrupt to occur.

15.3 Basic Operation Details

As a basic guideline for interpreting and sending HDLC messages, the following sequences can be applied:

15.3.1 Receive a HDLC Message

1. enable RPS interrupts
2. wait for interrupt to occur
3. disable RPS interrupt and enable either RPE, RNE, or RHALF interrupt
4. read RHIR to obtain REMPTY status
    a. if REMPTY=0, then record OBYTE, CBYTE, and POK bits and then read the FIFO
        a1. if CBYTE=0 then skip to step 5
        a2. if CBYTE=1 then skip to step 7
    b. if REMPTY=1, then skip to step 6
5. repeat step 4
6. wait for interrupt, skip to step 4
7. if POK=0, then discard whole packet, if POK=1, accept the packet
    a. disable RPE, RNE, or RHALF interrupt, enable RPS interrupt and return to step 1.

15.3.2 Transmit an HDLC Message

1. make sure HDLC controller is done sending any previous messages and is current sending flags by checking that the FIFO is empty by reading the TEMPTY status bit in the THIR register
2. enable either the THALF or TNF interrupt
3. read THIR to obtain TFULL status
    a. if TFULL=0, then write a byte into the FIFO and skip to next step (special case occurs when the last byte is to be written, in this case set TEOM=1 before writing the byte and then skip to step 6)
    b. if TFULL=1, then skip to step 5
4. repeat step 3
5. wait for interrupt, skip to step 3
6. disable THALF or TNF interrupt and enable TMEND interrupt
7. wait for an interrupt, then read TUDR status bit to make sure packet was transmitted correctly.

15.4 HDLC Register Description

HCR: HDLC CONTROL REGISTER (Address=B0 Hex)

(MSB)							(LSB)
–	RHR	TFS	THR	TABT	TEOM	TZSD	TCRCD

SYMBOL	POSITION	NAME AND DESCRIPTION
–	HCR.7	**Not Assigned.** Should be set to zero when written.
RHR	HCR.6	**Receive HDLC Reset.** A 0 to 1 transition will reset the HDLC controller. Must be cleared and set again for a subsequent reset.
TFS	HCR.5	**Transmit Flag/Idle Select.** 0 = 7Eh 1 = FFh
THR	HCR.4	**Transmit HDLC Reset.** A 0 to 1 transition will reset the HDLC controller. Must be cleared and set again for a subsequent reset.
TABT	HCR.3	**Transmit Abort.** A 0 to 1 transition will cause the FIFO contents to be dumped and one FEh abort to be sent followed by 7Eh or FFh flags/idle until a new packet is initiated by writing new data into the FIFO. Must be cleared and set again for a subsequent abort to be sent.
TEOM	HCR.2	**Transmit End of Message.** Should be set to a one just before the last data byte of a HDLC packet is written into the transmit FIFO at THFR. This bit will be cleared by the HDLC controller when the last byte has been transmitted.
TZSD	HCR.1	**Transmit Zero Stuffer Defeat.** Overrides internal enable. 0 = enable the zero stuffer (normal operation) 1 = disable the zero stuffer
TCRCD	HCR.0	**Transmit CRC Defeat.** 0 = enable CRC generation (normal operation) 1 = disable CRC generation

HSR: HDLC STATUS REGISTER (Address=B1 Hex)

(MSB)							(LSB)
FRCL	RPE	RPS	RHALF	RNE	THALF	TNF	TMEND

SYMBOL	POSITION	NAME AND DESCRIPTION
FRCL	HSR.7	**Framer Receive Carrier Loss.** Set when 255 (or 2048 if CCR3.0 = 1) consecutive zeros have been detected at RPOSI and RNEGI.
RPE	HSR.6	**Receive Packet End.** Set when the HDLC controller detects either the finish of a valid message (i.e., CRC check complete) or when the controller has experienced a message fault such as a CRC checking error, or an overrun condition, or an abort has been seen. The setting of this bit prompts the user to read the RHIR register for details.
RPS	HSR.5	**Receive Packet Start**. Set when the HDLC controller detects an opening byte. The setting of this bit prompts the user to read the RHIR register for details.

SYMBOL	POSITION	NAME AND DESCRIPTION
RHALF	HSR.4	**Receive FIFO Half Full.** Set when the receive 64–byte FIFO fills beyond the half way point. The setting of this bit prompts the user to read the RHIR register for details.
RNE	HSR.3	**Receive FIFO Not Empty.** Set when the receive 64–byte FIFO has at least one byte available for a read. The setting of this bit prompts the user to read the RHIR register for details.
THALF	HSR.2	**Transmit FIFO Half Empty.** Set when the transmit 64–byte FIFO empties beyond the half way point. The setting of this bit prompts the user to read the THIR register for details.
TNF	HSR.1	**Transmit FIFO Not Full.** Set when the transmit 64–byte FIFO has at least one byte available. The setting of this bit prompts the user to read the THIR register for details.
TMEND	HSR.0	**Transmit Message End.** Set when the transmit HDLC controller has finished sending a message. The setting of this bit prompts the user to read the THIR register for details.

NOTE:

The RPE, RPS, and TMEND bits are latched and will be cleared when read.

HIMR: HDLC INTERRUPT MASK REGISTER (Address=B2 Hex)

(MSB)							(LSB)
FRCL	RPE	RPS	RHALF	RNE	THALF	TNF	TMEND

SYMBOL	POSITION	NAME AND DESCRIPTION
FRCL	HIMR.7	**Framer Receive Carrier Loss.** 0 = interrupt masked 1 = interrupt enabled
RPE	HIMR.6	**Receive Packet End.** 0 = interrupt masked 1 = interrupt enabled
RPS	HIMR.5	**Receive Packet Start.** 0 = interrupt masked 1 = interrupt enabled
RHALF	HIMR.4	**Receive FIFO Half Full.** 0 = interrupt masked 1 = interrupt enabled
RNE	HIMR.3	**Receive FIFO Not Empty.** 0 = interrupt masked 1 = interrupt enabled
THALF	HIMR.2	**Transmit FIFO Half Empty.** 0 = interrupt masked 1 = interrupt enabled
TNF	HIMR.1	**Transmit FIFO Not Full.** 0 = interrupt masked 1 = interrupt enabled

SYMBOL	POSITION	NAME AND DESCRIPTION
TMEND	HIMR.0	**Transmit Message End.** 0 = interrupt masked 1 = interrupt enabled

RHIR: RECEIVE HDLC INFORMATION REGISTER (Address=B3 Hex)

(MSB)							(LSB)
RABT	RCRCE	ROVR	RVM	REMPTY	POK	CBYTE	OBYTE

SYMBOL	POSITION	NAME AND DESCRIPTION
RABT	RHIR.7	**Abort Sequence Detected.** Set whenever the HDLC controller sees 7 or more ones in a row.
RCRCE	RHIR.6	**CRC Error.** Set when the CRC checksum is in error.
ROVR	RHIR.5	**Overrun.** Set when the HDLC controller has attempted to write a byte into an already full receive FIFO.
RVM	RHIR.4	**Valid Message.** Set when the HDLC controller has detected and checked a complete HDLC packet.
REMPTY	RHIR.3	**Empty.** A real–time bit that is set high when the receive FIFO is empty.
POK	RHIR.2	**Packet OK.** Set when the byte available for reading in the receive FIFO at RHFR is the last byte of a valid message (and hence no abort was seen, no overrun occurred, and the CRC was correct).
CBYTE	RHIR.1	**Closing Byte.** Set when the byte available for reading in the receive FIFO at RHFR is the last byte of a message (whether the message was valid or not).
OBYTE	RHIR.0	**Opening Byte.** Set when the byte available for reading in the receive FIFO at RHFR is the first byte of a message.

NOTE:

The RABT, RCRCE, ROVR, and RVM bits are latched and will be cleared when read.

RHFR: RECEIVE HDLC FIFO REGISTER (Address=B4 Hex)

(MSB)							(LSB)
HDLC7	HDLC6	HDLC5	HDLC4	HDLC3	HDLC2	HDLC1	HDLC0

SYMBOL	POSITION	NAME AND DESCRIPTION
HDLC7	RHFR.7	**HDLC Data Bit 7**. MSB of a HDLC packet data byte.
HDLC6	RHFR.6	**HDLC Data Bit 6.**
HDLC5	RHFR.5	**HDLC Data Bit 5.**
HDLC4	RHFR.4	**HDLC Data Bit 4.**
HDLC3	RHFR.3	**HDLC Data Bit 3.**
HDLC2	RHFR.2	**HDLC Data Bit 2.**
HDLC1	RHFR.1	**HDLC Data Bit 1.**
HDLC0	RHFR.0	**HDLC Data Bit 0.** LSB of a HDLC packet data byte.

THIR: TRANSMIT HDLC INFORMATION REGISTER (Address=B6 Hex)

(MSB)							(LSB)
–	–	–	–	–	TEMPTY	TFULL	TUDR

SYMBOL	POSITION	NAME AND DESCRIPTION
–	THIR.7	**Not Assigned.** Could be any value when read.
–	THIR.6	**Not Assigned.** Could be any value when read.
–	THIR.5	**Not Assigned.** Could be any value when read.
–	THIR.4	**Not Assigned.** Could be any value when read.
–	THIR.3	**Not Assigned.** Could be any value when read.
TEMPTY	THIR.2	**Transmit FIFO Empty.** A real–time bit that is set high when the FIFO is empty.
TFULL	THIR.1	**Transmit FIFO Full.** A real–time bit that is set high when the FIFO is full.
TUDR	THIR.0	**Transmit FIFO Under-run.** Set when the transmit FIFO empties out without the TEOM control bit being set. An abort is automatically sent.

NOTE:

The TUDR bit is latched and will be cleared when read.

THFR: TRANSMIT HDLC FIFO REGISTER (Address=B7 Hex)

(MSB)							(LSB)
HDLC7	HDLC6	HDLC5	HDLC4	HDLC3	HDLC2	HDLC1	HDLC0

SYMBOL	POSITION	NAME AND DESCRIPTION
HDLC7	THFR.7	**HDLC Data Bit 7.** MSB of a HDLC packet data byte.
HDLC6	THFR.6	**HDLC Data Bit 6.**
HDLC5	THFR.5	**HDLC Data Bit 5.**
HDLC4	THFR.4	**HDLC Data Bit 4.**
HDLC3	THFR.3	**HDLC Data Bit 3.**
HDLC2	THFR.2	**HDLC Data Bit 2.**
HDLC1	THFR.1	**HDLC Data Bit 1.**
HDLC0	THFR.0	**HDLC Data Bit 0.** LSB of a HDLC packet data byte.

RDC1: RECEIVE HDLC DS0 CONTROL REGISTER 1 (Address=B8 Hex)

(MSB)							(LSB)
RHS	RSaDS	RDS0M	RD4	RD3	RD2	RD1	RD0

SYMBOL	POSITION	NAME AND DESCRIPTION
RHS	RDC1.7	**Receive HDLC source** 0 = Sa bits defined by RCR2.3 to RCR2.7. 1 = Sa bits or DS0 channels defined by RDC1 (see bits defined below).
RSaDS	RDC1.6	**Receive Sa Bit / DS0 Select.** 0 = route Sa bits to the HDLC controller. RD0 to RD4 defines which Sa bits are to be routed. RD4 corresponds to Sa4, RD3 to Sa5, RD2 to Sa6, RD1 to Sa7 and RD0 to Sa8.

SYMBOL	POSITION	NAME AND DESCRIPTION
		1 = route DS0 channels into the HDLC controller. RDC1.5 is used to determine how the DS0 channels are selected.
RDS0M	RDC1.5	**DS0 Selection Mode.** 0 = utilize the RD0 to RD4 bits to select which single DS0 channel to use. 1 = utilize the RCHBLK control registers to select which DS0 channels to use.
RD4	RDC1.4	**DS0 Channel Select Bit 4.** MSB of the DS0 channel select.
RD3	RDC1.3	**DS0 Channel Select Bit 3.**
RD2	RDC1.2	**DS0 Channel Select Bit 2.**
RD1	RDC1.1	**DS0 Channel Select Bit 1.**
RD0	RDC1.0	**DS0 Channel Select Bit 0.** LSB of the DS0 channel select.

RDC2: RECEIVE HDLC DS0 CONTROL REGISTER 2 (Address=B9 Hex)

(MSB)							(LSB)
RDB8	RDB7	RDB6	RDB5	RDB4	RDB3	RDB2	RDB1

SYMBOL	POSITION	NAME AND DESCRIPTION
RDB8	RDC2.7	**DS0 Bit 8 Suppress Enable.** MSB of the DS0. Set to one to stop this bit from being used.
RDB7	RDC2.6	**DS0 Bit 7 Suppress Enable.** Set to one to stop this bit from being used.
RDB6	RDC2.5	**DS0 Bit 6 Suppress Enable.** Set to one to stop this bit from being used.
RDB5	RDC2.4	**DS0 Bit 5 Suppress Enable.** Set to one to stop this bit from being used.
RDB4	RDC2.3	**DS0 Bit 4 Suppress Enable.** Set to one to stop this bit from being used.
RDB3	RDC2.2	**DS0 Bit 3 Suppress Enable.** Set to one to stop this bit from being used.
RDB2	RDC2.1	**DS0 Bit 2 Suppress Enable.** Set to one to stop this bit from being used.
RDB1	RDC2.0	**DS0 Bit 1 Suppress Enable.** LSB of the DS0. Set to one to stop this bit from being used.

TDC1: TRANSMIT HDLC DS0 CONTROL REGISTER 1 (Address=BA Hex)

(MSB)							(LSB)
THE	TSaDS	TDS0M	TD4	TD3	TD2	TD1	TD0

SYMBOL	POSITION	NAME AND DESCRIPTION
THE	TDC1.7	**Transmit HDLC Enable.** 0 = disable HDLC controller (no data inserted by HDLC controller into the transmit data stream) 1 = enable HDLC controller to allow insertion of HDLC data into either the Sa position or multiple DS0 channels as defined by TDC1 (see bit definitions below).
TSaDS	TDC1.6	**Transmit Sa Bit / DS0 Select.** This bit is ignored if TDC1.7 is set to zero. 0 = route Sa bits from the HDLC controller. TD0 to TD4 defines which Sa bits are to be routed. TD4 corresponds to Sa4, TD3 to Sa5, TD2 to Sa6, TD1 to Sa7 and TD0 to Sa8. 1 = route DS0 channels from the HDLC controller. TDC1.5 is used to determine how the DS0 channels are selected.

SYMBOL	POSITION	NAME AND DESCRIPTION
TDS0M	TDC1.5	**DS0 Selection Mode.** 0 = utilize the TD0 to TD4 bits to select which single DS0 channel to use. 1 = utilize the TCHBLK control registers to select which DS0 channels to use.
TD4	TDC1.4	**DS0 Channel Select Bit 4.** MSB of the DS0 channel select.
TD3	TDC1.3	**DS0 Channel Select Bit 3.**
TD2	TDC1.2	**DS0 Channel Select Bit 2.**
TD1	TDC1.1	**DS0 Channel Select Bit 1.**
TD0	TDC1.0	**DS0 Channel Select Bit 0.** LSB of the DS0 channel select.

TDC2: TRANSMIT HDLC DS0 CONTROL REGISTER 2 (Address=BB Hex)

(MSB)							(LSB)
TDB8	TDB7	TDB6	TDB5	TDB4	TDB3	TDB2	TDB1

SYMBOL	POSITION	NAME AND DESCRIPTION
TDB8	TDC2.7	**DS0 Bit 8 Suppress Enable.** MSB of the DS0. Set to one to stop this bit from being used.
TDB7	TDC2.6	**DS0 Bit 7 Suppress Enable.** Set to one to stop this bit from being used.
TDB6	TDC2.5	**DS0 Bit 6 Suppress Enable.** Set to one to stop this bit from being used.
TDB5	TDC2.4	**DS0 Bit 5 Suppress Enable.** Set to one to stop this bit from being used.
TDB4	TDC2.3	**DS0 Bit 4 Suppress Enable.** Set to one to stop this bit from being used.
TDB3	TDC2.2	**DS0 Bit 3 Suppress Enable.** Set to one to stop this bit from being used.
TDB2	TDC2.1	**DS0 Bit 2 Suppress Enable.** Set to one to stop this bit from being used.
TDB1	TDC2.0	**DS0 Bit 1 Suppress Enable.** LSB of the DS0. Set to one to stop this bit from being used.

16 LINE INTERFACE FUNCTIONS

The line interface function in the DS21354/554 contains three sections; (1) the receiver which handles clock and data recovery, (2) the transmitter which waveshapes and drives the E1 line, and (3) the jitter attenuator. Each of the these three sections is controlled by the Line Interface Control Register (LICR) which is described below.

LICR: LINE INTERFACE CONTROL REGISTER (Address=18 Hex)

(MSB)							(LSB)
L2	L1	L0	EGL	JAS	JABDS	DJA	TPD

SYMBOL	POSITION	NAME AND DESCRIPTION
L2	LICR.7	**Line Build Out Select Bit 2.** Sets the transmitter build out; see Table 16-1 and Table 16-2.
L1	LICR.6	**Line Build Out Select Bit 1.** Sets the transmitter build out; see Table 16-1 and Table 16-2.
L0	LICR.5	**Line Build Out Select Bit 0.** Sets the transmitter build out; see Table 16-1 and Table 16-2.
EGL	LICR.4	**Receive Equalizer Gain Limit.** 0 = –12 dB 1 = –43 dB

SYMBOL	POSITION	NAME AND DESCRIPTION
JAS	LICR.3	**Jitter Attenuator Select.** 0 = place the jitter attenuator on the receive side 1 = place the jitter attenuator on the transmit side
JABDS	LICR.2	**Jitter Attenuator Buffer Depth Select.** 0 = 128 bits 1 = 32 bits (use for delay sensitive applications)
DJA	LICR.1	**Disable Jitter Attenuator.** 0 = jitter attenuator enabled 1 = jitter attenuator disabled
TPD	LICR.0	**Transmit Power Down.** 0 = normal transmitter operation 1 = powers down the transmitter and 3-states the TTIP and TRING pins

16.1 Receive Clock And Data Recovery

The DS21354/554 contains a digital clock recovery system. See Figure 3-1 and Figure 16-1 for more details. The device couples to the receive E1 shielded twisted pair or COAX via a 1:1 transformer. See Table 16-3 for transformer details. The 2.048 MHz clock attached at the MCLK pin is internally multiplied by 16 via an internal PLL and fed to the clock recovery system. The clock recovery system uses the clock from the PLL circuit to form a 16 times over-sampler which is used to recover the clock and data. This over-sampling technique offers outstanding jitter tolerance (see Figure 16-3).

Normally, the clock that is output at the RCLKO pin is the recovered clock from the E1 AMI/HDB3 waveform presented at the RTIP and RRING inputs. When no AMI signal is present at RTIP and RRING, a Receive Carrier Loss (RCL) condition will occur and the RCLKO will be sourced from the clock applied at the MCLK pin. If the jitter attenuator is either placed in the transmit path or is disabled, the RCLKO output can exhibit slightly shorter high cycles of the clock. This is due to the highly over-sampled digital clock recovery circuitry. If the jitter attenuator is placed in the receive path (as is the case in most applications), the jitter attenuator restores the RCLK to being close to 50% duty cycle. Please see the Receive AC Timing Characteristics in Section 21.3 for more details.

16.2 Transmit Waveshaping And Line Driving

The DS21354/554 uses a set of laser–trimmed delay lines along with a precision Digital–to–Analog Converter (DAC) to create the waveforms that are transmitted onto the E1 line. The waveforms meet the ITU G.703 specifications. See Figure 16-5.

The user will select which waveform is to be generated by properly programming the L2/L1/L0 bits in the Line Interface Control Register (LICR). The DS21354/554 can set up in a number of various configurations depending on the application. See tables below and Figure 16-5.

LINE BUILD OUT SELECT IN LICR FOR THE DS21554 Table 16-1

L2	L1	L0	APPLICATION	TRANSFORMER	RETURN LOSS*	RT**
0	0	0	75 ohm normal	1:1.15 step–up	NM	0 ohms
0	0	1	120 ohm normal	1:1.15 step–up	NM	0 ohms
0	1	0	75 ohm w/ protection resistors	1:1.15 step–up	NM	8.2 ohms
0	1	1	120 ohm w/ protection resistors	1:1.15 step–up	NM	8.2 ohms
1	0	0	75 ohm w/ high return loss	1:1.15 step–up	21dB	27 ohms
1	1	0	75 ohm w/ high return loss	1:1.36 step–up	21dB	18 ohms
1	0	0	120 ohm w/ high return loss	1:1.36 step–up	21dB	27 ohms

* NM = Not Meaningful (Return Loss value too low for significance)
** See *Application Note 324* for details on E1 line interface design

LINE BUILD OUT SELECT IN LICR FOR THE DS21354 Table 16-2

L2	L1	L0	APPLICATION	TRANSFORMER	RETURN LOSS*	RT**
0	0	0	75 ohm normal	1:2 step–up	NM	0 ohms
0	0	1	120 ohm normal	1:2 step–up	NM	0 ohms
0	1	0	75 ohm w/ protection resistors	1:2 step–up	NM	2.5 ohms
0	1	1	120 ohm w/ protection resistors	1:2 step–up	NM	2.5 ohms
1	0	0	75 ohm w/ high return loss	1:2 step–up	21dB	6.2 ohms
1	0	1	120 ohm w/ high return loss	1:2 step–up	21dB	11.6 ohms

* NM = Not Meaningful (Return Loss value too low for significance)
** See *Application Note 324* for details on E1 line interface design

Due to the nature of the design of the transmitter in the DS21354/554, very little jitter (less then 0.005 UIpp broadband from 10 Hz to 100 kHz) is added to the jitter present on TCLK. Also, the waveform created is independent of the duty cycle of TCLK. The transmitter in the device couples to the E1 transmit shielded twisted pair or COAX via a 1:1.15 or 1:1.36 step up transformer as shown in Figure 16-1. In order for the devices to create the proper waveforms, the transformer used must meet the specifications listed in Table 16-3. The line driver in the device contains a current limiter that will prevent more than 50 mA (rms) from being sourced in a 1 ohm load.

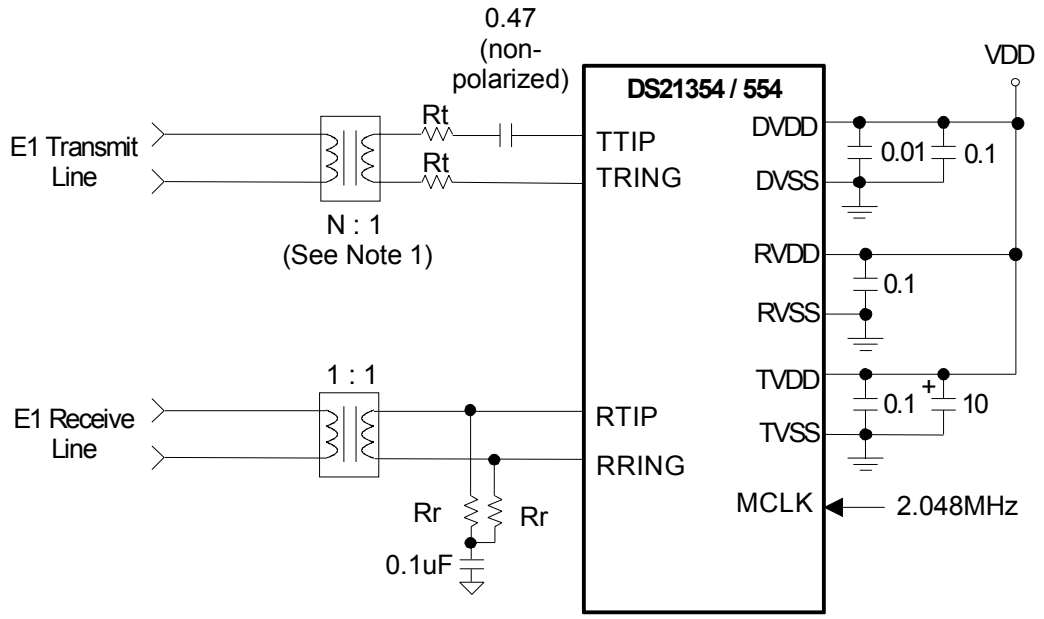
TRANSFORMER SPECIFICATIONS Table 16-3

SPECIFICATION	RECOMMENDED VALUE
Turns Ratio DS21354	1:1(receive) and 1:2(transmit)+/-3%
Turns Ratio DS21554	1:1(receive) and 1:1.15 or 1:1.36(transmit)+/-3%
Primary Inductance	600µH minimum
Leakage Inductance	1.0µH maximum
Intertwining Capacitance	40 pF maximum
DC Resistance	1.2 Ohms maximum

16.3 Jitter Attenuator

The DS21354/554 contains an onboard jitter attenuator that can be set to a depth of either 32 or 128 bits via the JABDS bit in the Line Interface Control Register (LICR). The 128–bit mode is used in applications where large excursions of wander are expected. The 32–bit mode is used in delay sensitive applications. The characteristics of the attenuation are shown in Figure 16-3. The jitter attenuator can be placed in either the receive path or the transmit path by appropriately setting or clearing the JAS bit in the LICR. Also, the jitter attenuator can be disabled (in effect, removed) by setting the DJA bit in the LICR. In order for the jitter attenuator to operate properly, a 2.048 MHz clock (+/-50 ppm) must be applied at the MCLK pin or a crystal with similar characteristics must be applied across the MCLK and XTALD pins. If a crystal is applied across the MCLK and XTALD pins, then the maximum effective series resistance should be 30 ohms and capacitors should be placed from each leg of the crystal to ground as shown in Figure 16-2. Onboard circuitry adjusts either the recovered clock from the clock/data recovery block or the clock applied at the TCLKI pin to create a smooth jitter free clock which is used to clock data out of the jitter attenuator FIFO. It is acceptable to provide a gapped/bursty clock at the TCLKI pin if the jitter attenuator is placed on the transmit side. If the incoming jitter exceeds either 120 UIpp (buffer depth is 128 bits) or 28 UIpp (buffer depth is 32 bits), then the DS21354/554 will divide the internal nominal 32.768 MHz clock by either 15 or 17 instead of the normal 16 to keep the buffer from overflowing. When the device divides by either 15 or 17, it also sets the Jitter Attenuator Limit Trip (JALT) bit in the Receive Information Register (RIR.5).

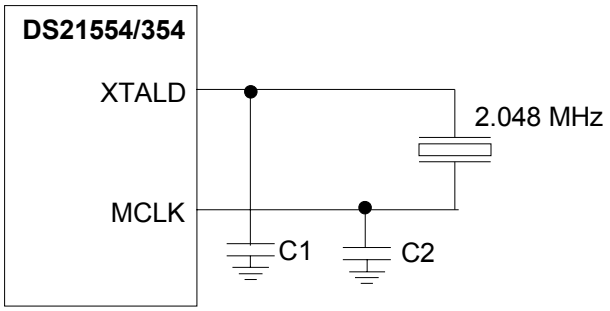
BASIC EXTERNAL ANALOG CONNECTIONS Figure 16-1



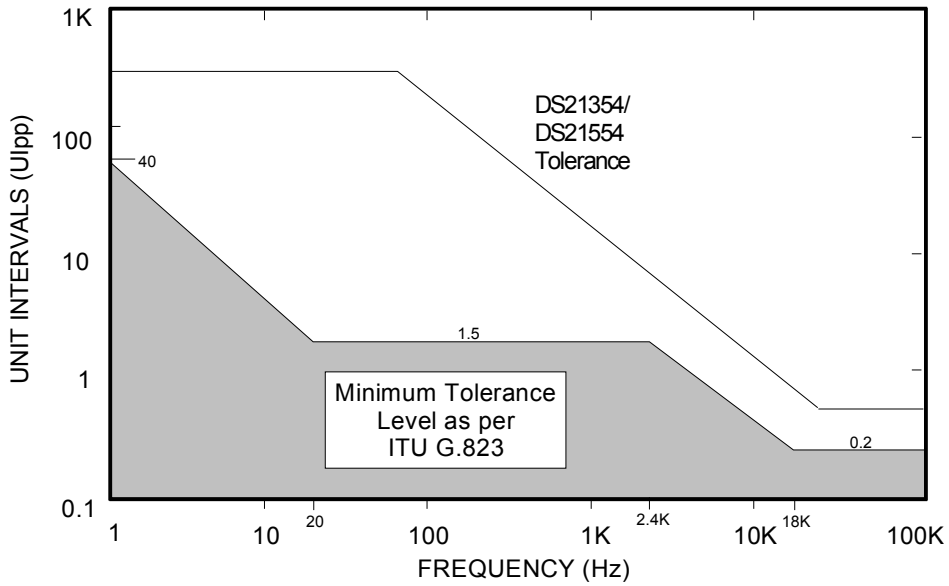
Notes:

All capacitors values are in uf.
10uf capacitor on TVDD is of tantalum construction.
See Table 16-1 and Table 16-2 for transformer selection.

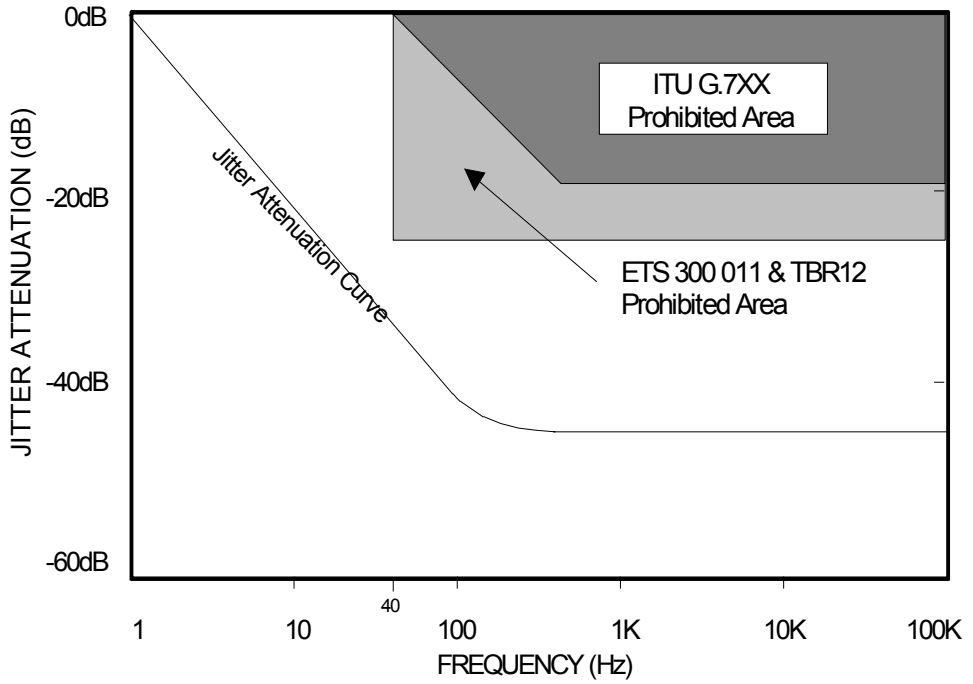
OPTIONAL CRYSTAL CONNECTION Figure 16-2



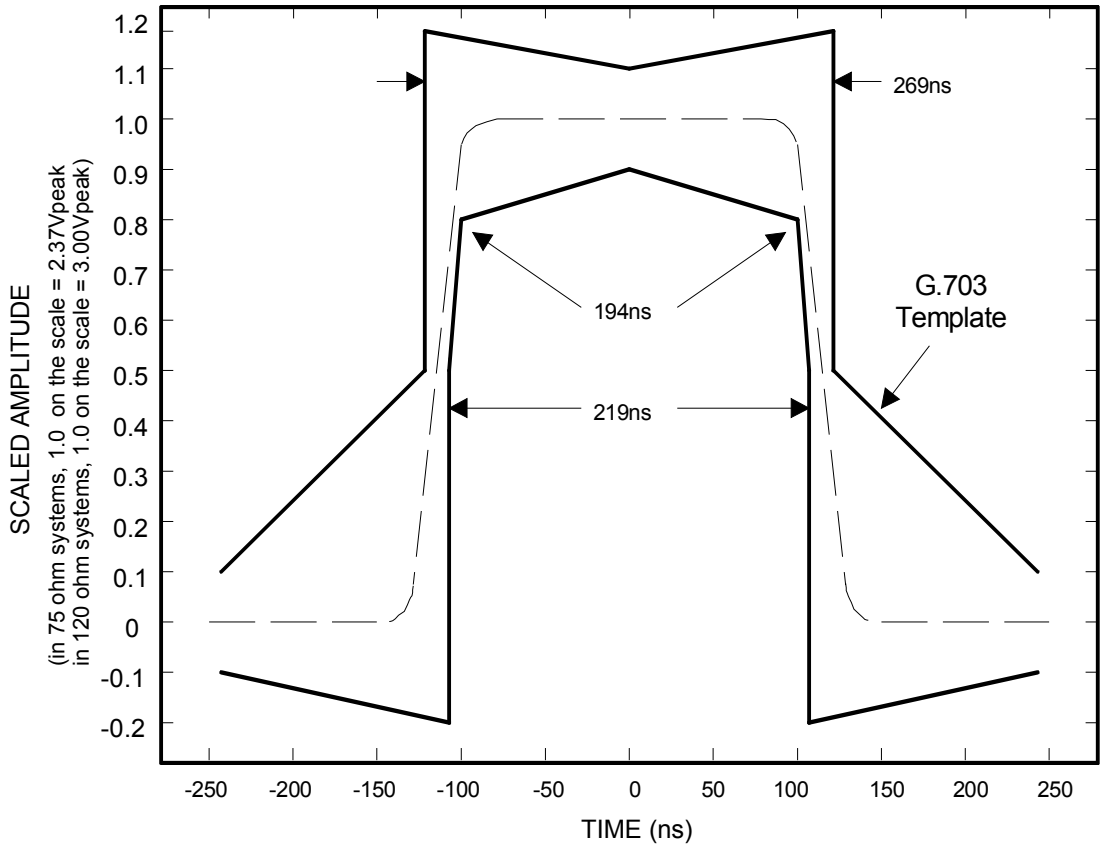
JITTER TOLERANCE Figure 16-3



JITTER ATTENUATION Figure 16-4



TRANSMIT WAVEFORM TEMPLATE Figure 16-5

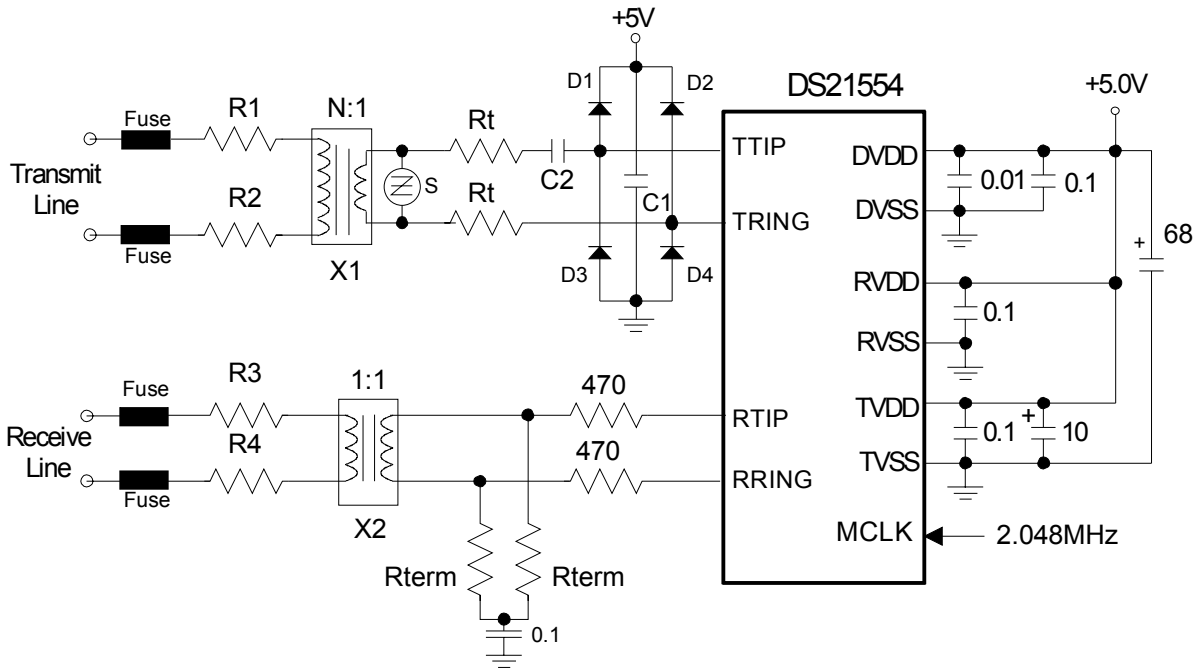


16.4 Protected Interfaces

In certain applications, such as connecting to the PSTN, it is required that the network interface be protected from and resistant to certain electrical conditions. These conditions are divided into two categories, surge and power line cross. A typical cause of surge is lightening strike. Power line cross refers to accidental contact with high voltage power wiring. For protection against surges, additional components and PCB layout considerations are required to reroute and dissipate this energy. In a surge event, the network interface must not be damaged and continue to work after the event. In the event of a power line contact, components such as fuses or PTCs that can "open" the circuit are required to prevent the possibility of a fire caused by overheating the transformer. The circuit examples in this data sheet are for "Secondary Over Voltage Protection" schemes for the line terminating equipment. Primary protection is typically provided by the network service provide and is external to the equipment.

Figure 16-6 shows an example circuit for the 5 volt device and Figure 16-7 is an example for the 3.3 volt device. In both examples, fuses are used to provide protection against power line cross. 470 ohm input resistors on the receive pair, a transient suppresser and a diode bridge on the transmit pair provide surge protection. Resistors R1 – R4 provide surge protection for the fuse. Careful selection of the transformer will allow the use of a fuse that requires no additional surge protection such as the circuit shown in Figure 16-7. The circuit shown in Figure 16-7 is required for 3.3 volt operation since additional resistance in the transmit pair cannot be tolerated. For more information on line interface design, consult the E1 Line Interface Design Criteria and Secondary Over Voltage Protection application notes. These application notes are available from Dallas Semiconductor's web site.

PROTECTED INTERFACE EXAMPLE FOR THE DS21554 Figure 16-6

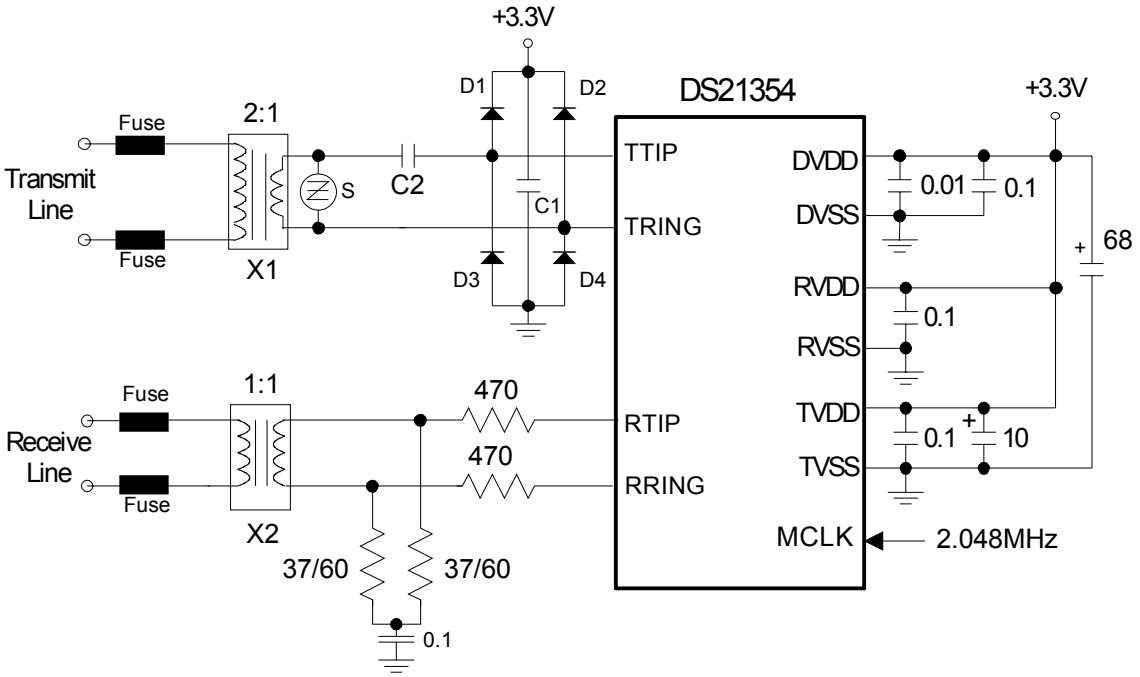


Note:

All capacitor values are in uf.
The 10uf capacitor on TVDD is of tantalum construction.
The 68uf cap is required to maintain VDD during a transient event.

COMPONET	DESCRIPTION
D1 – D4	Schottky Diode, International Rectifier 11DQ04
C1	0.1uf ceramic in parallel with 10uf tantalum
C2	.47 uf, non polarized ceramic construction
S	Semtech LC01-6, 6V low capacitance TVS
Fuse	For more information on the selection of these components see the separate application notes on **Secondary Over Voltage Protection** and **T1 Network Interface Design Criteria**. These applications notes are available from Dallas Semiconductor's Web site at www.dalsemi.com
Rt	
Rterm	
R1, R2, R3, R4	
X1	
X2	

PROTECTED INTERFACE EXAMPLE FOR THE DS21354 Figure 16-7



Note:

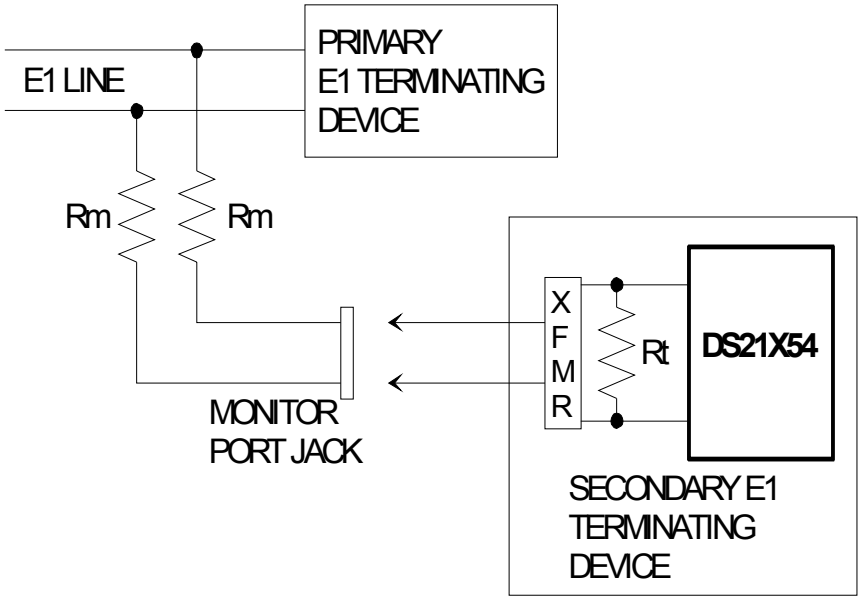
All capacitor values are in uf.
The 10uf capacitor on TVDD is of tantalum construction.
The 68uf cap is required to maintain VDD during a transient event.

COMPONENT	DESCRIPTION
D1 – D4	Schottky Diode, International Rectifier 11DQ04
C1	0.1uf ceramic in parallel with 10uf tantalum
C2	.47 uf, non polarized ceramic construction
Fuse	1.25A slo-blo, Littlefuse V2301.25
S	Semtech LC01-6, 6V low capacitance TVS
X1, X2	Transpower PT314, Low DCR

16.5 Receive Monitor Mode

When connecting to a monitor port a large resistive loss is incurred due to the voltage divider between the E1 line termination resistors (Rt) and the monitor port isolation resistors (Rm) as shown in the Figure 16-8. The receiver of the DS21354/554 can provide gain to overcome the resistive loss of a monitor connection. This is typically a purely resistive loss/gain and should not be confused with the cable loss characteristics of an E1 transmission line. Via the TEST3 register as shown in the table below, the receiver can be programmed to provide both 12dB and 30dB of gain.

TYPICAL MONITOR PORT APPLICATION Figure 16-8



RECEIVE MONITOR MODE GAIN Table 16-4

TEST3 (Address = AC Hex) Register Value	Gain
72 Hex	12dB
70 Hex	30dB

17 JTAG-BOUNDARY SCAN ARCHITECTURE AND TEST ACCESS PORT

17.1 Description

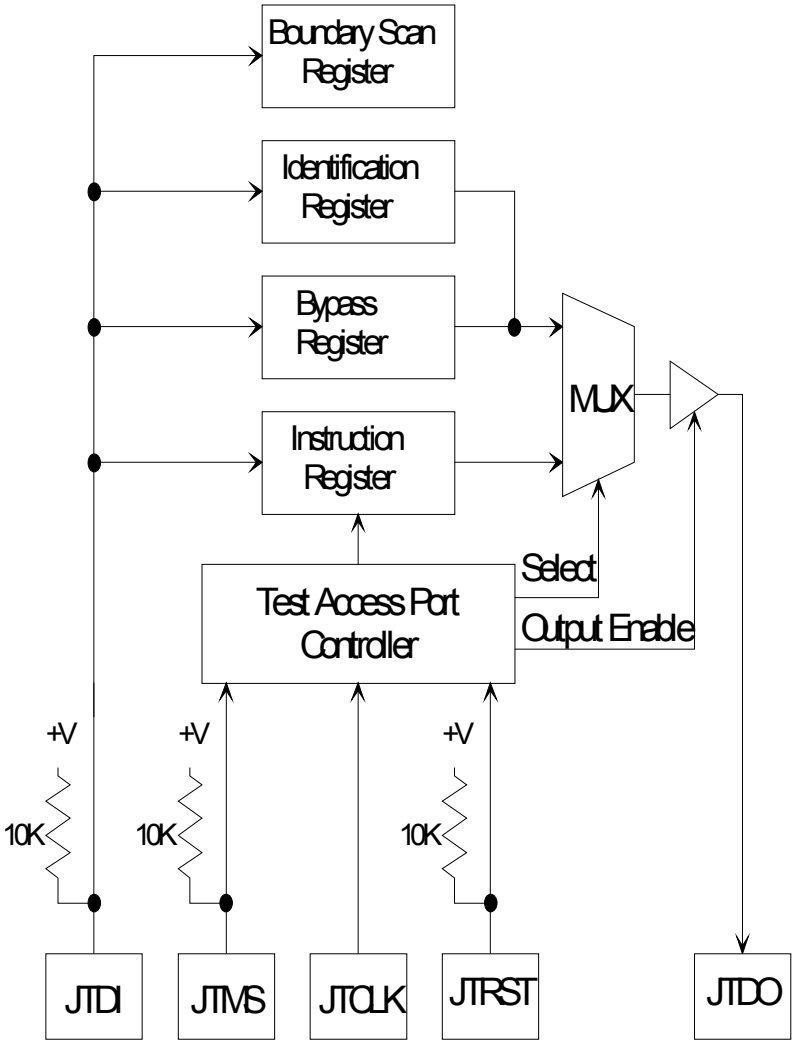
The DS21354/554 IEEE 1149.1 design supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. See Figure 17-1. The device contains the following as required by IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture.

Test Access Port (TAP)
TAP Controller
Instruction Register
Bypass Register
Boundary Scan Register
Device Identification Register

The DS21354/554 are enhanced versions of the DS2152 and are backward pin-compatible. The JTAG feature uses pins that had no function in the DS2152. When using the JTAG feature, be sure FMS (pin 76) is tied LOW enabling the newly defined pins of the DS21354/554. Details on Boundary Scan Architecture and the Test Access Port can be found in IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994.

The Test Access Port has the necessary interface pins; JTRST, JTCLK, JTMS, JTDI, and JTDO. See the pin descriptions for details.

JTAG FUNCTIONAL BLOCK DIAGRAM Figure 17-1



17.2 TAP Controller State Machine

The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK. See Figure 17-2.

Test-Logic-Reset

Upon power up, the TAP Controller will be in the Test-Logic-Reset state. The Instruction register will contain the IDCODE instruction. All system logic of the device will operate normally.

Run-Test-Idle

The Run-Test-Idle is used between scan operations or during specific tests. The Instruction register and test registers will remain idle.

Select-DR-Scan

All test registers retain their previous state. With JTMS LOW, a rising edge of JTCLK moves the controller into the Capture-DR state and will initiate a scan sequence. JTMS HIGH during a rising edge on JTCLK moves the controller to the Select-IR-Scan state.

Capture-DR

Data may be parallel-loaded into the test data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected register does not allow parallel loads, the test register will remain at its current value. On the rising edge of JTCLK, the controller will go to the Shift-DR state if JTMS is LOW or it will go to the Exit1-DR state if JTMS is HIGH.

Shift-DR

The test data register selected by the current instruction will be connected between JTDI and JTDO and will shift data one stage towards its serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it will maintain its previous state.

Exit1-DR

While in this state, a rising edge on JTCLK will put the controller in the Update-DR state, which terminates the scanning process, if JTMS is HIGH. A rising edge on JTCLK with JTMS LOW will put the controller in the Pause-DR state.

Pause-DR

Shifting of the test registers is halted while in this state. All test registers selected by the current instruction will retain their previous state. The controller will remain in this state while JTMS is LOW. A rising edge on JTCLK with JTMS HIGH will put the controller in the Exit2-DR state.

Exit2-DR

A rising edge on JTCLK with JTMS HIGH while in this state will put the controller in the Update-DR state and terminate the scanning process. A rising edge on JTCLK with JTMS LOW will enter the Shift-DR state.

Update-DR

A falling edge on JTCLK while in the Update-DR state will latch the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output due to changes in the shift register.

Select-IR-Scan

All test registers retain their previous state. The instruction register will remain unchanged during this state. With JTMS LOW, a rising edge on JTCLK moves the controller into the Capture-IR state and will initiate a scan sequence for the instruction register. JTMS HIGH during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

Capture-IR

The Capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is HIGH on the rising edge of JTCLK, the controller will enter the Exit1-IR state. If JTMS is LOW on the rising edge of JTCLK, the controller will enter the Shift-IR state.

Shift-IR

In this state, the shift register in the instruction register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK towards the serial output. The parallel register, as well as all test registers, remain at their previous states. A rising edge on JTCLK with JTMS HIGH will move the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS LOW will keep the controller in the Shift-IR state while moving data one stage thorough the instruction shift register.

Exit1-IR

A rising edge on JTCLK with JTMS LOW will put the controller in the Pause-IR state. If JTMS is HIGH on the rising edge of JTCLK, the controller will enter the Update-IR state and terminate the scanning process.

Pause-IR

Shifting of the instruction shift register is halted temporarily. With JTMS HIGH, a rising edge on JTCLK will put the controller in the Exit2-IR state. The controller will remain in the Pause-IR state if JTMS is LOW during a rising edge on JTCLK.

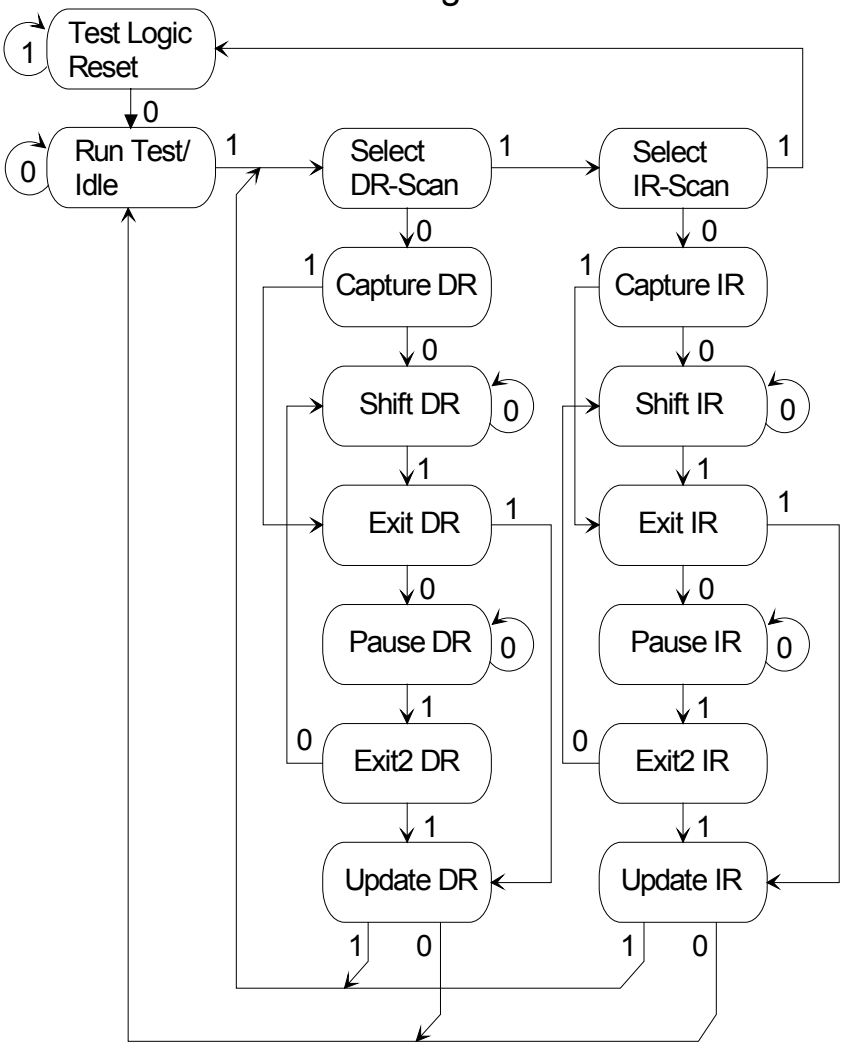
Exit2-IR

A rising edge on JTCLK with JTMS LOW will put the controller in the Update-IR state. The controller will loop back to Shift-IR if JTMS is HIGH during a rising edge of JTCLK in this state.

Update-IR

The instruction code shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS LOW, will put the controller in the Run-Test-Idle state. With JTMS HIGH, the controller will enter the Select-DR-Scan state.

TAP CONTROLLER STATE DIAGRAM Figure 17-2



17.3 Instruction Register

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register will be connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS LOW will shift the data one stage towards the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS HIGH will move the controller to the Update-IR state The falling edge of that same JTCLK will latch the data in the instruction shift register to the instruction parallel output. Instructions supported by the DS21354/554 with their respective operational binary codes are shown in Table 17-1.

INSTRUCTION CODES FOR IEEE 1149.1 ARCHITECTURE Table 17-1

Instruction	Selected Register	Instruction Codes
SAMPLE/PRELOAD	Boundary Scan	010
BYPASS	Bypass	111
EXTEST	Boundary Scan	000
CLAMP	Bypass	011
HIGHZ	Bypass	100
IDCODE	Device Identification	001

SAMPLE/PRELOAD

This is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. The digital I/Os of the device can be sampled at the boundary scan register without interfering with the normal operation of the device by using the Capture-DR state. SAMPLE/PRELOAD also allows the device to shift data into the boundary scan register via JTDI using the Shift-DR state.

BYPASS

When the BYPASS instruction is latched into the parallel instruction register, JTDI connects to JTDO through the one-bit bypass test register. This allows data to pass from JTDI to JTDO not affecting the device's normal operation.

EXTEST

This allows testing of all interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur. Once enabled via the Update-IR state, the parallel outputs of all digital output pins will be driven. The boundary scan register will be connected between JTDI and JTDO. The Capture-DR will sample all digital inputs into the boundary scan register.

CLAMP

All digital outputs of the device will output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs will not change during the CLAMP instruction.

HIGHZ

All digital outputs of the device will be placed in a high impedance state. The BYPASS register will be connected between JTDI and JTDO.

IDCODE

When the IDCODE instruction is latched into the parallel instruction register, the identification test register is selected. The device identification code will be loaded into the identification register on the rising edge of JTCLK following entry into the Capture-DR state. Shift-DR can be used to shift the identification code out serially via JTDO. During Test-Logic-Reset, the identification code is forced into the instruction register's parallel output. The ID code will always have a '1' in the LSB position. The next 11 bits identify the manufacturer's JEDEC number and number of continuation bytes followed by 16 bits for the device and 4 bits for the version. See Table 17-2. Table 17-3 lists the device ID codes for the SCT devices.

ID CODE STRUCTURE Table 17-2

MSB			**LSB**
Version Contact Factory	Device ID	JEDEC	1
4 bits	16bits	00010100001	1

DEVICE ID CODES Table 17-3

DEVICE	16-BIT ID
DS21354	0005h
DS21554	0003h
DS21352	0004h
DS21552	0002h

17.4 Test Registers

IEEE 1149.1 requires a minimum of two test registers; the bypass register and the boundary scan register. An optional test register has been included with the DS21354/554 design. This test register is the identification register and is used in conjunction with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

Boundary Scan Register

This register contains both a shift register path and a latched parallel output for all control cells and digital I/O cells and is n bits in length. See Table 17-4 for all of the cell bit locations and definitions.

Bypass Register

This is a single one-bit shift register used in conjunction with the BYPASS, CLAMP, and HIGHZ instructions which provides a short path between JTDI and JTDO.

Identification Register

The identification register contains a 32-bit shift register and a 32-bit latched parallel output. This register is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state. See Table 17-3 and Table 17-4 for more information on bit usage.

BOUNDARY SCAN CONTROL BITS Table 17-4

BIT	PIN	SYMBOL	TYPE	CONTROL BIT DESCRIPTION
2	1	RCHBLK	O	
	2	JTMS	I	
1	3	8MCLK	O	
	4	JTCLK	I	
	5	JTRST	I	
0	6	RCL	O	
	7	JTDI	I	
	8	N/C	–	
	9	N/C	–	
	10	JTDO	O	
72	11	BTS	I	
71	12	LIUC	I	
70	13	8XCLK	O	
69	14	TEST	I	
68	15	NC	–	
	16	RTIP	I	
	17	RRING	I	
	18	RVDD	–	
	19	RVSS	–	
	20	RVSS	–	
	21	MCLK	I	
	22	XTALD	O	
67	23	NC	–	
	24	RVSS	–	
66	25	INT	O	
	26	N/C	–	

BIT	PIN	SYMBOL	TYPE	CONTROL BIT DESCRIPTION
	27	N/C	–	
	28	N/C	–	
	29	TTIP	O	
	30	TVSS	–	
	31	TVDD	–	
	32	TRING	O	
65	33	TCHBLK	O	
64	34	TLCLK	O	
63	35	TLINK	I	
62	36	CI	I	
61	–	TSYNC.cntl	–	0 = TSYNC an input 1 = TSYNC an output
60	37	TSYNC	I/O	
59	38	TPOSI	I	
58	39	TNEGI	I	
57	40	TCLKI	I	
56	41	TCLKO	O	
55	42	TNEGO	O	
54	43	TPOSO	O	
	44	DVDD	–	
	45	DVSS	–	
53	46	TCLK	I	
52	47	TSER	I	
51	48	TSIG	I	
50	49	TESO	O	
49	50	TDATA	I	
48	51	TSYSCLK	I	
47	52	TSSYNC	I	
46	53	TCHCLK	O	
45	54	CO	O	
44	55	MUX	I	
43	–	BUS.cntl	–	0 = D0-D7/AD0-AD7 are inputs 1 = D0-D7/AD0-AD7 are outputs
42	56	D0/AD0	I/O	
41	57	D1/AD1	I/O	
40	58	D2/AD2	I/O	
39	59	D3/AD3	I/O	
	60	DVSS	–	
	61	DVDD	–	
38	62	D4/AD4	I/O	
37	63	D5/AD5	I/O	
36	64	D6/AD6	I/O	
35	65	D7/AD7	I/O	
34	66	A0	I	
33	67	A1	I	
32	68	A2	I	

BIT	PIN	SYMBOL	TYPE	CONTROL BIT DESCRIPTION
31	69	A3	I	
30	70	A4	I	
29	71	A5	I	
28	72	A6	I	
27	73	ALE(AS)/A7	I	
26	74	RD*(DS*)	I	
25	75	CS*	I	
24	76	FMS	I	
23	77	WR*(R/W*)	I	
22	78	RLINK	O	
21	79	RLCLK	O	
	80	DVSS	–	
	81	DVDD		
20	82	RCLK	O	
	83	DVDD	–	
	84	DVSS	–	
19	85	RDATA	O	
18	86	RPOSI	I	
17	87	RNEGI	I	
16	88	RCLKI	I	
15	89	RCLKO	O	
14	90	RNEGO	O	
13	91	RPOSO	O	
12	92	RCHCLK	O	
11	93	RSIGF	O	
10	94	RSIG	O	
9	95	RSER	O	
8	96	RMSYNC	O	
7	97	RFSYNC	O	
6	–	RSYNC.cntl	–	0 = RSYNC an input 1 = RSYNC an output
5	98	RSYNC	I/O	
4	99	RLOS/LOTC	O	
3	100	RSYSCLK	I	

18 INTERLEAVED PCM BUS OPERATION

In many architectures, the outputs of individual framers are combined into higher speed serial buses to simplify transport across the system. The DS21354/554 can be configured to allow data and signaling buses to be multiplexed into higher speed data and signaling buses eliminating external hardware saving board space and cost.

The interleaved PCM bus option (IBO) supports two bus speeds. The 4.096 MHz bus speed allows two SCTs to share a common bus. The 8.192 MHz bus speed allows four SCTs to share a common bus. See Figure 18-1 for an example of 4 devices sharing a common 8.192MHz PCM bus. Each SCT that shares a common bus must be configured through software and requires the use of one or two device pins. The elastic stores of each SCT must be enabled and configured for 2.048 MHz operation. See Figure 18-1 and Table 18-1.

For all bus configurations, one SCT will be configured as the master device and the remaining SCTs will be configured as slave devices. In the 4.096 MHz bus configuration there is one master and one slave. In the 8.192 MHz bus configuration there is one master and three slaves. Refer to the IBO register description for more detail.

IBO: INTERLEAVE BUS OPERATION REGISTER (Address = B5 Hex)

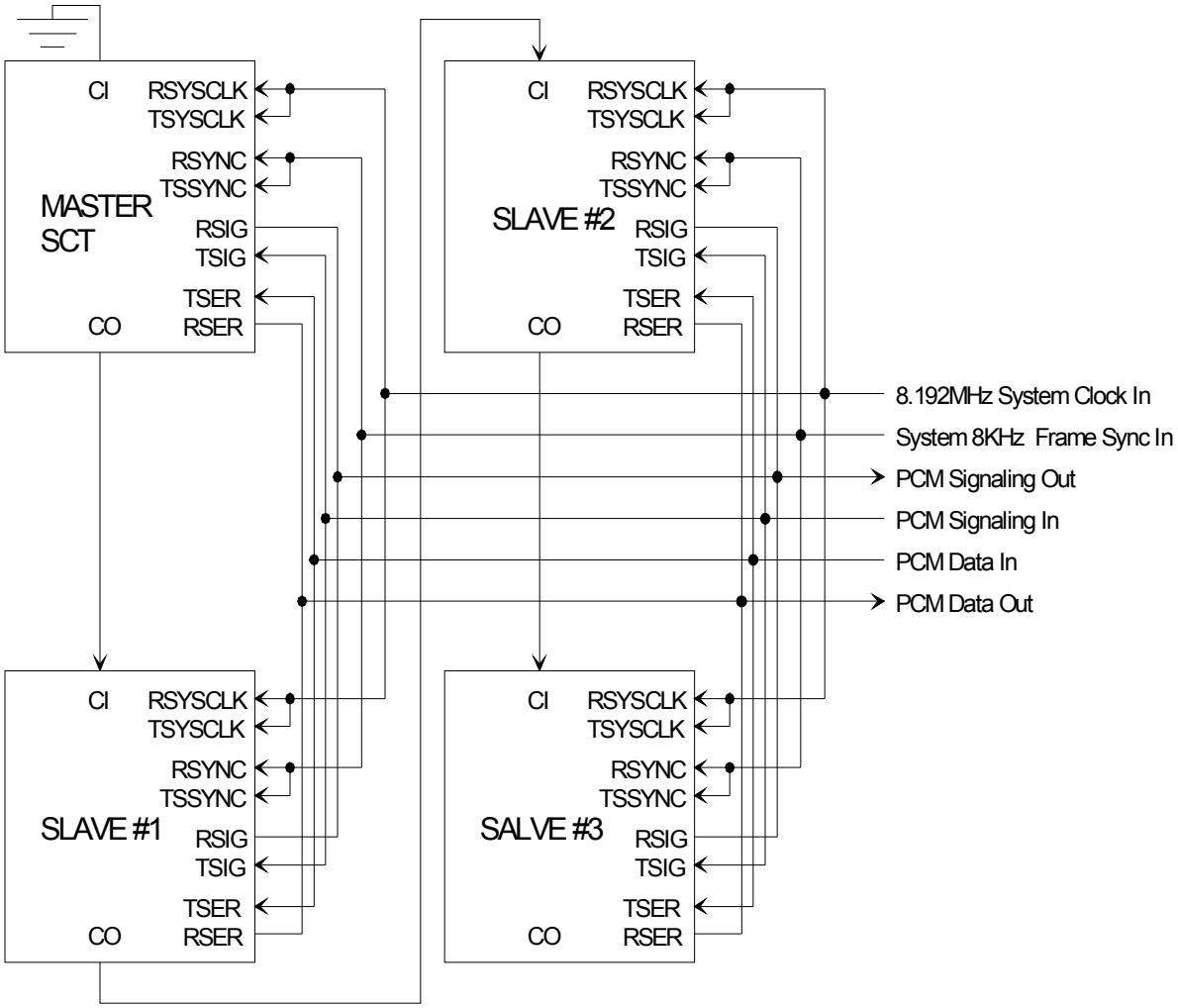
(MSB)							(LSB)
-	-	-	-	IBOEN	INTSEL	MSEL0	MSEL1

SYMBOL	POSITION	NAME AND DESCRIPTION
-	IBO.6	**Not Assigned**. Should be set to 0.
-	IBO.6	**Not Assigned.** Should be set to 0.
-	IBO.5	**Not Assigned**. Should be set to 0.
-	IBO.4	**Not Assigned**. Should be set to 0.
IBOEN	IBO.3	**Interleave Bus Operation Enable** 0 = Interleave Bus Operation disabled. 1 = Interleave Bus Operation enabled.
INTSEL	IBO.2	**Interleave Type Select** 0 = Byte interleave. 1 = Frame interleave.
MSEL0	IBO.1	**Master Device Bus Select Bit 0** See Table 18-1.
MSEL1	IBO.0	**Master Device Bus Select Bit 1** See Table 18-1.

IBO MASTER DEVICE SELECT Table 18-1

MSEL1	MSEL0	Function
0	0	Slave device.
0	1	Master device with 1 slave device (4.096 MHz bus rate)
1	0	Master device with 3 slave devices (8.192 MHz bus rate)
1	1	Reserved

IBO BASIC CONFIGURATION USING 4 SCTS Figure 18-1



18.1 Channel Interleave

In channel interleave mode data is output to the PCM Data Out bus one channel at a time from each of the connected SCTs until all channels of frame n from all each SCT has been place on the bus. This mode can be used even when the connected SCTs are operating asynchronous to each other. The elastic stores will manage slip conditions. See Figure 19-11 and Figure 19-5 for details.

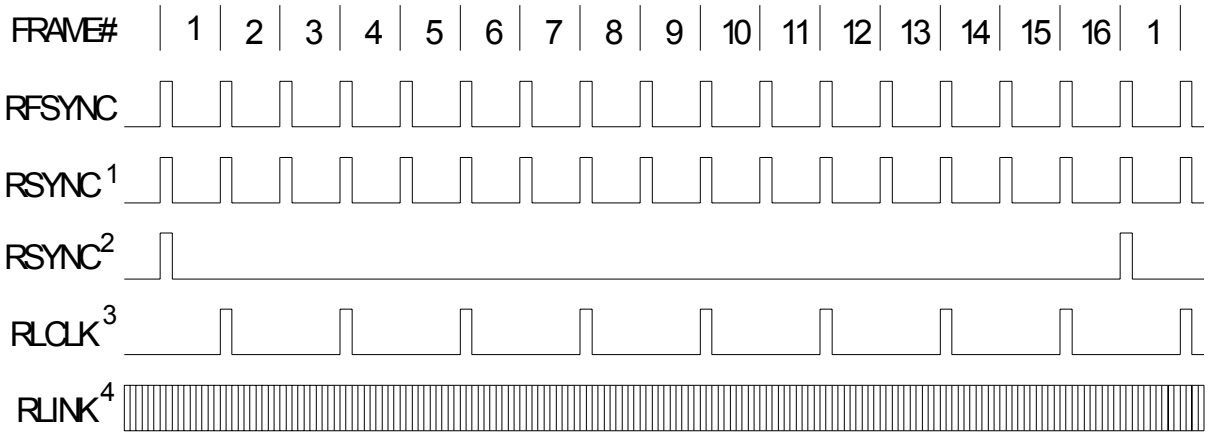
18.2 Frame Interleave

In frame interleave mode data is output to the PCM Data Out bus one frame at a time from each of the connected SCTs. This mode is used only when all connected SCTs are synchronous. In this mode, slip conditions are not allowed. See Figure 19-2 and Figure 19-6 for details.

19 FUNCTIONAL TIMING DIAGRAMS

19.1 Receive

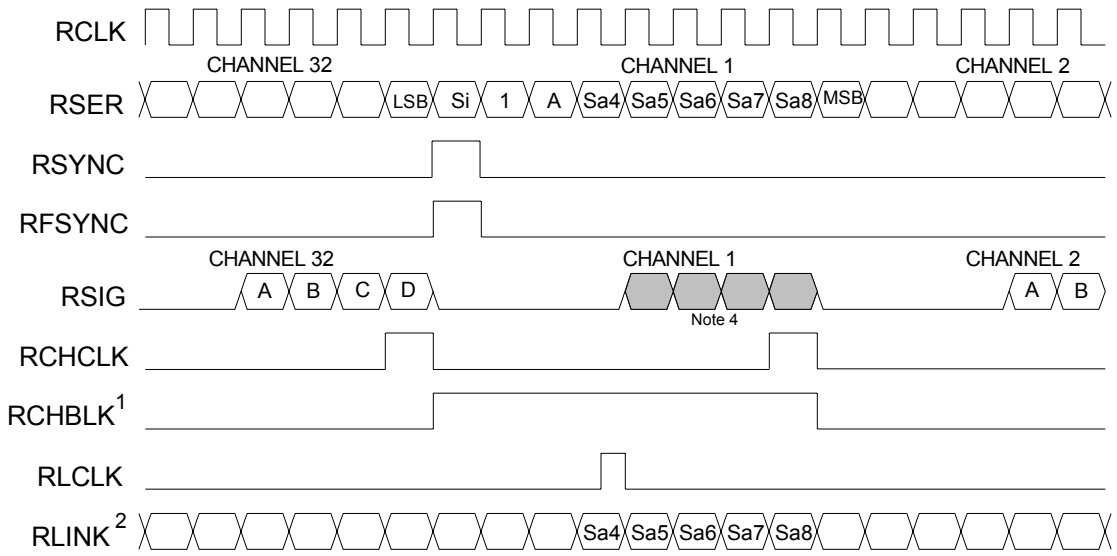
RECEIVE SIDE TIMING Figure 19-1



Notes:

1. RSYNC in frame mode (RCR1.6 = 0)
2. RSYNC in multiframe mode (RCR1.6 = 1)
3. RLCLK is programmed to output just the Sa bits
4. RLINK will always output all 5 Sa bits as well as the rest of the receive data stream
5. This diagram assumes the CAS MF begins in the RAF frame

RECEIVE SIDE BOUNDARY TIMING (with elastic store disabled) Figure 19-2

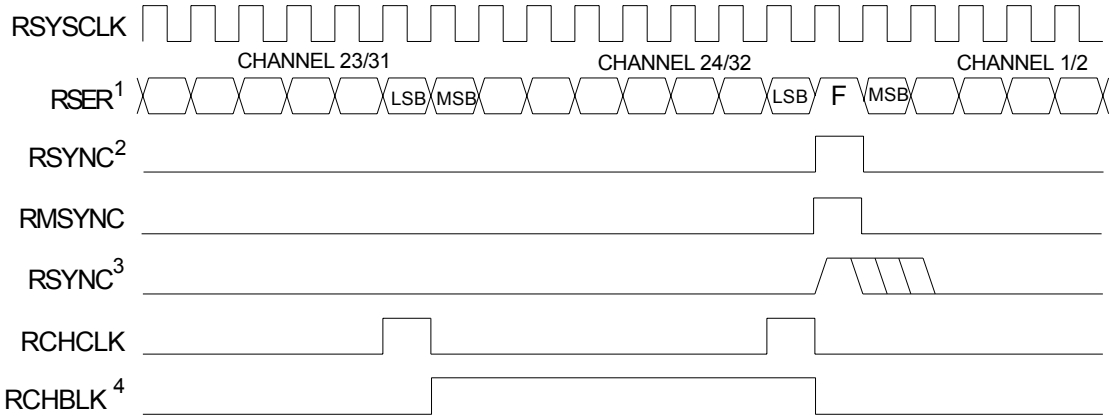


Notes:

1. RCHBLK is programmed to block channel 1
2. RLCLK is programmed to mark the Sa4 bit in RLINK
3. Shown isa RNAF frame boundary
4. RSIG normally contains the CAS multiframe alignment nibble (0000) in channel 1

RECEIVE SIDE 1.544 MHz BOUNDARY TIMING (with elastic store enabled)

Figure 19-3

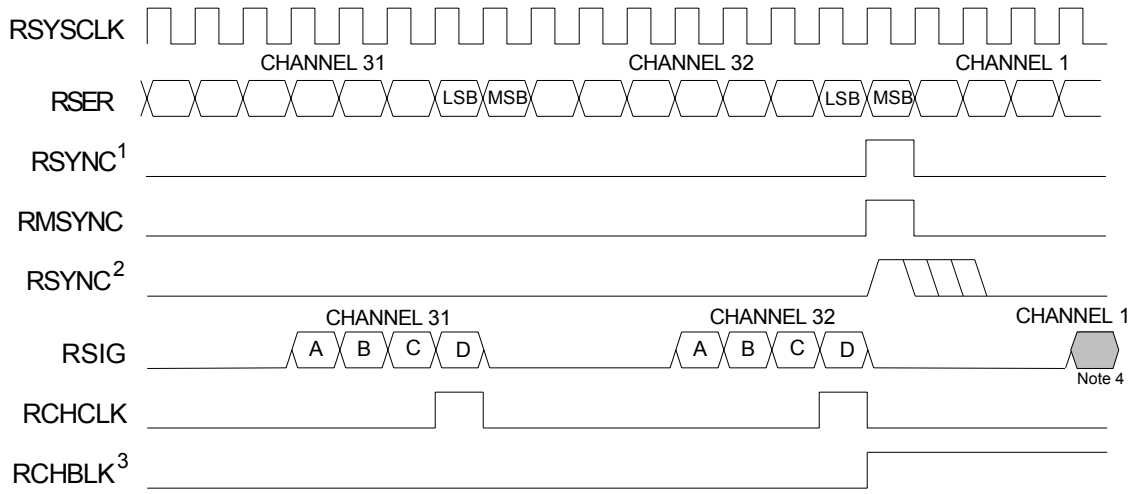


Notes:

1. Data from the E1 channels 1. 5. 9, 13, 17, 21, 25, and 29 is dropped (channel 2 from the E1 link is (mapped to channel 1 of the T1 link, etc.) and the F-bit position is added (forced to on1)
2. RSYNC in the output mode (RCR1.5 = 0)
3. RSYNC in the input mode (RCR1.5 = 1)
4. RCHBLK is programmed to block channel 24

RECEIVE SIDE 2.048 MHz BOUNDARY TIMING (with elastic store enabled)

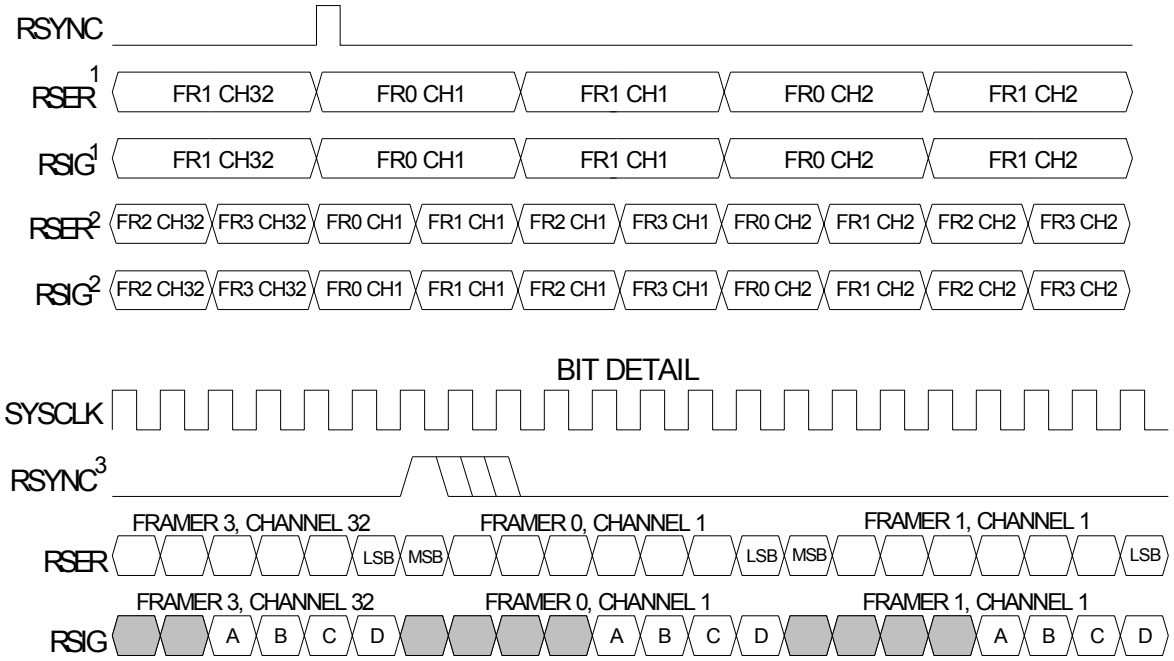
Figure 19-4



Notes:

1. RSYNC is in the output mode (RCR1.5 = 0)
2. RSYNC is in the input mode (RCR1.5 = 1)
3. RCHBLK is programmed to block channel 1
4. RSIG normally contains the CAS multiframe alignment nibble (0000) in Channel 1

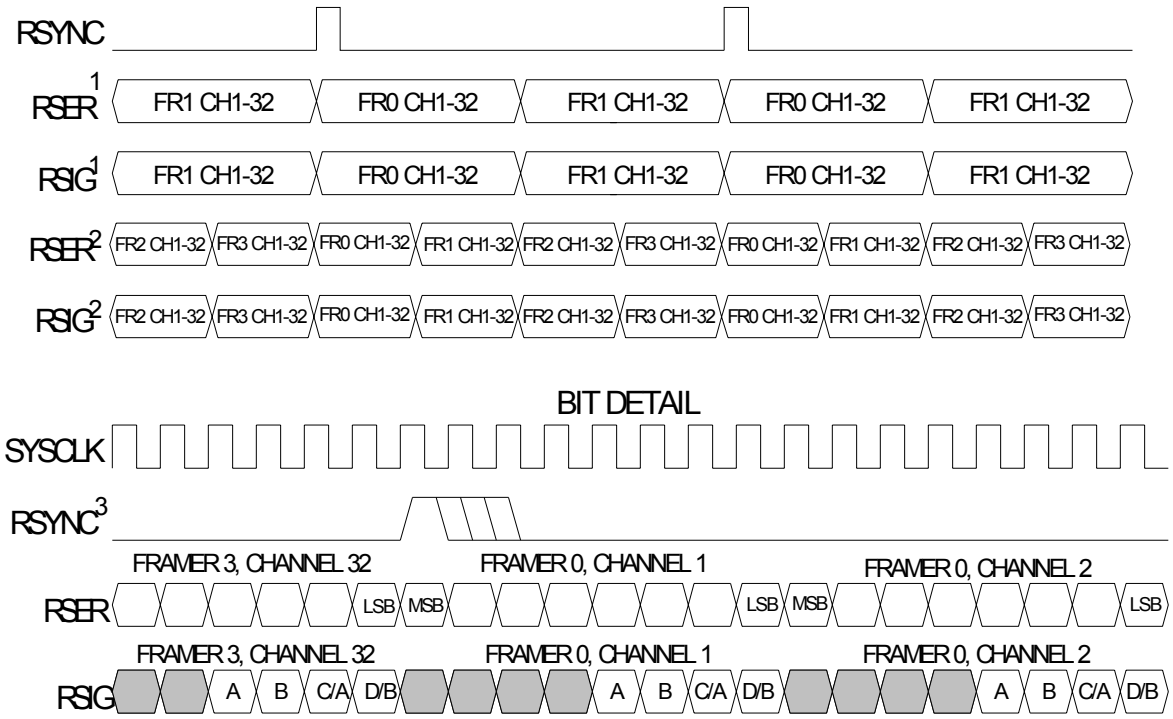
RECEIVE SIDE INTERLEAVE BUS OPERATION, BYTE MODE Figure 19-5



Notes:

1. 4.096 MHz bus configuration.
2. 8.192 MHz bus configuration.
3. RSYNC is in the input mode (RCR1.5 = 0).

RECEIVE SIDE INTERLEAVE BUS OPERATION, FRAME MODE Figure 19-6

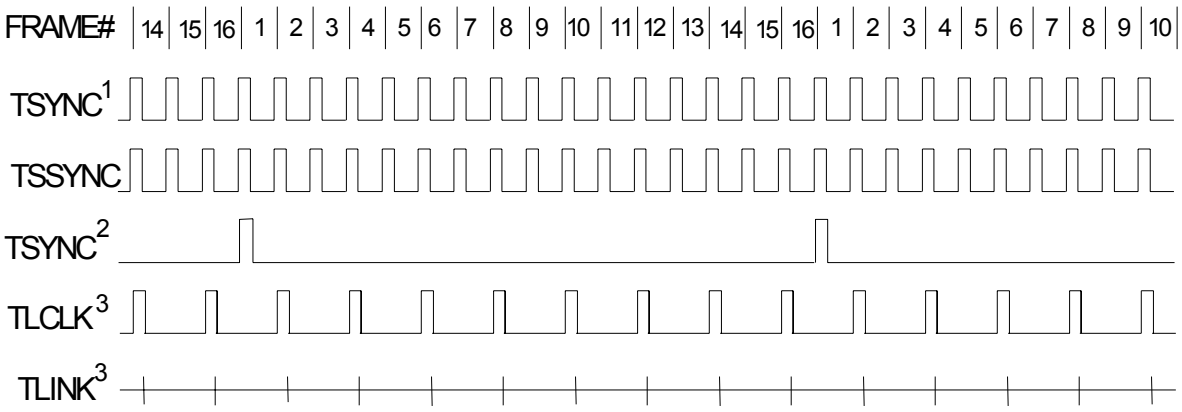


Notes:

1. 4.096 MHz bus configuration.
2. 8.192 MHz bus configuration.
3. RSYNC is in the input mode (RCR1.5 = 0).

19.2 Transmit

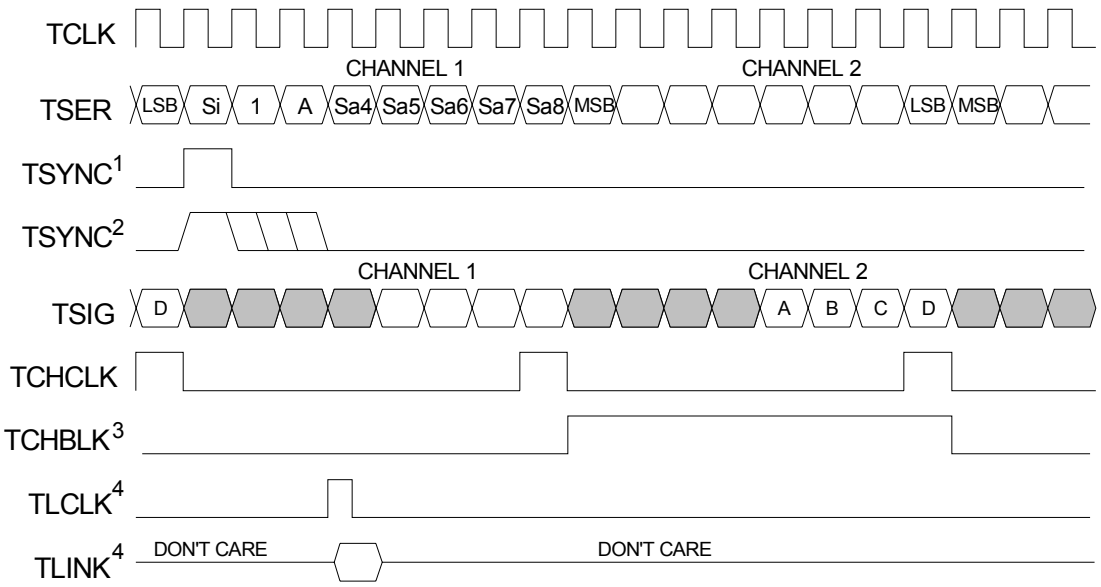
TRANSMIT SIDE TIMING Figure 19-7



Notes:

1. TSYNC in frame mode (TCR1.1 = 0)
2. TSYNC in multiframe mode (TCR1.1 = 1)
3. TLINK is programmed to source just the Sa4 bit
4. This diagram assumes both the CAS MF and the CRC4 MF begin with the TAF frame
5. TLINK and TLCLK are not synchronous with TSSYNC

TRANSMIT SIDE BOUNDARY TIMING (with elastic store disabled) Figure 19-8

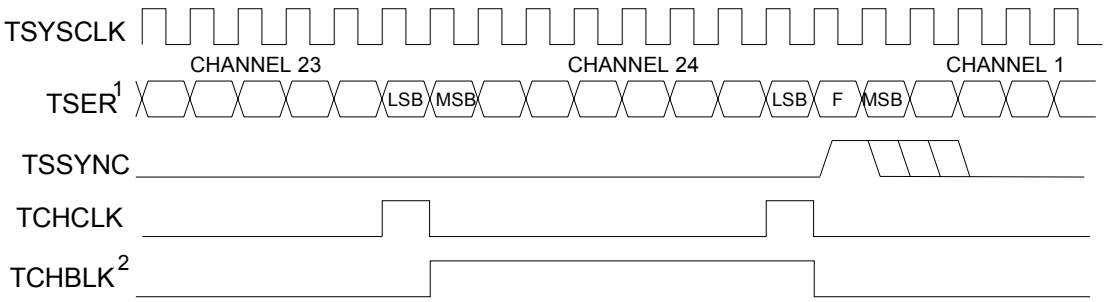


Notes:

1. TSYNC is in the output mode (TCR1.0 = 1)
2. TSYNC is in the input mode (TCR1.0 = 0)
3. TCHBLK is programmed to block channel 2
4. TLINK is programmed to source the Sa4 bit
5. The signaling data at TSIG during channel 1 is normally overwritten in the transmit formatter with the CAS MF alignment nibble (0000)
6. Shown is a TNAF frame boundary

TRANSMIT SIDE 1.544 MHz BOUNDARY TIMING (with elastic store enabled)

Figure 19-9

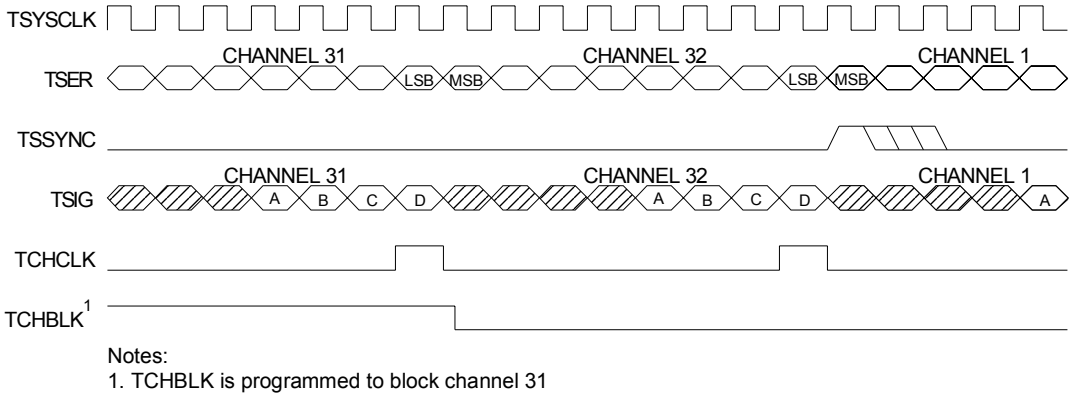


Notes:

1. The F bit position in the TSER data is ignored
2. TCHBLK is programmed to block channel 24

TRANSMIT SIDE 2.048 MHz BOUNDARY TIMING (with elastic store enabled)

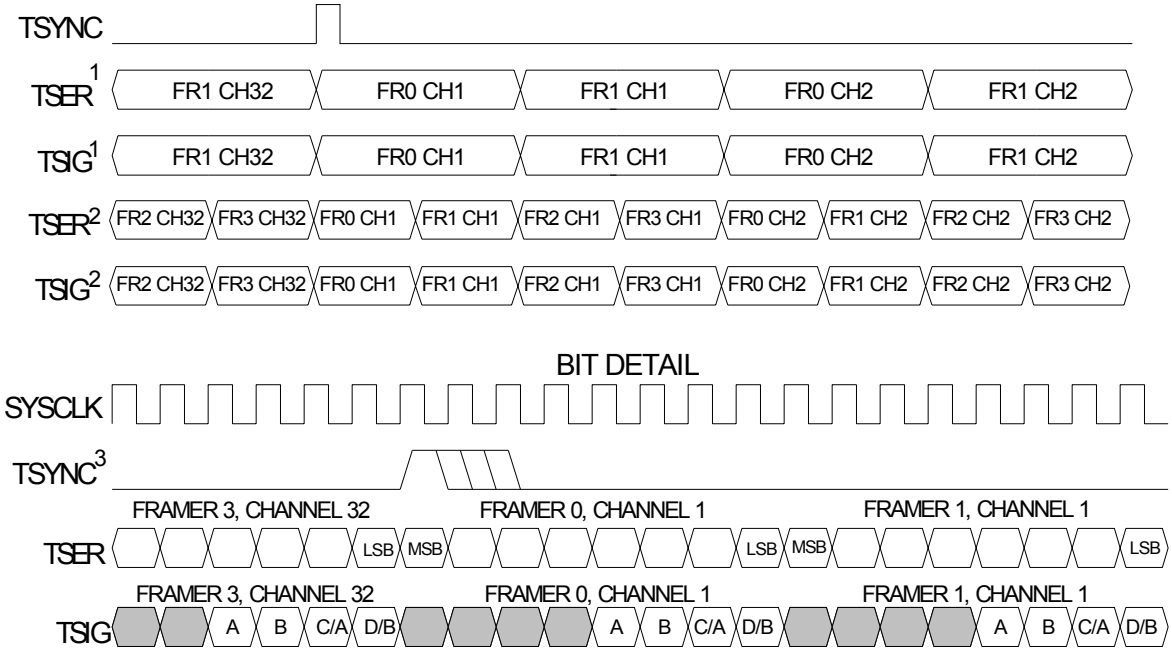
Figure 19-10



Notes:

1. TCHBLK is programmed to block channel 31

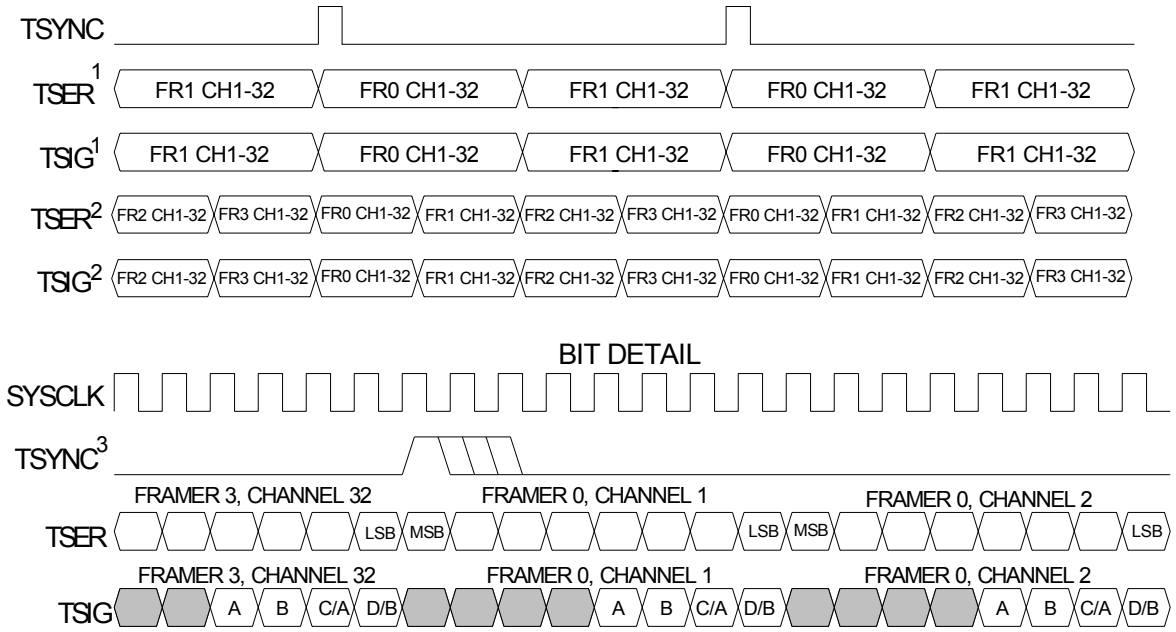
TRANSMIT SIDE INTERLEAVE BUS OPERATION, BYTE MODE Figure 19-11



Notes:

1. 4.096 MHz bus configuration.
2. 8.192 MHz bus configuration.
3. TSYNC is in the input mode (TCR1.0 = 0).

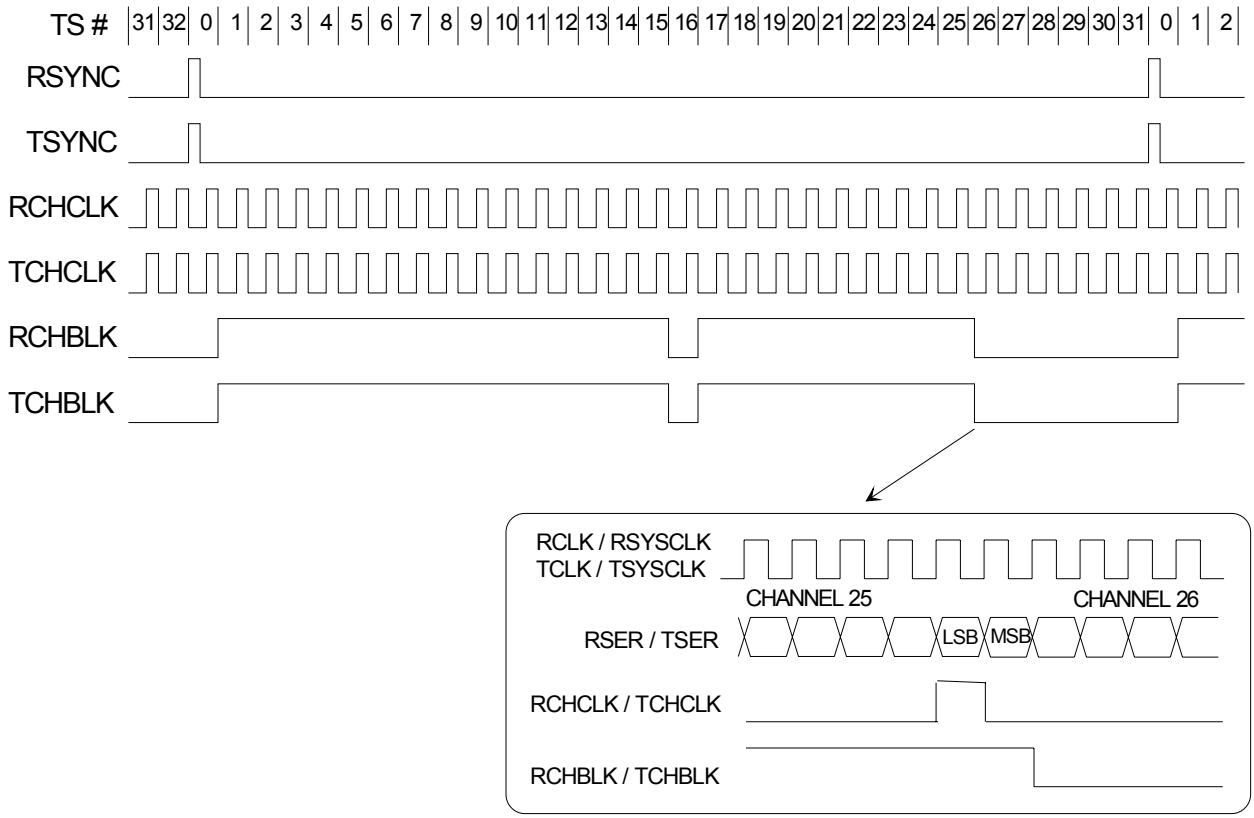
TRANSMIT SIDE INTERLEAVE BUS OPERATION, FRAME MODE Figure 19-12



NOTES:

1. 4.096 MHz bus configuration.
2. 8.192 MHz bus configuration.
3. TSYNC is in the input mode (TCR1.0 = 0).

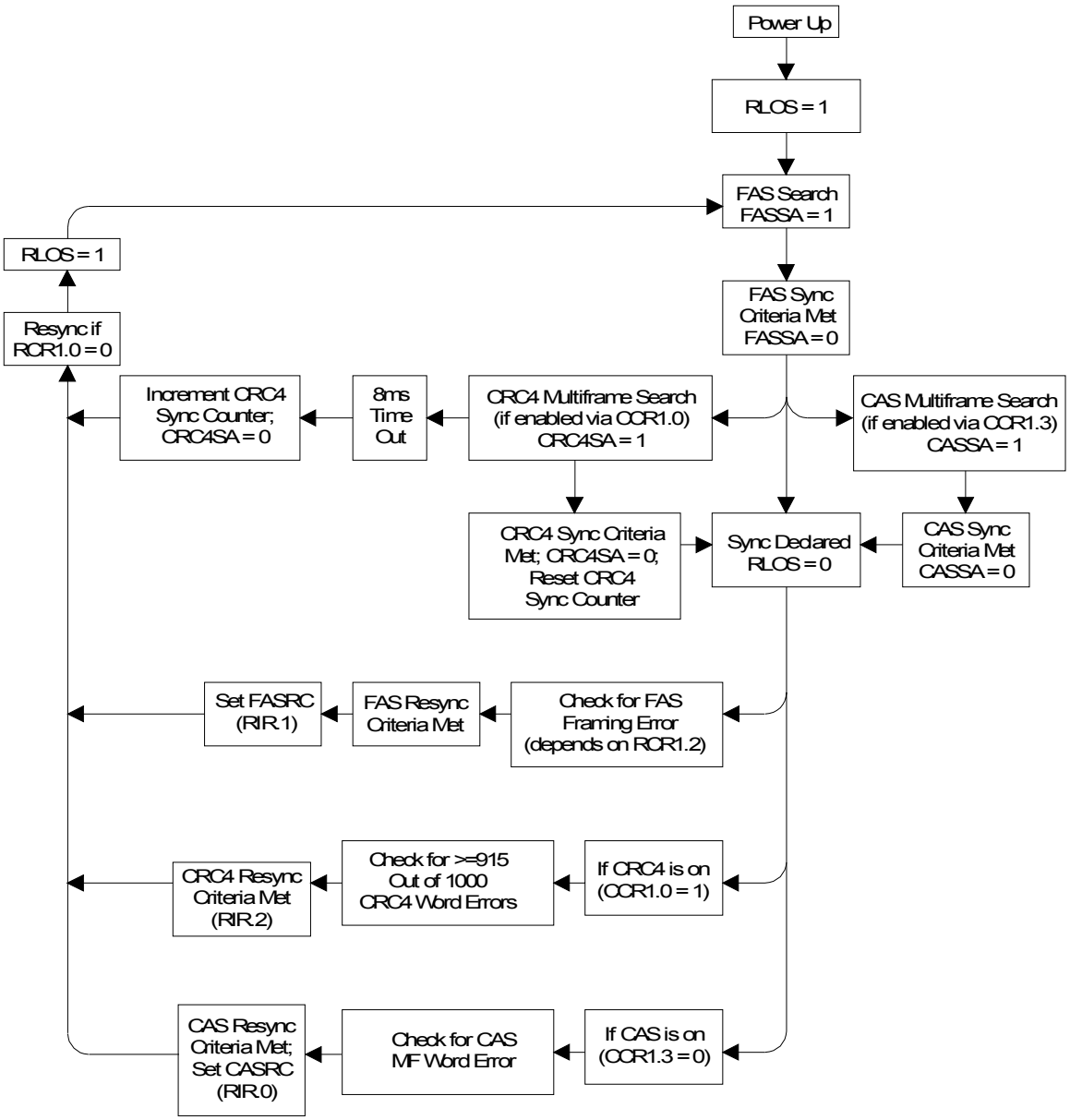
G.802 TIMING Figure 19-13



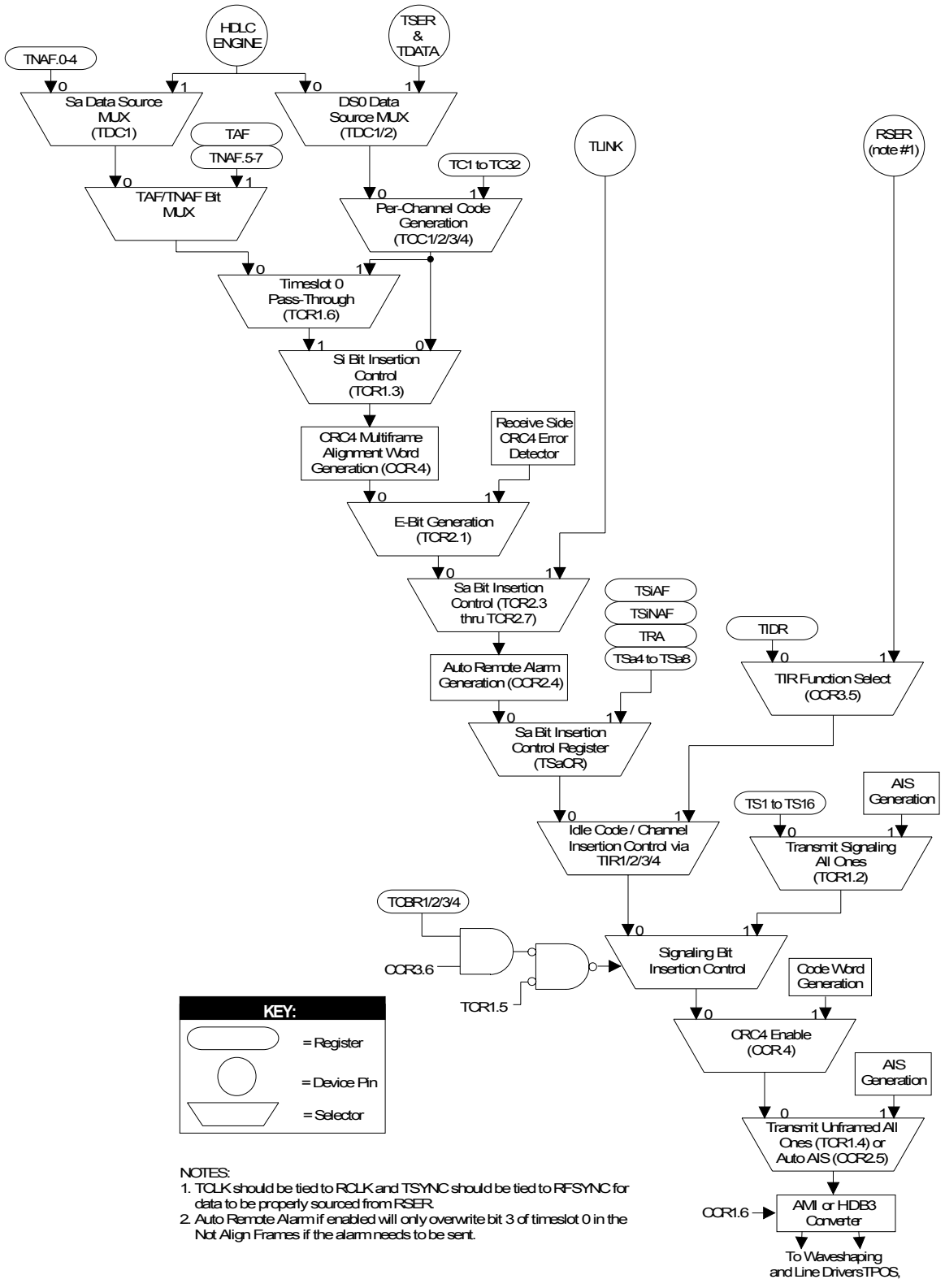
NOTES:

1. RCHBLK or TCHBLK programmed to pulse high during timeslots 1 through 15, 17 through 25, and bit 1 of timeslot 26

DS21354/554 FRAMER SYNCHRONIZATION FLOWCHART Figure 19-14



DS21354/554 TRANSMIT DATA FLOW Figure 19-15



NOTES:
1. TCLK should be tied to RCLK and TSYNC should be tied to RFSYNC for data to be properly sourced from RSER.
2. Auto Remote Alarm if enabled will only overwrite bit 3 of timeslot 0 in the Not Align Frames if the alarm needs to be sent.

20 OPERATING PARAMETERS

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to +6.0V
Operating Temperature for DS21354L / DS21554L	0°C to 70°C
Operating Temperature for DS21354LN / DS21554LN	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	See J-STD-020A Specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C; V_{DD} = 3.3V ± 5% for DS21354L;
0°C to 70°C; V_{DD} = 5.0V ± 5% for DS21554L;
-40°C to +85°C; V_{DD} = 3.3V ± 5% for DS21354LN;
-40°C to +85°C; V_{DD} = 5.0V ± 5% for DS21554LN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		5.5	V	
Logic 0	V_{IL}	–0.3		+0.8	V	
Supply for DS21354	V_{DD}	3.135	3.3	3.465	V	1
Supply for DS21554	V_{DD}	4.75	5	5.25	V	1

CAPACITANCE

(t_A =25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output Capacitance	C_{OUT}		7		pF	

DC CHARACTERISTICS

(0°C to 70°C; V_{DD} = 3.3V ± 5% for DS21354L;
0°C to 70°C; V_{DD} = 5.0V ± 5% for DS21554L;
-40°C to +85°C; V_{DD} = 3.3V ± 5% for DS21354LN;
-40°C to +85°C; V_{DD} = 5.0V ± 5% for DS21554LN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current @ 5V	I_{DD}		75		mA	2
Supply Current @ 3.3V	I_{DD}		75		mA	2
Input Leakage	I_{IL}	–1.0		+1.0	µA	3
Output Leakage	I_{LO}			1.0	µA	4
Output Current (2.4V)	I_{OH}	–1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:
1. Applies to RVDD, TVDD, and DVDD.
2. TCLK = TCLKI = RCLKI = TSYSCLK = RSYSCLK = MCLK = 2.048 MHz; outputs open circuited.
3. $0.0V < V_{IN} < V_{DD}$.
4. Applied to INT* when 3–stated.

21 AC TIMING PARAMETERS AND DIAGRAMS

21.1 Multiplexed Bus AC Characteristics

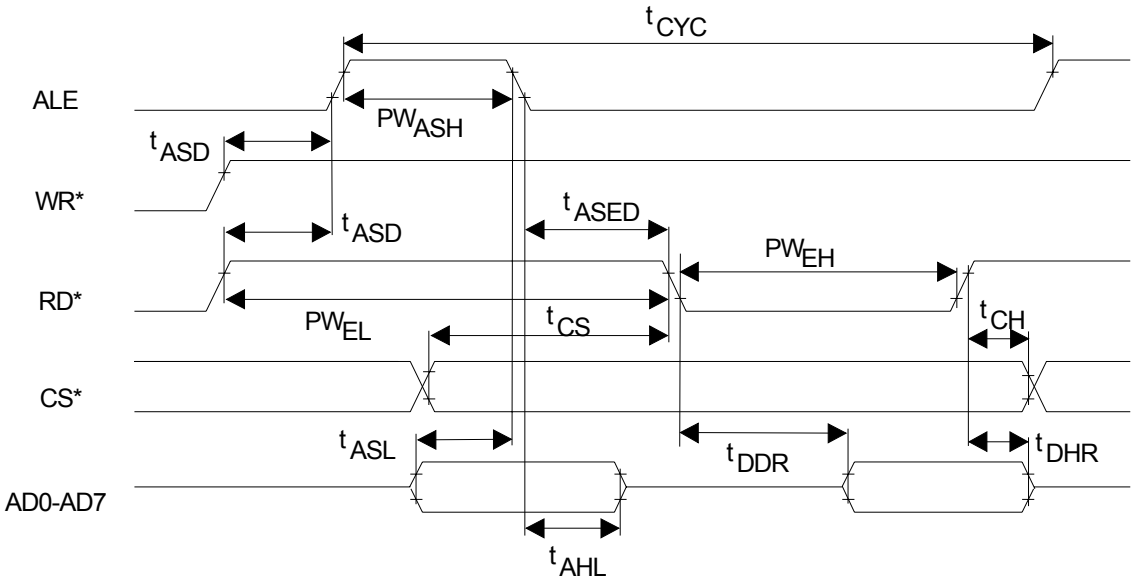
AC CHARACTERISTICS – MULTIPLEXED PARALLEL PORT (MUX = 1)

[See Figure 21-1 to Figure 21-3]

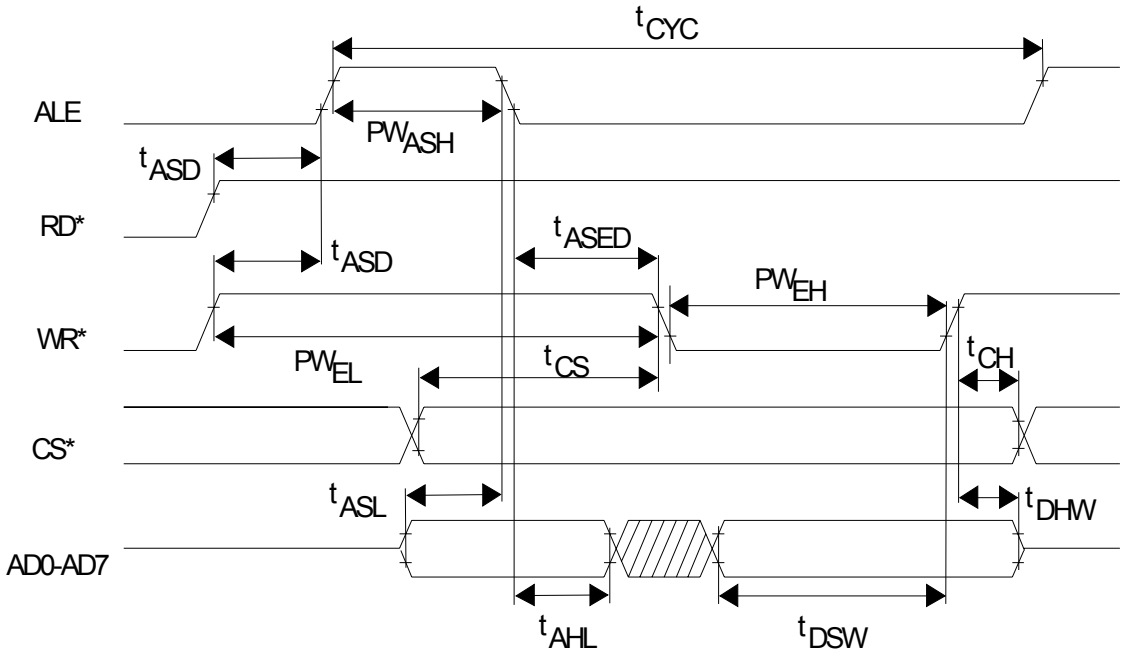
(0°C to 70°C; V_{DD} = 3.3V ± 5% for DS21354L;
0°C to 70°C; V_{DD} = 5.0V ± 5% for DS21554L;
-40°C to +85°C; V_{DD} = 3.3V ± 5% for DS21354LN;
-40°C to +85°C; V_{DD} = 5.0V ± 5% for DS21554LN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	200			ns	
Pulse Width, DS low or RD* high	PW_{EL}	100			ns	
Pulse Width, DS high or RD* low	PW_{EH}	100			ns	
Input Rise/Fall times	t_R , t_F			20	ns	
R/W* Hold Time	t_{RWH}	10			ns	
R/W* Set Up time before DS high	t_{RWS}	50			ns	
CS* Set Up time before DS, WR* or RD* active	t_{CS}	20			ns	
CS* Hold time	t_{CH}	0			ns	
Read Data Hold time	t_{DHR}	10		50	ns	
Write Data Hold time	t_{DHW}	0			ns	
Muxed Address valid to AS or ALE fall	t_{ASL}	15			ns	
Muxed Address Hold time	t_{AHL}	10			ns	
Delay time DS, WR* or RD* to AS or ALE rise	t_{ASD}	20			ns	
Pulse Width AS or ALE high	PW_{ASH}	30			ns	
Delay time, AS or ALE to DS, WR* or RD*	t_{ASED}	10			ns	
Output Data Delay time from DS or RD*	t_{DDR}	20		80	ns	
Data Set Up time	t_{DSW}	50			ns	

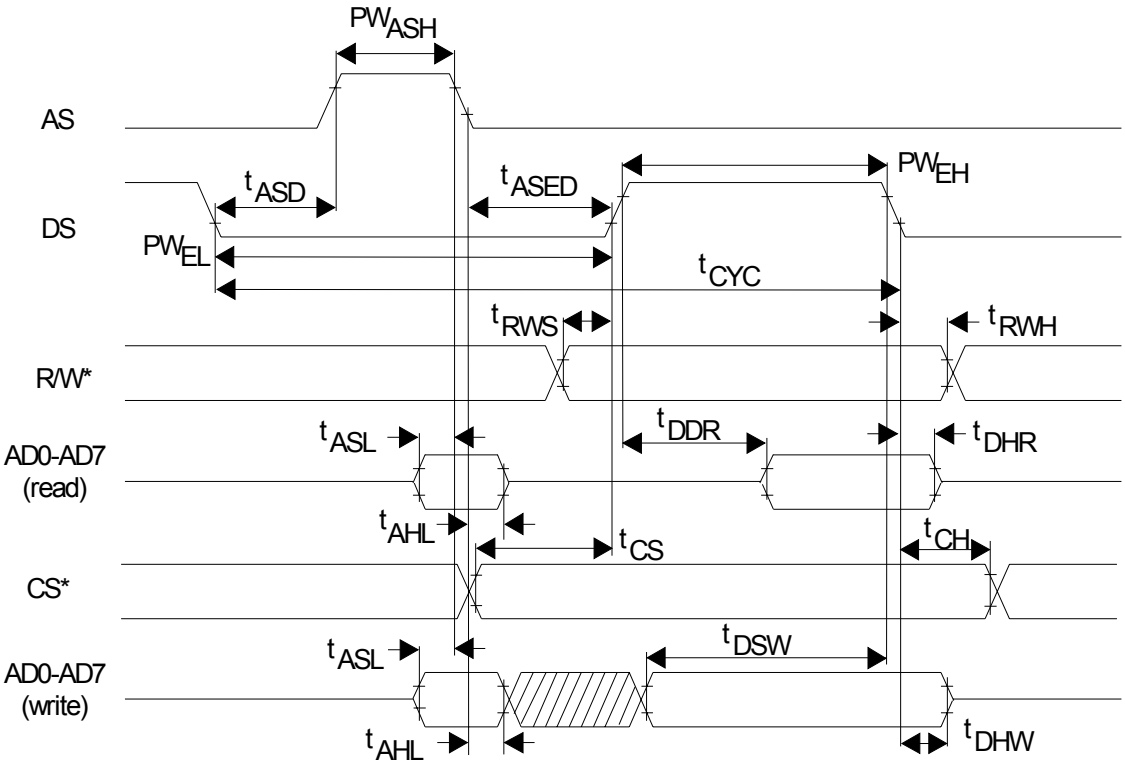
INTEL BUS READ AC TIMING (BTS=0 / MUX = 1) Figure 21-1



INTEL BUS WRITE TIMING (BTS=0 / MUX=1) Figure 21-2



MOTOROLA BUS AC TIMING (BTS = 1 / MUX = 1) Figure 21-3



21.2 Non-Multiplexed Bus AC Characteristics

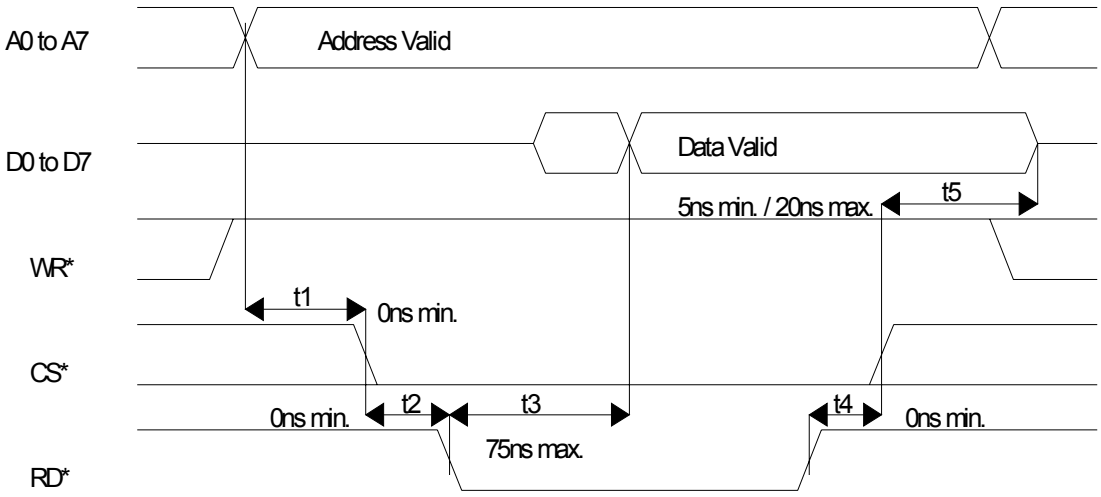
AC CHARACTERISTICS – NON-MULTIPLEXED PARALLEL PORT (MUX = 0)

[See Figure 21-4 to Figure 21-7]

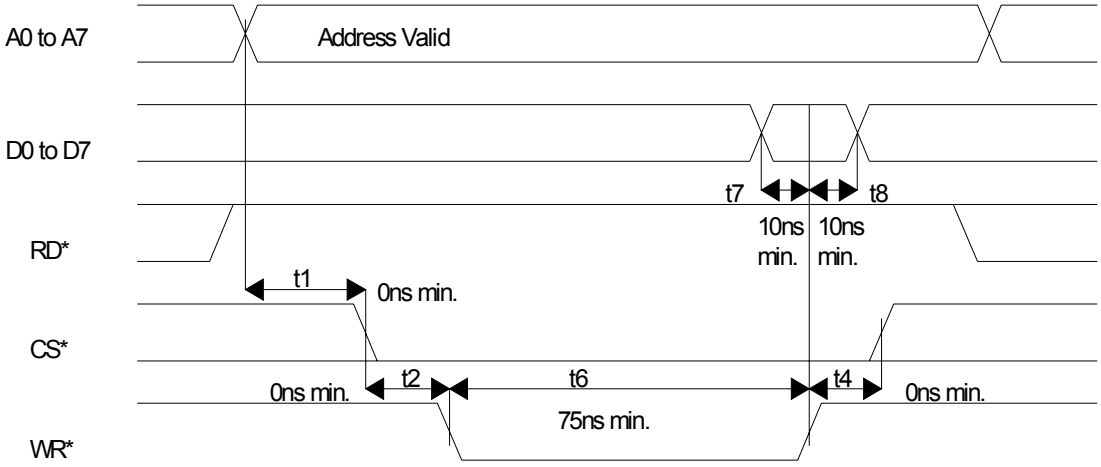
(0°C to 70°C; V_{DD} = 3.3V ± 5% for DS21354L;
0°C to 70°C; V_{DD} = 5.0V ± 5% for DS21554L;
-40°C to +85°C; V_{DD} = 3.3V ± 5% for DS21354LN;
-40°C to +85°C; V_{DD} = 5.0V ± 5% for DS21554LN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Set Up Time for A0 to A7, Valid to CS* Active	t1	0			ns	
Set Up Time for CS* Active to either RD*, WR*, or DS* Active	t2	0			ns	
Delay Time from either RD* or DS* Active to Data Valid	t3			75	ns	
Hold Time from either RD*, WR*, or DS* Inactive to CS* Inactive	t4	0			ns	
Hold Time from CS* Inactive to Data Bus 3–state	t5	5		20	ns	
Wait Time from either WR* or DS* Active to Latch Data	t6	75			ns	
Data Set Up Time to either WR* or DS* Inactive	t7	10			ns	
Data Hold Time from either WR* or DS* Inactive	t8	10			ns	
Address Hold from either WR* or DS* inactive	t9	10			ns	

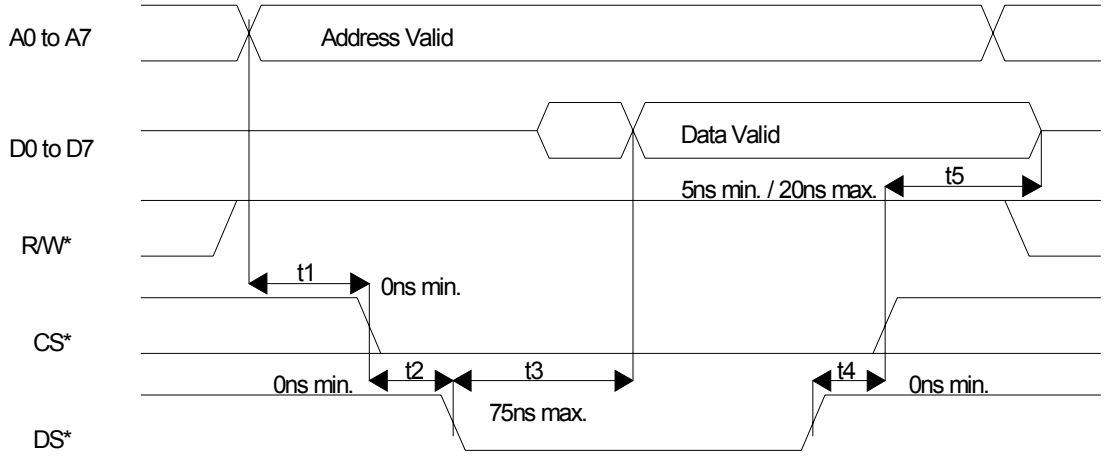
INTEL BUS READ AC TIMING (BTS=0 / MUX=0) Figure 21-4



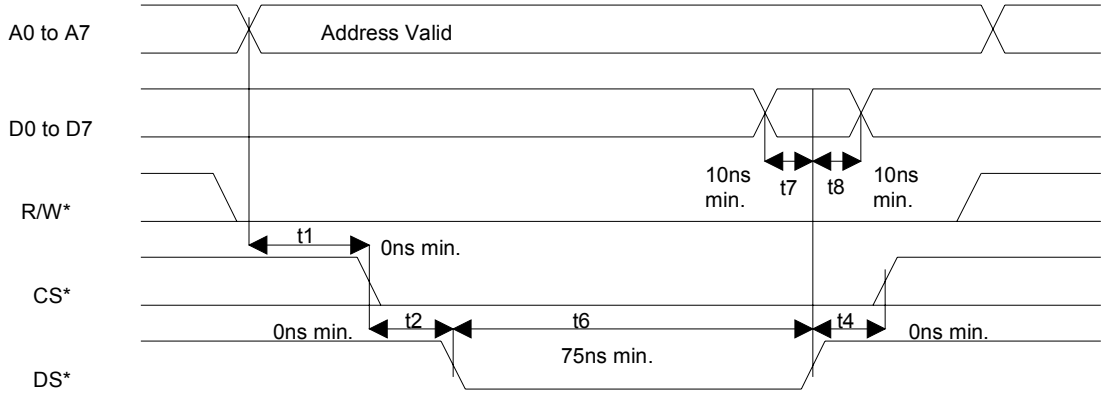
INTEL BUS WRITE AC TIMING (BTS=0 / MUX=0) Figure 21-5



MOTOROLA BUS READ AC TIMING (BTS=1 / MUX=0) Figure 21-6



MOTOROLA BUS WRITE AC TIMING (BTS=1 / MUX=0) Figure 21-7



21.3 Receive Side AC Characteristics

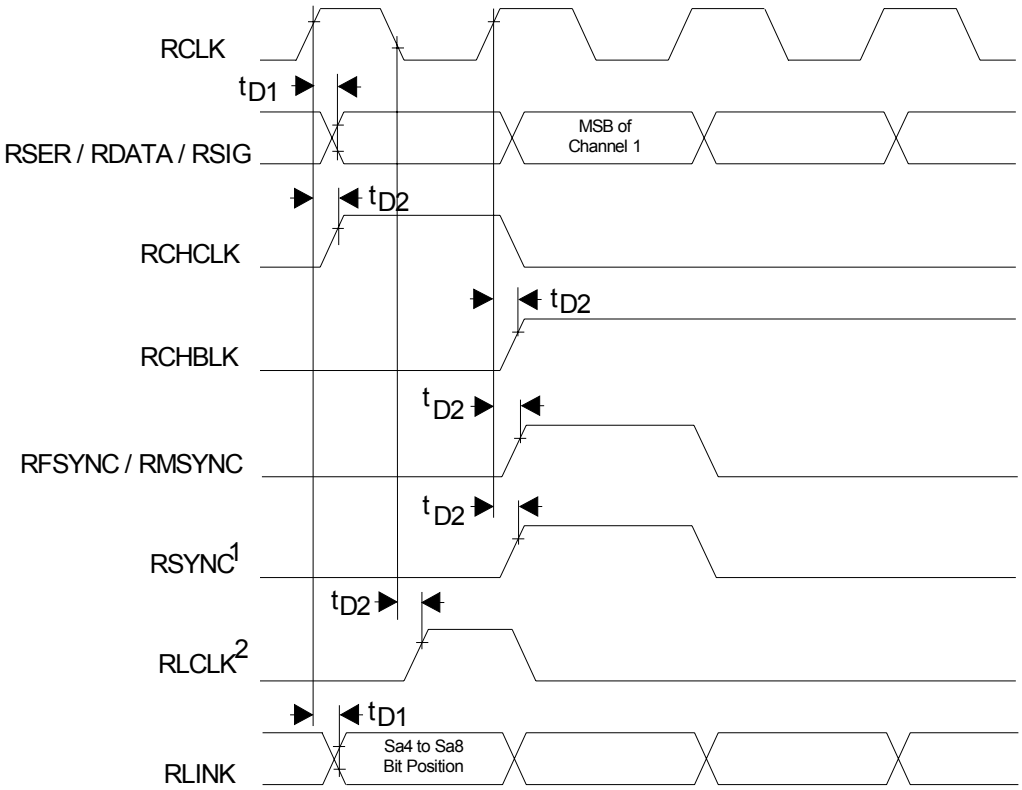
AC CHARACTERISTICS – RECEIVE SIDE [See Figure 21-8 to Figure 21-10]
(0°C to 70°C; V_{DD} = 3.3V ± 5% for DS21354L;
0°C to 70°C; V_{DD} = 5.0V ± 5% for DS21554L;
-40°C to +85°C; V_{DD} = 3.3V ± 5% for DS21354LN;
-40°C to +85°C; V_{DD} = 5.0V ± 5% for DS21554LN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLKO Period	t_{LP}		488		ns	
RCLKO Pulse Width	t_{LH}	200	244		ns	1
	t_{LL}	200	244		ns	1
RCLKO Pulse Width	t_{LH}	150	244		ns	2
	t_{LL}	150	244		ns	2
RCLKI Period	t_{CP}		488		ns	
RCLKI Pulse Width	t_{CH}	75			ns	
	t_{CL}	75			ns	
RSYSCLK Period	t_{SP}	100	648		ns	3
	t_{SP}	100	488		ns	4
	t_{SP}	100	244		ns	5
	t_{SP}	100	122		ns	6
RSYSCLK Pulse Width	t_{SH}	50			ns	
	t_{SL}	50			ns	
RSYNC Set Up to RSYSCLK Falling	t_{SU}	20		t_{SH} –5	ns	
RSYNC Pulse Width	t_{PW}	50			ns	
RPOSI/RNEGI Set Up to RCLKI Falling	t_{SU}	20			ns	
RPOSI/RNEGI Hold From RCLKI Falling	t_{HD}	20			ns	
RSYSCLK/RCLKI Rise and Fall Times	t_R, t_F			25	ns	
Delay RCLKO to RPOSO, RNEGO Valid	t_{DD}			50	ns	
Delay RCLK to RSER, RDATA, RSIG, RLINK Valid	t_{D1}			50	ns	
Delay RCLK to RCHCLK, RSYNC, RCHBLK, RFSYNC, RLCLK	t_{D2}			50	ns	
Delay RSYSCLK to RSER, RSIG Valid	t_{D3}			50	ns	
Delay RSYSCLK to RCHCLK, RCHBLK, RMSYNC, RSYNC, CO	t_{D4}			50	ns	
CI Set Up to RSYSCLK Rising	t_{SC}	20			ns	
CI Pulse Width	t_{WC}	50			ns	

NOTES:

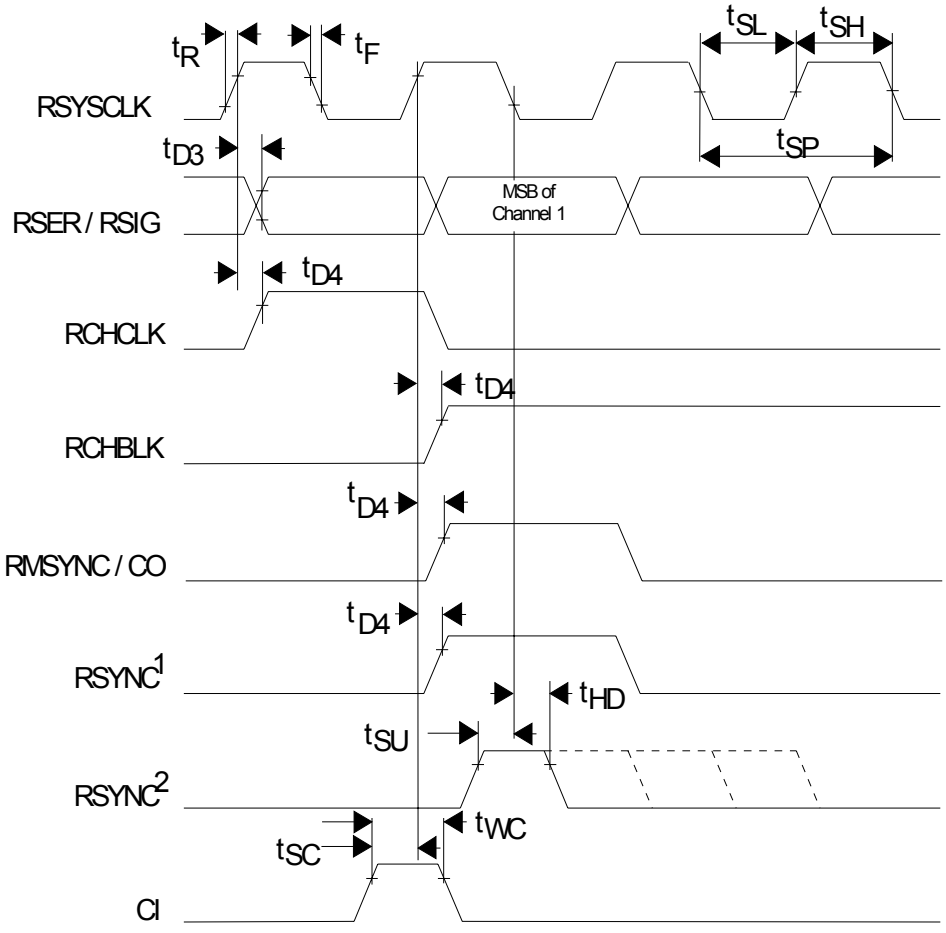
1. Jitter attenuator enabled in the receive path.
2. Jitter attenuator disabled or enabled in the transmit path.
3. RSYSCLK = 1.544 MHz.
4. RSYSCLK = 2.048 MHz.
5. RSYSCLK = 4.096 MHz
6. RSYSCLK = 8.192 MHz

RECEIVE SIDE AC TIMING Figure 21-8



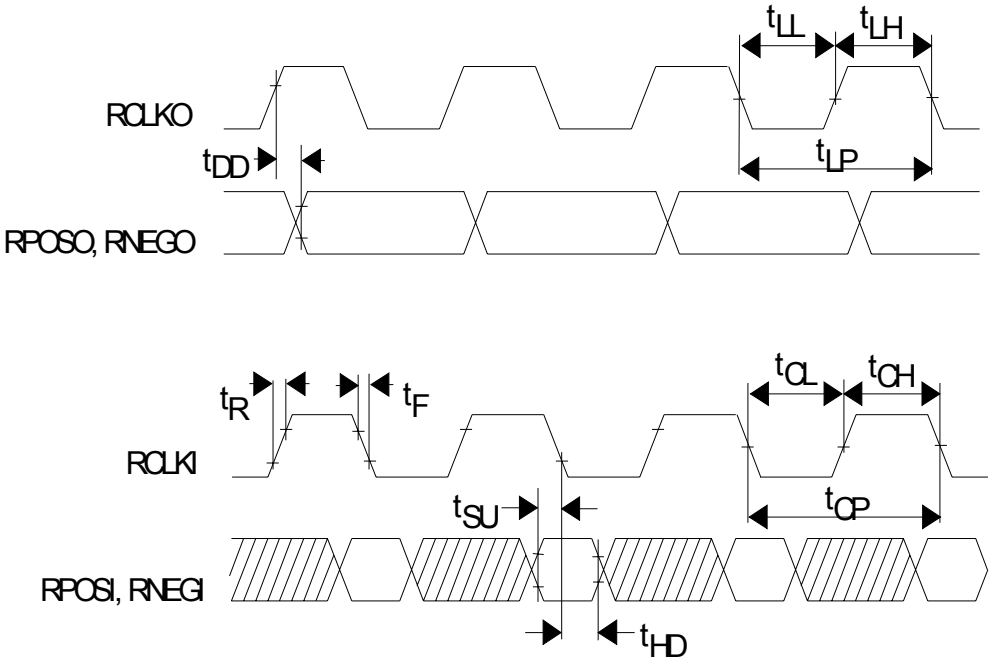
Notes:
1. RSYNC is in the output mode (RCR1.5 = 0).
2. RLCLK will only pulse high during Sa bit locations as defined in RCR2; no relationship between RLCLK and RSYNC or RFSYNC is implied.

RECEIVE SYSTEM SIDE AC TIMING Figure 21-9



Notes:
1. RSYNC is in the output mode (RCR1.5 = 0)
2. RSYNC is in the input mode (RCR1.5 = 1)

RECEIVE LINE INTERFACE AC TIMING Figure 21-10



21.4 Transmit AC Characteristics

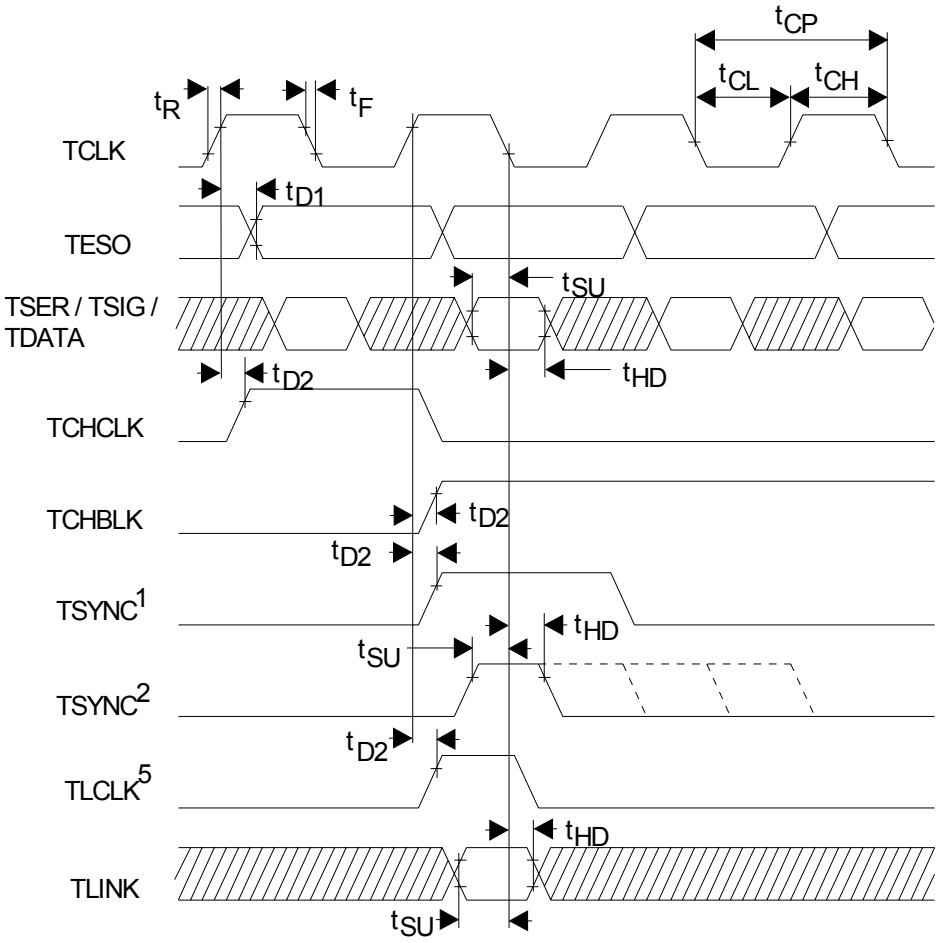
AC CHARACTERISTICS – TRANSMIT SIDE [See Figure 21-11 to Figure 21-13]
(0°C to 70°C; V_{DD} = 3.3V ± 5% for DS21354L;
0°C to 70°C; V_{DD} = 5.0V ± 5% for DS21554L;
-40°C to +85°C; V_{DD} = 3.3V ± 5% for DS21354LN;
-40°C to +85°C; V_{DD} = 5.0V ± 5% for DS21554LN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_{CP}		488		ns	
TCLK Pulse Width	t_{CH} t_{CL}	75 75			ns ns	
TCLKI Period	t_{LP}		488		ns	
TCLKI Pulse Width	t_{LH} t_{LL}	75 75			ns ns	
TSYSCLK Period	t_{SP} t_{SP} t_{SP} t_{SP}	100 100 100 100	648 448 244 122		ns ns ns ns	1 2 3 4
TSYSCLK Pulse Width	t_{SH} t_{SL}	50 50			ns ns	
TSYNC or TSSYNC Set Up to TCLK or TSYSCLK falling	t_{SU}	20		t_{CH} –5 or t_{SH} –5	ns	
TSYNC or TSSYNC Pulse Width	t_{PW}	50			ns	
TSER, TSIG, TDATA, TLINK, TPOSI, TNEGI Set Up to TCLK, TSYSCLK, TCLKI Falling	t_{SU}	20			ns	
TSER, TSIG, TDATA, TLINK, TPOSI, TNEGI Hold from TCLK, TSYSCLK, TCLKI Falling	t_{HD}	20			ns	
TCLK, TCLKI or TSYSCLK Rise and Fall Times	t_R , t_F			25	ns	
Delay TCLKO to TPOSO, TNEGO Valid	t_{DD}			50	ns	
Delay TCLK to TESO Valid	t_{D1}			50	ns	
Delay TCLK to TCHBLK, TCHCLK, TSYNC, TLCLK	t_{D2}			50	ns	
Delay TSYSCLK to TCHCLK, TCHBLK, CO	t_{D3}			75	ns	
CI Set Up to TSYSCLK Rising	t_{SC}	20			ns	
CI Pulse Width	t_{WC}	50			ns	

NOTES:

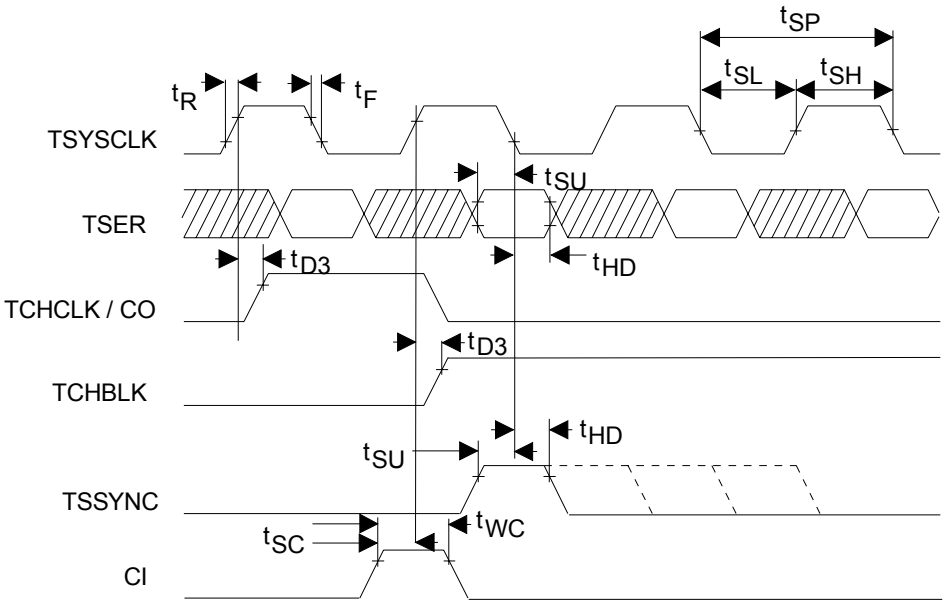
1. TSYSCLK = 1.544 MHz.
2. TSYSCLK = 2.048 MHz.
3. TSYSCLK = 4.096 MHz
4. TSYSCLK = 8.192 MHz

TRANSMIT SIDE AC TIMING Figure 21-11



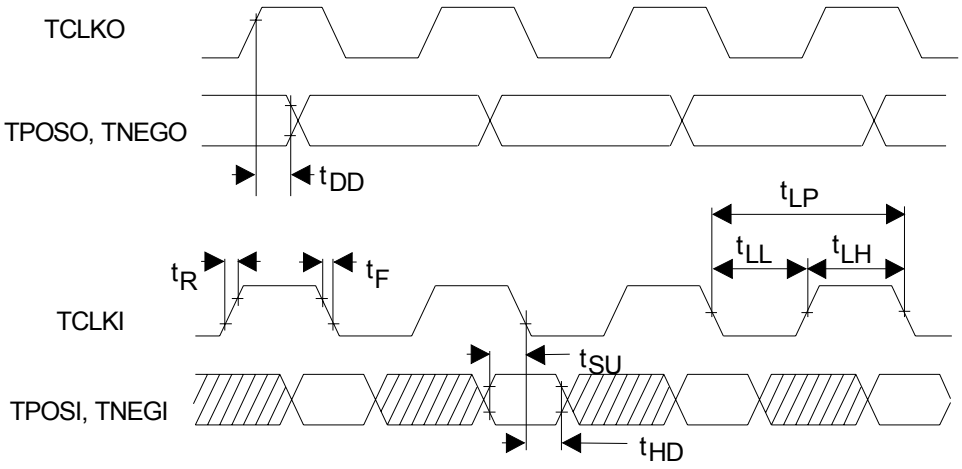
Notes:
1. TSYNC is in the output mode (TCR1.0 = 1).
2. TSYNC is in the input mode (TCR1.0 = 0).
3. TSER is sampled on the falling edge of TCLK when the transmit side elastic store is disabled.
4. TCHCLK and TCHBLK are synchronous with TCLK when the transmit side elastic store is disabled.
5. TLINK is only sampled during Sa bit locations as defined in TCR2; no relationship between TLCLK/TLINK and TSYNC is implied.

TRANSMIT SYSTEM SIDE AC TIMING Figure 21-12

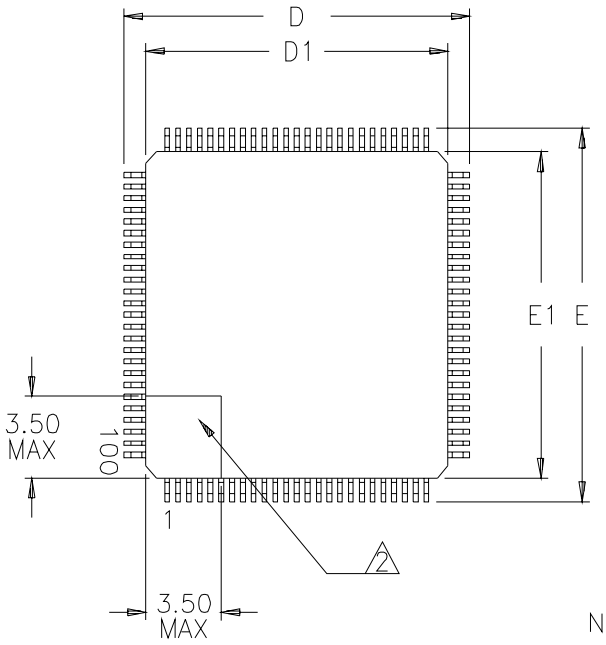


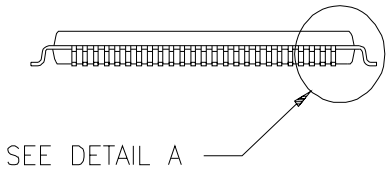
Notes:
1. TSER is only sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.
2. TCHCLK and TCHBLK are synchronous with TSYSCLK when the transmit side elastic store is enabled.

TRANSMIT LINE INTERFACE SIDE AC TIMING Figure 21-13



22 MECHANICAL DESCRIPTION

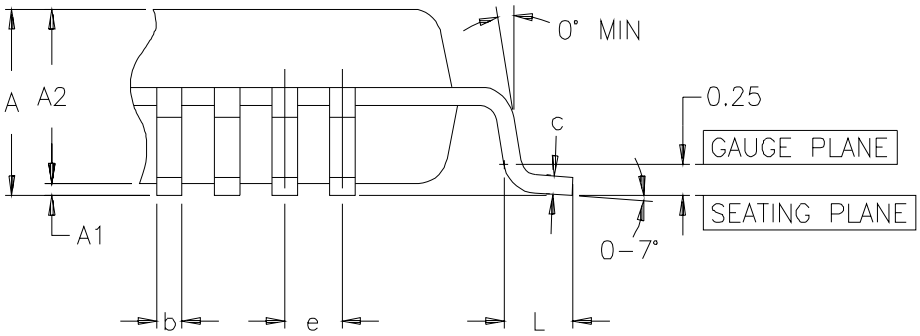




NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION; PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.
4. ALL DIMENSIONS ARE IN MILLIMETERS.

DIM	MIN	MAX
A	–	1.60
A1	0.05	–
A2	1.35	1.45
b	0.17	0.27
c	0.09	0.20
D	15.80	16.20
D1	14.00 BSC	
E	15.80	16.20
E1	14.00 BSC	
e	0.50 BSC	
L	0.45	0.75



DETAIL A