DS1994
4kb Plus Time Memory iButton

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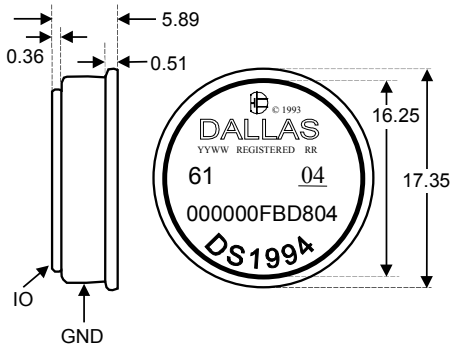
SPECIAL FEATURES

- 4096 bits of Read/Write Nonvolatile Memory
- 256-bit Scratchpad Ensures Integrity of Data Transfer
- Memory Partitioned into 256-bit Pages for Packetizing Data
- Data Integrity Assured with Strict Read/Write Protocols
- Contains Real-Time Clock/Calendar in Binary Format
- Interval Timer Can Automatically Accumulate Time When Power is Applied
- Programmable Cycle Counter can Accumulate the Number of System Power-On/Off Cycles
- Programmable Alarms Can Be Set to Generate Interrupts for Interval Timer, Real-Time Clock, and/or Cycle Counter
- Write-Protect Feature Provides Tamperproof Time Data
- Programmable Expiration Date That Limits Access to SRAM and Timekeeping
- Clock Accuracy is Better Than ±2 Minutes/ Month at 25°C
- Operating Temperature Range from -40°C to +70°C
- Over 10 Years of Data Retention

COMMON iButton® FEATURES

- Unique, Factory-Lasered, and Tested 64-bit Registration Number (8-bit Family Code + 48-bit Serial Number + 8-bit CRC Tester) Assures Absolute Traceability Because No Two Parts Are Alike
- Multidrop Controller for MicroLAN
- Digital Identification and Information by Momentary Contact
- Chip-Based Data Carrier Compactly Stores Information
- Data Can Be Accessed While Affixed to Object
- Economically Communicates to Bus Master with a Single Digital Signal at 16.3kbps
- Standard 16mm Diameter and 1-Wire® Protocol Ensure Compatibility with iButton Family
- Button Shape is Self-Aligning with Cup-Shaped Probes
- Durable Stainless Steel Case Engraved with Registration Number Withstands Harsh Environments
- Easily Affixed with Self-Stick Adhesive Backing, Latched by its Flange, or Locked with a Ring Pressed onto its Rim
- Presence Detector Acknowledges when Reader First Applies Voltage
- Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus, Approved under Entity Concept for Use in Class I, Division 1, Group A, B, C and D Locations

F5 MICROCAN



All dimensions shown in millimeters.

ORDERING INFORMATION

DS1994L-F5 F5 MicroCan

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EXAMPLES OF ACCESSORIES

DS9096P Self-Stick Adhesive Pad
DS9101 Multi-Purpose Clip
DS9093RA Mounting Lock Ring
DS9093F Snap-In Fob
DS9092 iButton Probe

iButton DESCRIPTION

The DS1994 Memory iButton is a rugged read/write data carrier that acts as a localized database, easily accessible with minimal hardware. The nonvolatile memory and optional timekeeping capability offer a simple solution to storing and retrieving vital information pertaining to the object to which the iButton is attached. Data is transferred serially through the 1-Wire protocol that requires only a single data lead and a ground return.

The scratchpad is an additional page that acts as a buffer when writing to memory. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command transfers the data to memory. This process ensures data integrity when modifying the memory. A 48-bit serial number is factory lasered into each DS1994 to provide a guaranteed unique identity that allows for absolute traceability. The durable MicroCan package is highly resistant to environmental hazards such as dirt, moisture, and shock. Its compact, coin-shaped profile is self-aligning with mating receptacles, allowing the DS1994 to be easily used by human operators. Accessories permit the DS1994 to be mounted on almost any surface including plastic key fobs, photo-ID badges, and PC boards.

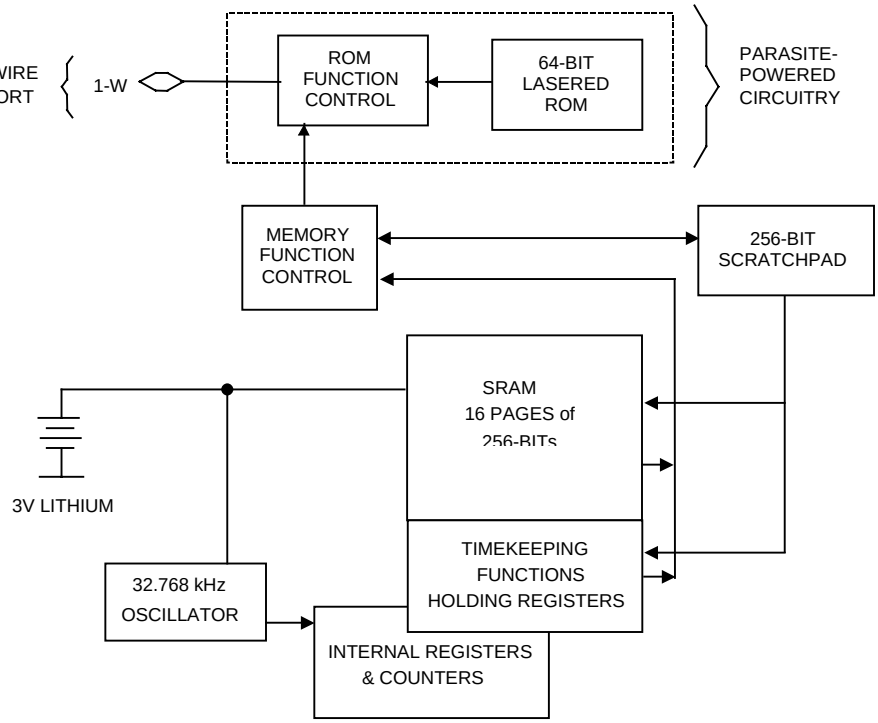
The DS1994 also includes time-keeping functions, a real-time clock/calendar, interval timer, cycle counter, and programmable interrupts, in addition to the nonvolatile memory. The internal clock can be programmed to deny memory access based on absolute time/date, total elapsed time, or the number of accesses. These features allow the DS1994 to be used to create a stopwatch, alarm clock, time and date stamp, logbook, hour meter, calendar, system power cycle timer, interval timer, and event scheduler.

OPERATION

The DS1994 has four main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, 3) 4096-bit SRAM, and 4) timekeeping registers. The timekeeping section utilizes an on-chip oscillator that is connected to a 32.768kHz crystal. The SRAM and time-keeping registers reside in one contiguous address space referred to hereafter as memory. All data is read and written least significant bit first.

The memory functions are not available until the ROM function protocol has been established. This protocol is described in the ROM functions flowchart (Figure 9). The master must first provide one of four ROM function commands: 1) read ROM, 2) match ROM, 3) search ROM, or 4) skip ROM. After a ROM function sequence has been successfully executed, the memory functions are accessible and the master can then provide any one of the four memory function commands (Figure 6).

Figure 1. DS1994 BLOCK DIAGRAM



PARASITE POWER

The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry steals power whenever the data input is high. The data line provides sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) by parasiting off this input, lithium is conserved, and 2) if the lithium is exhausted for any reason, the ROM can still be read normally.

64-BIT LASERED ROM

Each DS1994 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits. (See Figure 2.) The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates, as shown in Figure 3. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in the Book of DS19xx iButton Standards. The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, 1 bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC should return the shift register to all zeros.

Figure 2. 64-BIT LASERED ROM

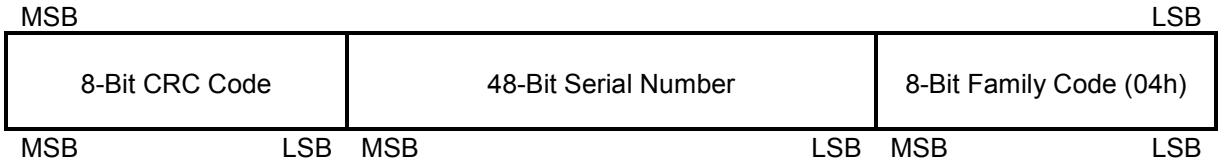
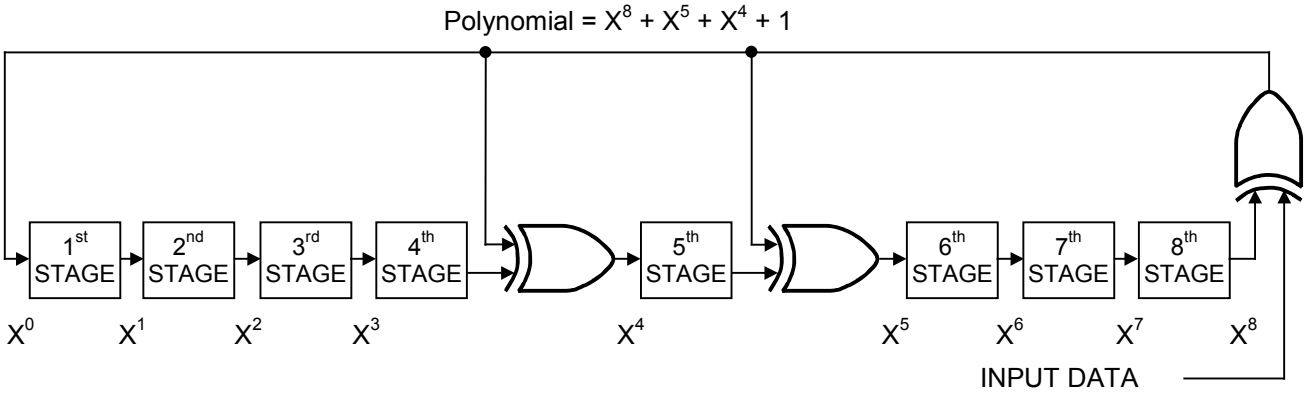


Figure 3. 1-WIRE CRC CODE



MEMORY

The memory map in Figure 4 shows a 32-Byte page called the scratchpad, and additional 32-Byte pages called memory. The DS1994 contains 16 pages that make up the 4096-bit SRAM. The DS1994 also contains page 16, which has only 30 Bytes containing the timekeeping registers.

The scratchpad is an additional page that acts as a buffer when writing to memory. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command transfers the data to memory. This process ensures data integrity when modifying the memory.

TIMEKEEPING

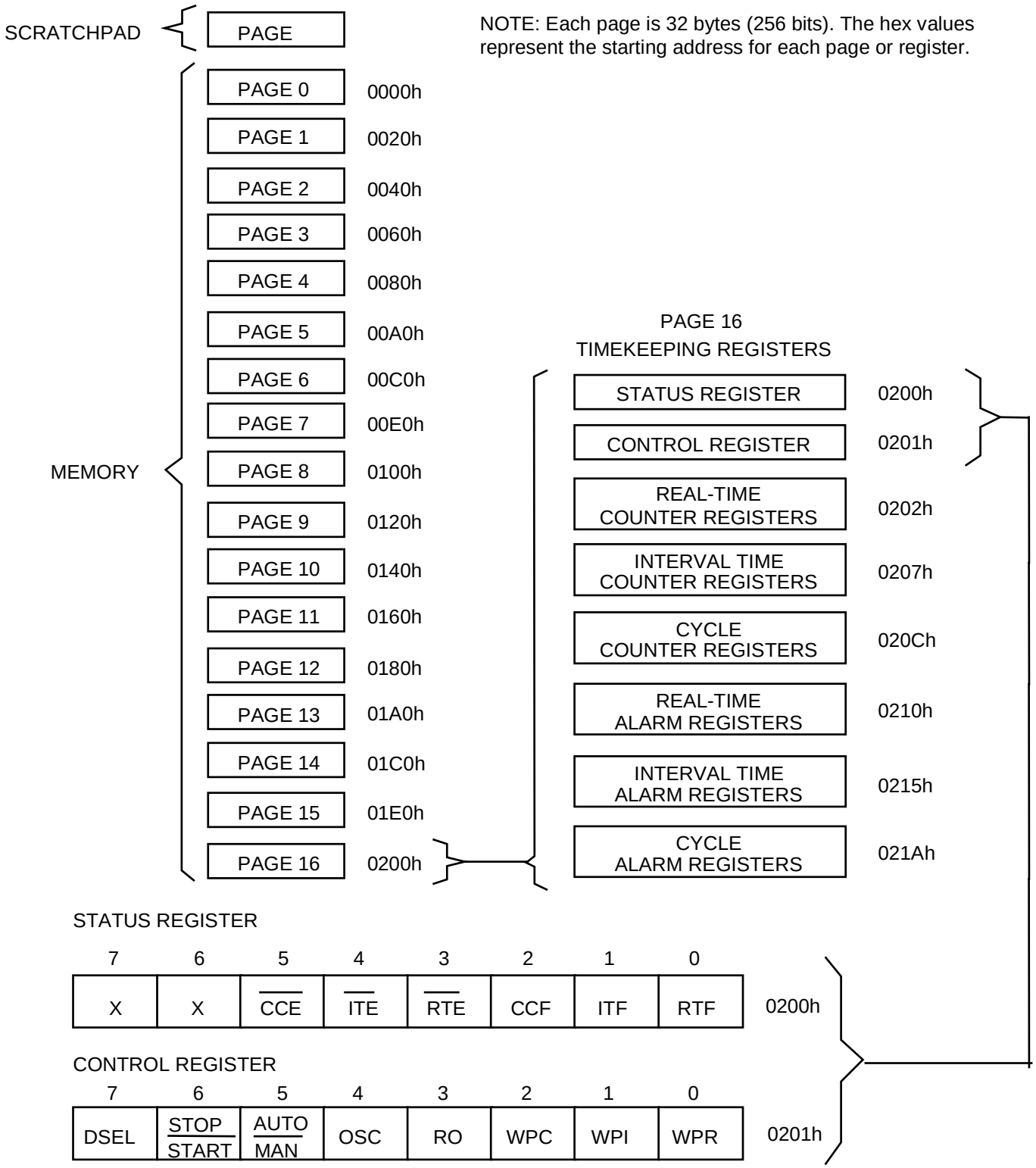
A 32.768kHz crystal oscillator is used as the time base for the timekeeping functions. The oscillator can be turned on or off by an enable bit in the control register. The oscillator must be on for the real-time clock, interval timer, and cycle counter to function.

The timekeeping functions are double buffered. This feature allows the master to read time or count without the data changing while it is being read. To accomplish this, a snapshot of the counter data is transferred to holding registers that the user accesses. This occurs after the 8th bit of the read memory function command.

Real-Time Clock

The real-time clock is a 5-Byte binary counter. It is incremented 256 times per second. The least significant Byte is a count of fractional seconds. The upper 4 Bytes are a count of seconds. The real-time clock can accumulate 136 years of seconds before rolling over. Time/date is represented by the number of seconds since a reference point, which is determined by the user. For example, 12:00 A.M., January 1, 1970 could be a reference point.

Figure 4. DS1994 MEMORY MAP



Interval Timer

The interval timer is a 5-Byte binary counter. When enabled, it is incremented 256 times per second. The least significant Byte is a count of fractional seconds. The interval timer can accumulate 136 years of seconds before rolling over. The interval timer has two modes of operation that are selected by the AUTO/$\overline{\text{MAN}}$ bit in the control register. In the auto mode, the interval timer begins counting after the data line has been high for a period of time determined by the DSEL bit in the control register. Similarly, the interval timer stops counting after the data line has been low for a period of time determined by the DSEL bit. In the manual mode, time accumulation is controlled by the STOP/$\overline{\text{START}}$ bit in the control register.

NOTE: For auto mode operation, the high level on the data line must be greater than or equal to 2.1V.

Cycle Counter

The cycle counter is a 4-Byte binary counter. It increments after the falling edge of the data line if the appropriate data line timing has been met. This timing is selected by the DSEL bit in the control register. (See the *Status/Control* section).

NOTE: For cycle counter operation, the high level on the data line must be greater than or equal to 2.1V.

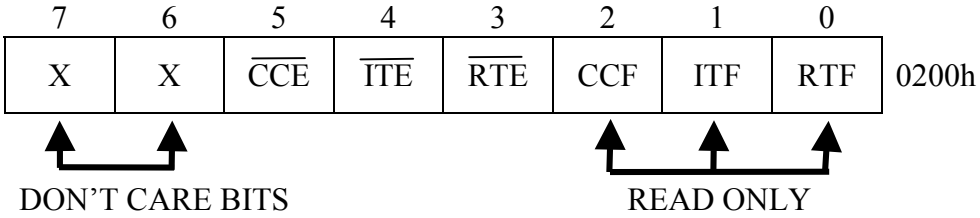
Alarm Registers

The alarm registers for the real-time clock, interval timer, and cycle counter all operate in the same manner. When the value of a given counter equals the value in its associated alarm register, the appropriate flag bit is set in the status register. If the corresponding interrupt enable bit in the status register is set, an interrupt is generated. If a counter and its associated alarm register are write protected when an alarm occurs, access to the device becomes limited. (See the *Status/Control*, *Interrupts*, and *Programmable Expiration* sections.)

STATUS/CONTROL REGISTERS

The status and control registers are the first two Bytes of page 16 (see Figure 4).

Status Register



0	RTF	Real-time clock alarm flag
1	ITF	Interval timer alarm flag
2	CCF	Cycle counter alarm flag

When a given alarm occurs, the corresponding alarm flag is set to a logic 1. The alarm flag is cleared by reading the status register.

3	$\overline{\text{RTE}}$	Real-time clock alarm flag
4	$\overline{\text{ITE}}$	Interval timer alarm flag
5	$\overline{\text{CCE}}$	Cycle counter alarm flag

Writing any of the interrupt enable bits to a logic 0 allows an interrupt condition to be generated when its corresponding alarm flag is set (see the *Interrupts* section).

Control Register

7	6	5	4	3	2	1	0	
$\overline{\text{DSEL}}$	STOP/$\overline{\text{START}}$	AUTO MAN.	OSC	RO	WPC	WPI	WPR	0201h

0	WPR	Write protect real-time clock/alarms registers
1	WPI	Write protect interval timer/alarms registers
2	WPC	Write protect cycle counter/alarms registers

Setting a write protect bit to a logic 1 permanently write protects the corresponding counter and alarm registers, all write protect bits, and additional bits in the control register. The write protect bits cannot be written in a normal manner (see the *Write Protect/Programmable Expiration* section).

3	RO	Read only

If a programmable expiration occurs and the read only bit is set to a logic 1, then the DS1994 becomes read only. If a programmable expiration occurs and the read only bit is a logic 0, then only the 64-bit lasered ROM can be accessed (see the *Write Protect/Programmable Expiration* section).

4	OSC	Oscillator enable

This bit controls the crystal oscillator. When set to a logic 1, the oscillator starts operation. When the oscillator bit is a logic 0, the oscillator stops.

5	AUTO/$\overline{\text{MAN}}$	Automatic/$\overline{\text{Manual}}$ Mode

When this bit is set to a logic 1, the interval timer is in automatic mode. In this mode, the interval timer is enabled by the data line. When this bit is set to a logic 0, the interval timer is in manual mode. In this mode, the interval timer is enabled by the STOP/$\overline{\text{START}}$ bit.

6	STOP/$\overline{\text{START}}$	Stop/$\overline{\text{Start}}$ (in manual mode)

If the interval timer is in manual mode, the interval timer starts counting when this bit is set to a logic 0 and stops counting when set to a logic 1. If the interval timer is in automatic mode, this bit has no effect.

7	DSEL	Delay Select Bit

This bit selects the delay that it takes for the cycle counter and the interval timer (in auto mode) to see a transition on the data line. When this bit is set to a logic 1, the delay time is 123 ± 2ms. This delay allows communication on the data line without starting or stopping the interval timer and without incrementing the cycle counter. When this bit is set to a logic 0, the delay time is 3.5 ± 0.5ms.

MEMORY FUNCTION COMMANDS

The Memory Function Flowchart (Figure 6) describes the protocols necessary for accessing the memory. An example follows the flowchart. Three address registers are provided as shown in Figure 5. The first two registers represent a 16-bit target address (TA1, TA2). The third register is the ending offset/data status Byte (E/S).

The target address points to a unique Byte location in memory. The first 5 bits of the target address (T4:T0) represent the Byte offset within a page. This Byte offset points to one of 32 possible Byte locations within a given page. For instance, 00000b points to the first Byte of a page where as 11111b would point to the last Byte of a page.

The third register (E/S) is a read only register. The first 5 bits (E4:E0) of this register are called the ending offset. The ending offset is a Byte offset within a page (1 of 32 Bytes). Bit 5 (PF) is the partial Byte flag. Bit 6 (OF) is the overflow flag. Bit 7 (AA) is the authorization accepted flag.

Figure 5. ADDRESS REGISTERS

	7	6	5	4	3	2	1	0
TARGET ADDRESS (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY)	AA	OF	PF	E4	E3	E2	E1	E0

Write Scratchpad Command [0Fh]

After issuing the write scratchpad command, the user must first provide the 2-Byte target address, followed by the data to be written to the scratchpad. The data is written to the scratchpad starting at the Byte offset (T4:T0). The ending offset (E4:E0) is the Byte offset at which the host stops writing data. The maximum ending offset is 11111b (31d). If the host attempts to write data past this maximum offset, the overflow flag (OF) is set and the remaining data is ignored. If the user writes an incomplete Byte and an overflow has not occurred, the partial Byte flag (PF) is set.

Read Scratchpad Command [AAh]

This command can be used to verify scratchpad data and target address. After issuing the read scratchpad command, the user can begin reading. The first two Bytes are the target address. The next Byte is the

ending offset/data status Byte (E/S), followed by the scratchpad data beginning at the Byte offset (T4:T0). The user can read data until the end of the scratchpad, after which the data read is all logic 1's.

Copy Scratchpad [55h]

This command is used to copy data from the scratchpad to memory. After issuing the copy scratchpad command, the user must provide a 3-Byte authorization pattern. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the AA (authorization accepted) flag is set and the copy begins. A logic 0 is transmitted after the data has been copied until the user issues a reset pulse. Any attempt to reset the part is ignored while the copy is in progress. Copy typically takes 30µs.

The data to be copied is determined by the three address registers. The scratchpad data, from the beginning offset through the ending offset, is copied to memory, starting at the target address. Anywhere from 1 to 32 Bytes can be copied to memory with this command. Whole Bytes are copied even if only partially written. The AA flag is cleared only by executing a write scratchpad command.

Read Memory [F0h]

The read memory command can be used to read the entire memory. After issuing the command, the user must provide the 2-Byte target address. After the two Bytes, the user reads data beginning from the target address and can continue until the end of memory, at which point logic 1's are read. It is important to realize that the target address registers contain the address provided. The ending offset/data status Byte is unaffected.

The hardware of the DS1994 provides a means to accomplish error-free writing to the memory section. To safeguard reading data in the 1-Wire environment and to simultaneously speed up data transfers, it is recommended to packetize data into data packets of the size of one memory page each. Such a packet would typically store a 16-bit CRC with each page of data to ensure rapid, error-free data transfers that eliminate having to read a page multiple times to determine if the received data is correct or not. (Refer to Application Note 114 for the recommended file structure to be used with the 1-Wire environment.)

Figure 6. MEMORY FUNCTIONS FLOWCHART

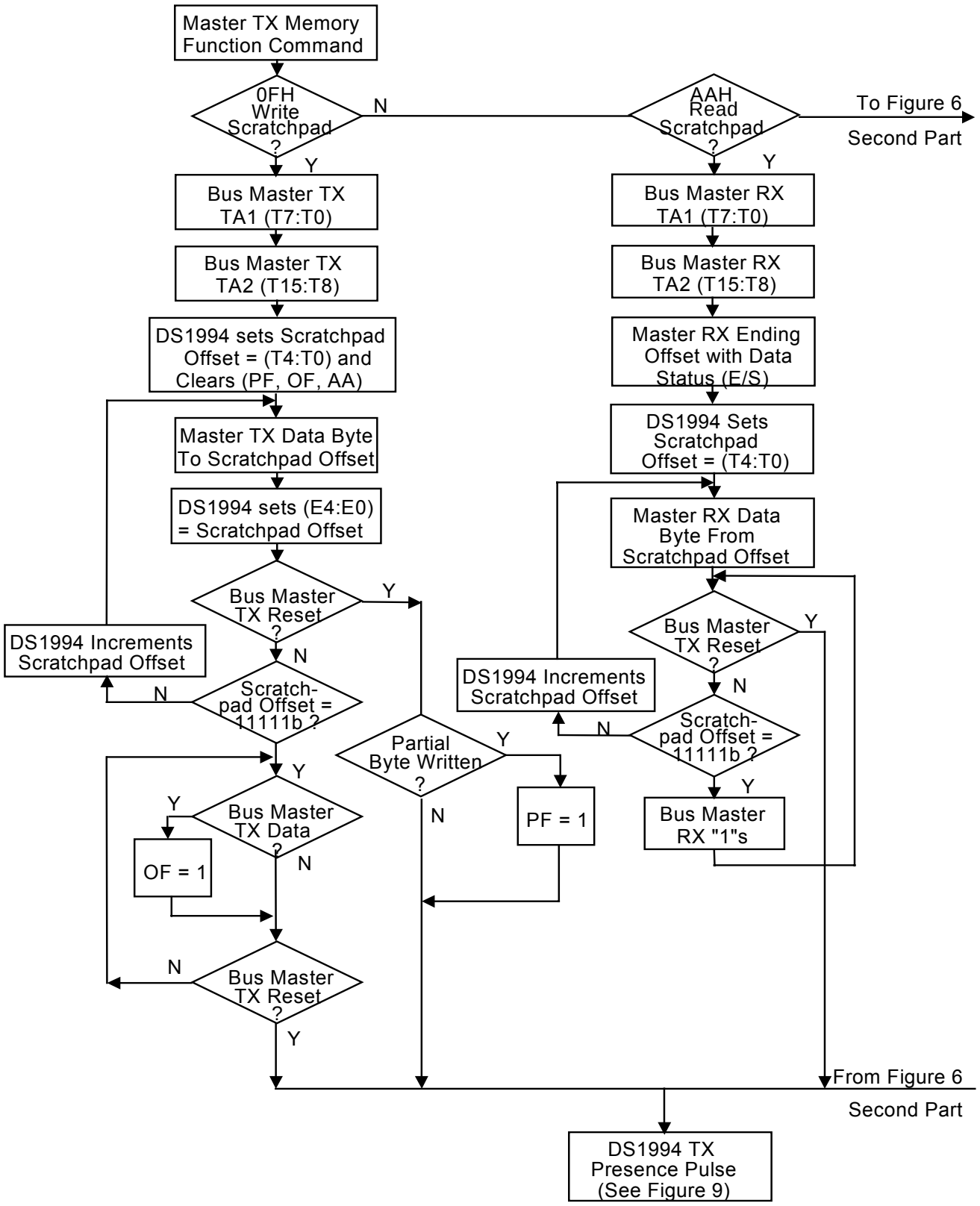
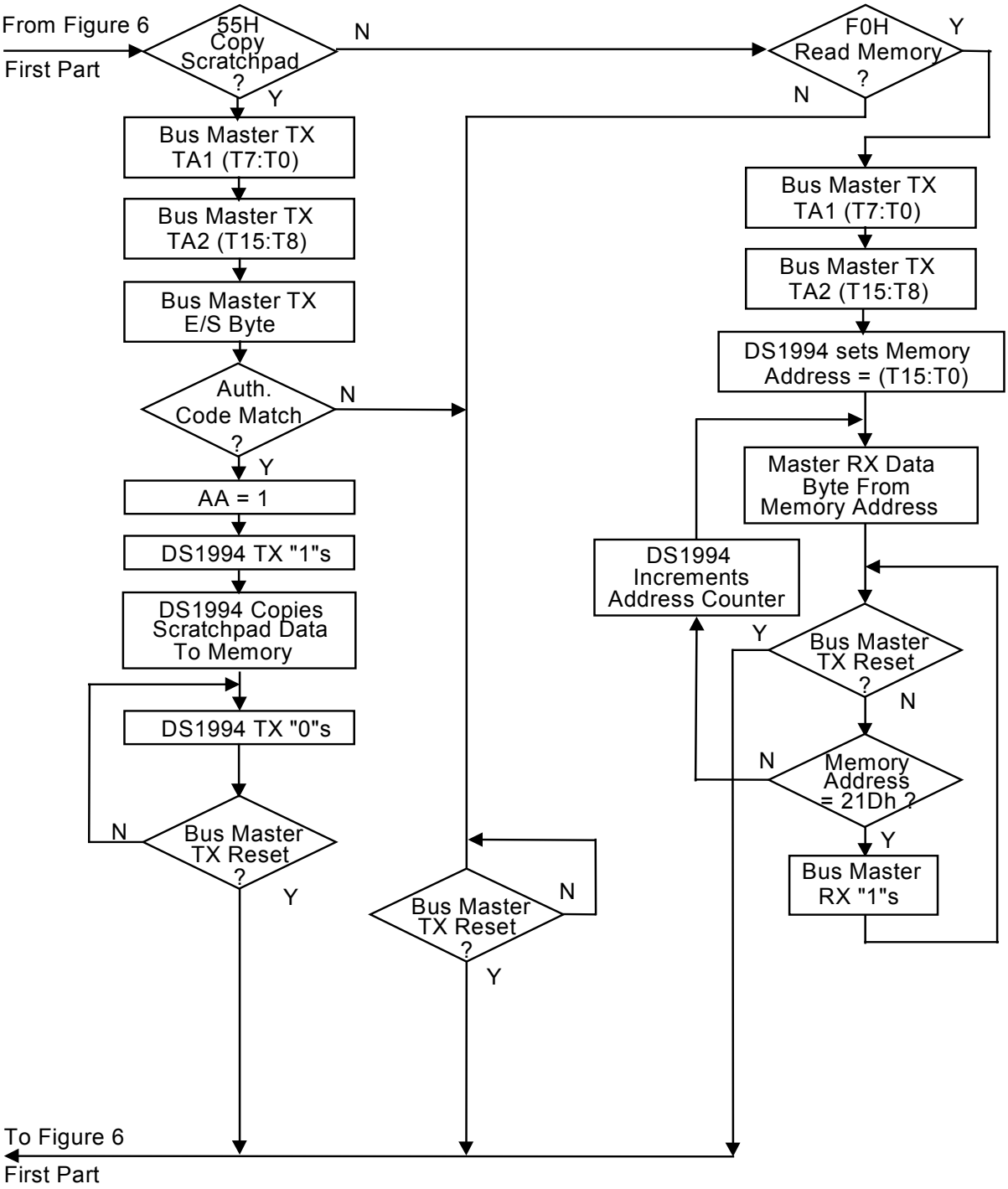


Figure 6. MEMORY FUNCTIONS FLOWCHART (continued)



MEMORY FUNCTION EXAMPLES

Example: Write two data Bytes to memory locations 0026h and 0027h (the seventh and eighth Bytes of page 1). Read entire memory.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480µs–960µs)
RX	Presence	Presence pulse
TX	CCh	Issue skip ROM command
TX	0Fh	Issue write scratchpad command
TX	26h	TA1, beginning offset = 6
TX	00h	TA2, address = 0026h
TX	<2 data Bytes>	Write 2 Bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue skip ROM command
TX	AAh	Issue read scratchpad command
RX	26h	Read TA1, beginning offset = 6
RX	00h	Read TA2, address = 0026h
RX	07h	Read E/S, ending offset = 7, flags = 0
RX	<2 data Bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue skip ROM command
TX	55h	Issue copy scratchpad command
TX	26h	TA1 } AUTHORIZATION CODE
TX	00h	TA2 } AUTHORIZATION CODE
TX	07h	E/S } AUTHORIZATION CODE
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue skip ROM command
TX	F0h	Issue read memory command
TX	00h	TA1, beginning offset = 6
TX	00h	TA2, address = 0000h
RX	<542 Bytes>	Read entire memory
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

WRITE PROTECT/PROGRAMMABLE EXPIRATION

The write protect bits (WPR, WPI, WPC) provide a means of write protecting the timekeeping data and limiting access to the DS1994 when an alarm occurs (programmable expiration). The write protect bits cannot be written by performing a single copy scratchpad command. Instead, to write these bits, the copy scratchpad command must be performed three times. Please note that the AA bit is set, as expected, after the first copy command is successfully executed. Therefore, the authorization pattern for the second and third copy command should have this bit set. The read scratchpad command can be used to verify the authorization pattern.

The write protect bits, once set, permanently write protect their corresponding counter and alarm registers, all write protect bits, and certain control register bits as shown in Figure 7. The time/count registers continue to count if the oscillator is enabled. If the user wishes to set more than one write protect bit, the user must set them at the same time. Once a write protect bit is set it cannot be undone, and the remaining write protect bits, if not set, cannot be set. The programmable expiration takes place when one or more write protect bits have been set and a corresponding alarm occurs. If the RO (read only) bit is set, only the read scratch and read memory function commands are available. If the RO bit is a logic 0, no memory function commands are available. The ROM functions are always available.

Figure 7. WRITE PROTECT CHART

WRITE PROTECT BIT SET:	WPR	WPI	WPC
Data Protected from User Modification:	Real-Time Clock Real-Time Alarm WPR WPI WPC RO OSC*	Interval Timer Interval Time Alarm WPR WPI WPC RO OSC* STOP/$\overline{\text{START}}$ ** AUTO/$\overline{\text{MAN}}$	Cycle Counter Cycle Counter Alarm WPR WPI WPC RO OSC* DSEL

* Becomes write 1 only, i.e., once written to a logic 1, cannot be written back to a logic 0.
** Forced to a logic 0.

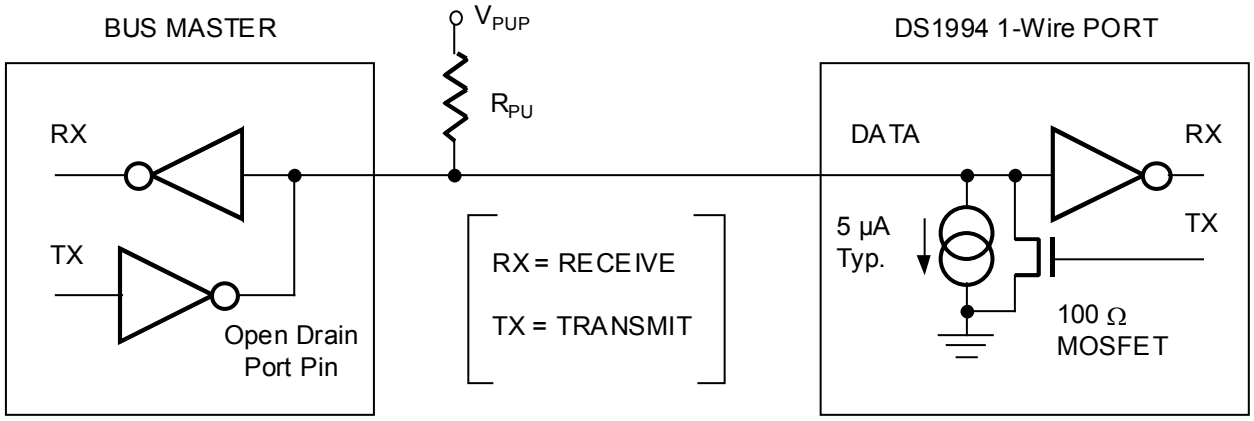
1-WIRE BUS SYSTEM

The 1-Wire bus is a system that has a single bus master and one or more slaves. In most instances, the DS1994 behaves as a slave. The exception is when the DS1994 generates an interrupt due to a timekeeping alarm. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or three-state outputs. The 1-Wire port of the DS1994 is open drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The 1-Wire bus has a maximum data rate of 16.3kbps and requires a pullup resistor of approximately 5kΩ. The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120µs, one or more of the devices on the bus can be reset.

Figure 8. HARDWARE CONFIGURATION



TRANSACTION SEQUENCE

The protocol for accessing the DS1994 through the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master, followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS1994 is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (see the flowchart in Figure 9).

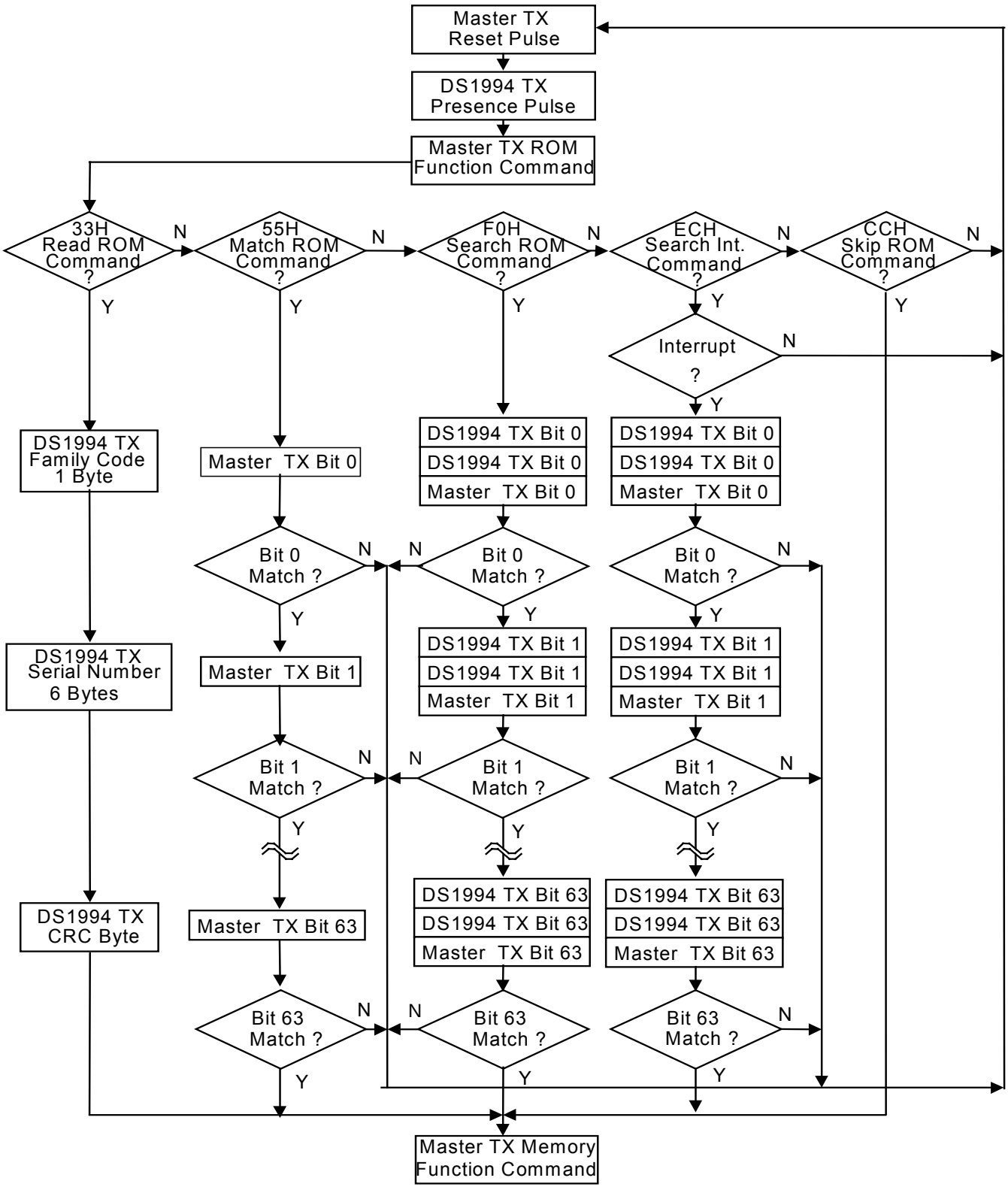
Read ROM [33h]

This command allows the bus master to read the DS1994's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS1994 on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48–bit serial number usually result in a mismatch of the CRC.

Match ROM [55h]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS1994 on a multidrop bus. Only the DS1994 that exactly matches the 64-bit ROM sequence responds to the subsequent memory function command. All slaves that do not match the 64-bit ROM sequence wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Figure 9. ROM FUNCTIONS FLOWCHART



Skip ROM [CCh]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The search ROM process is the repetition of a simple three–step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, three-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. Additional passes can identify the remaining number of devices and their ROM codes. See Chapter 5 of the Book of DS19xx iButton Standards for a comprehensive discussion of a search ROM, including an actual example.

Search Interrupt [ECh]

This ROM command works exactly as the normal ROM Search, but it identifies only devices with interrupts that have not yet been acknowledged.

1-WIRE SIGNALING

The DS1994 requires strict protocols to ensure data integrity. The protocol consists of five types of signaling on one line: reset sequence with reset pulse and presence pulse, write 0, write 1, read data, and interrupt pulse. The bus master initiates all these signals except presence pulse and interrupt pulse. The initialization sequence required to begin any communication with the DS1994 is shown in Figure 10. A reset pulse followed by a presence pulse indicates the DS1994 is ready to send or receive data given the correct ROM command and memory function command. The bus master transmits (Tx) a reset pulse (t_{RSTL}, minimum 480µs). The bus master then releases the line and goes into receive mode (Rx). The 1-Wire bus is pulled to a high state through the pullup resistor. After detecting the rising edge on the data line, the DS1994 waits (t_{PDH}, 15µs to 60µs) and then transmits the presence pulse (t_{PDL}, 60µs to 240µs). There are special conditions if interrupts are enabled for which the bus master must check the state of the 1-Wire bus after being in the Rx mode for 480µs. These conditions are discussed in the *Interrupt* section.

READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 11. The master driving the data line low initiates all time slots. The falling edge of the data line synchronizes the DS1994 to the master by triggering a delay circuit in the DS1994. During write time slots, the delay circuit determines when the DS1994 samples the data line. For a read data time slot, if a 0 is to be transmitted, the delay circuit determines how long the DS1994 holds the data line low overriding the 1 generated by the master. If the data bit is a 1, the iButton leaves the read data time slot unchanged.

Figure 10. INITIALIZATION PROCEDURE RESET AND PRESENCE PULSES

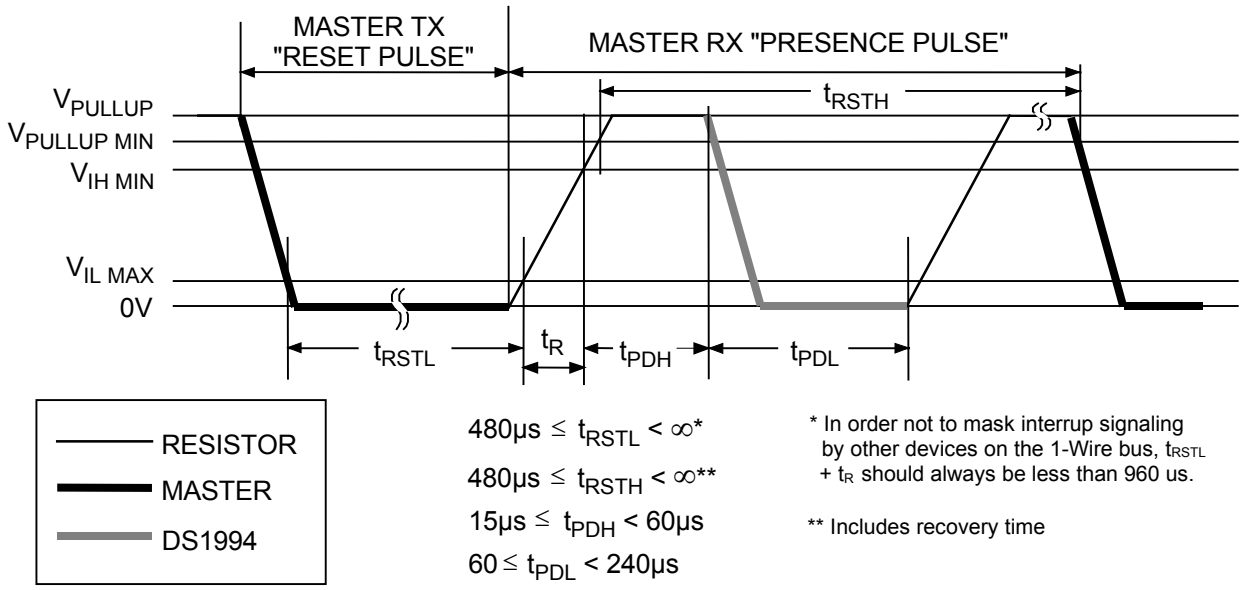


Figure 11. READ/WRITE TIMING DIAGRAM

Write-One Time Slot

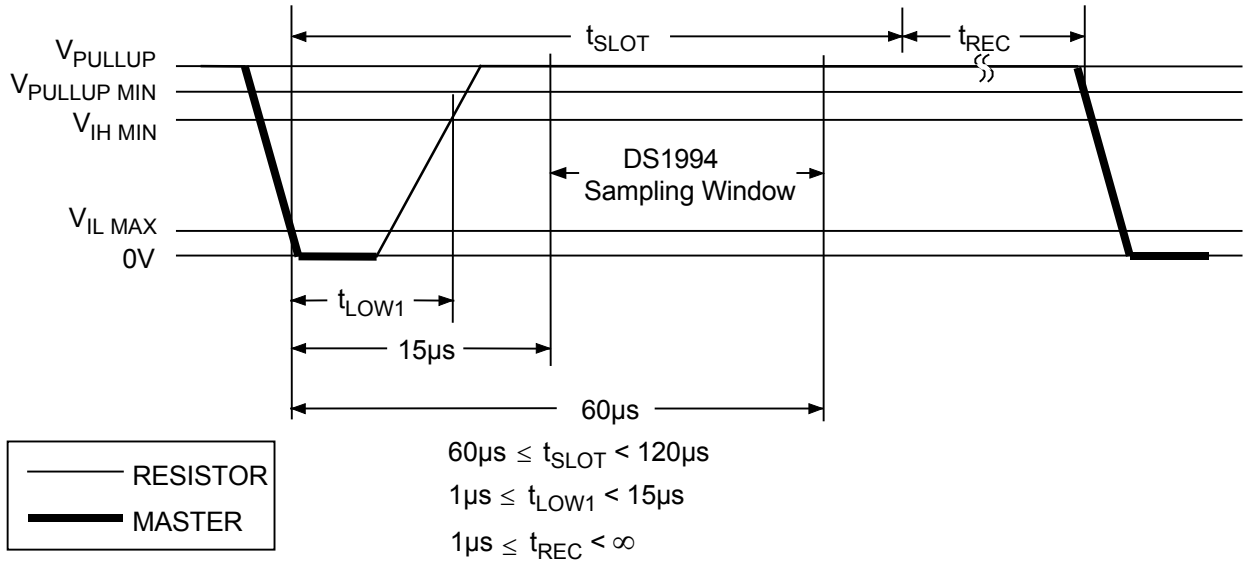
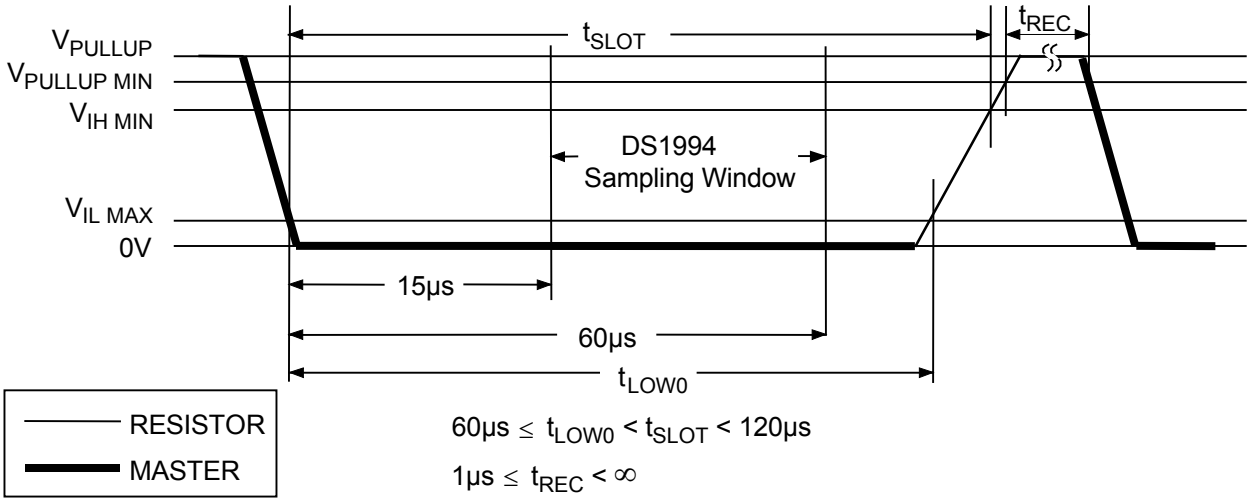
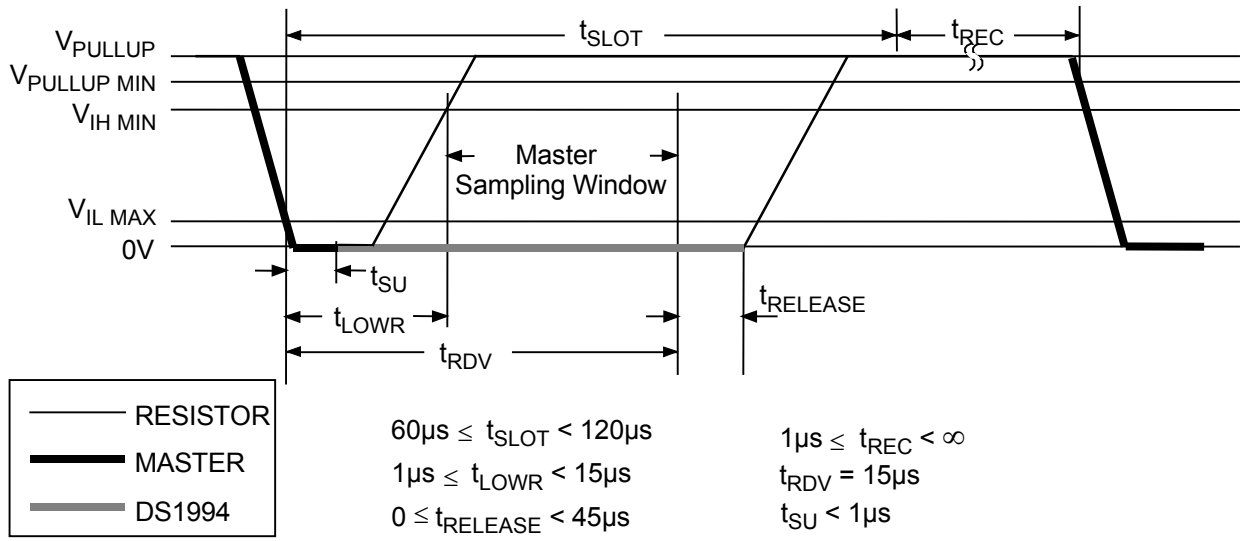


Figure 11. READ/WRITE TIMING DIAGRAM (continued)

Write-Zero Time Slot



Read-Data Time Slot



Interrupts

If the DS1994 detects an alarm condition, it automatically sets the corresponding alarm flag in the status register. An interrupt condition begins whenever any alarm flag is set and the flag's corresponding interrupt bit is enabled. The interrupt condition ceases when the alarm flags are cleared (i.e., the interrupt is acknowledged by reading the status register, address 200H) or if the corresponding interrupt enable bit is disabled.

The DS1994 can produce two types of interrupts: spontaneous interrupts, called type 1, and delayed interrupts, type 2. Spontaneous interrupts need to be armed by a reset pulse after all communication on the 1-Wire bus has finished. A single falling slope on the 1-Wire bus disarms this type of interrupt. If an alarm condition occurs while the device is disarmed, at first a type 2 interrupt is produced.

Spontaneous interrupts are signaled by the DS1994 by pulling the data line low for 960µs to 3840µs as the interrupt condition begins (Figure 12). After this long low pulse, a presence pulse follows. If the alarm condition occurs just after the master has sent a reset pulse, i.e., during the high or low time of the presence pulse, the DS1994 does not assert its interrupt pulse until the presence pulse is finished (Figure 13).

If the DS1994 cannot assert a spontaneous interrupt, either because the data line was not pulled high, communication was in progress, or the interrupt was not armed, it extends the next reset pulse to a total length of 960µs to 3840µs (delayed interrupt). If the alarm condition occurs during the reset low time of the reset pulse, the DS1994 immediately asserts its interrupt pulse; thus, the total low time of the pulse can be extended up to 4800µs (Figure 14). If a DS1994 with a not previously signaled alarm detects a power-on cycle on the 1-Wire bus, it sends a presence pulse and waits for the reset pulse sent by the master to extend it and to subsequently issue a presence pulse (Figure 15). As long as an interrupt has not been acknowledged by the master, the DS1994 continues sending interrupt pulses.

The interrupt signaling discussed so far is valid for the first opportunity the device has to signal an interrupt. It is not required for the master to acknowledge an interrupt immediately. If an interrupt is not acknowledged, the DS1994 continues signaling the interrupt with every reset pulse. To do so, the DS1994 either uses the waveform of the type 2 interrupt (Figure 14) or the waveform of the type 1A interrupt (Figure 13). The waveform of the type 2 interrupt is observed after a communication to a device other than the interrupting one; after successful communication to the interrupting device (without acknowledging the interrupt), the waveform of the type 1A interrupt is found.

Figure 12. TYPE 1 INTERRUPT

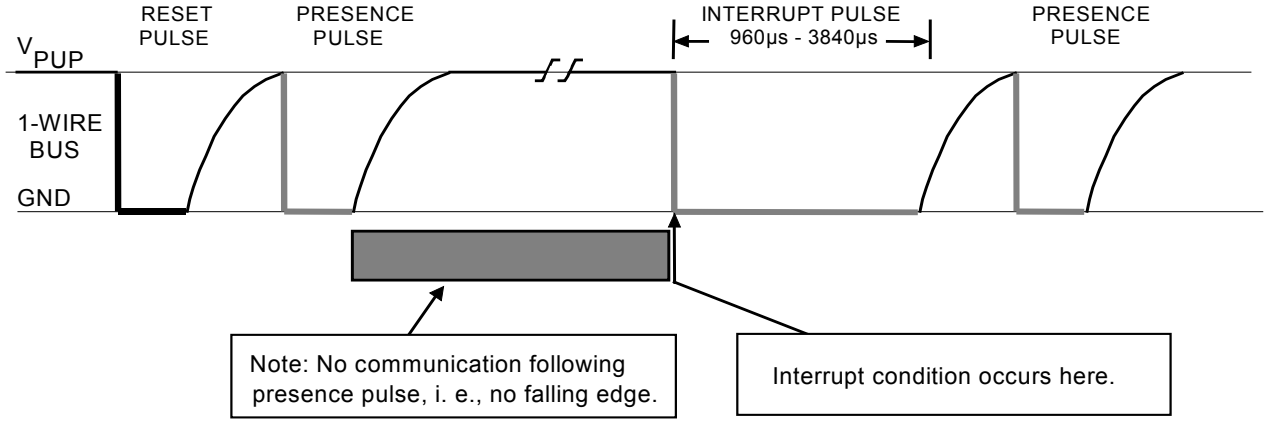


Figure 13. TYPE 1A INTERRUPT (SPECIAL CASE)

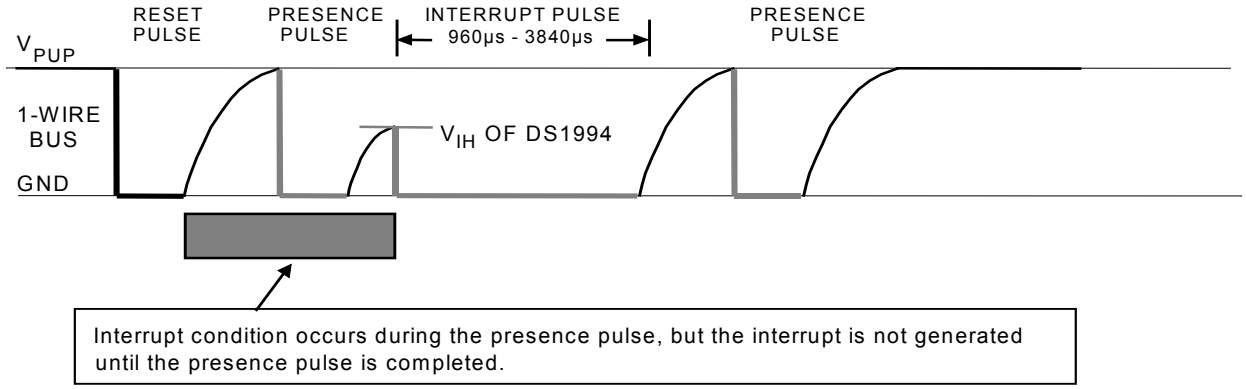


Figure 14. TYPE 2 INTERRUPT

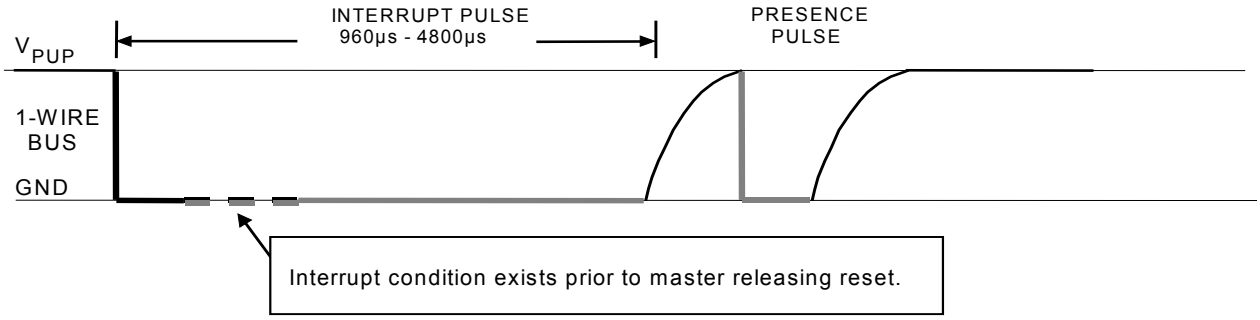
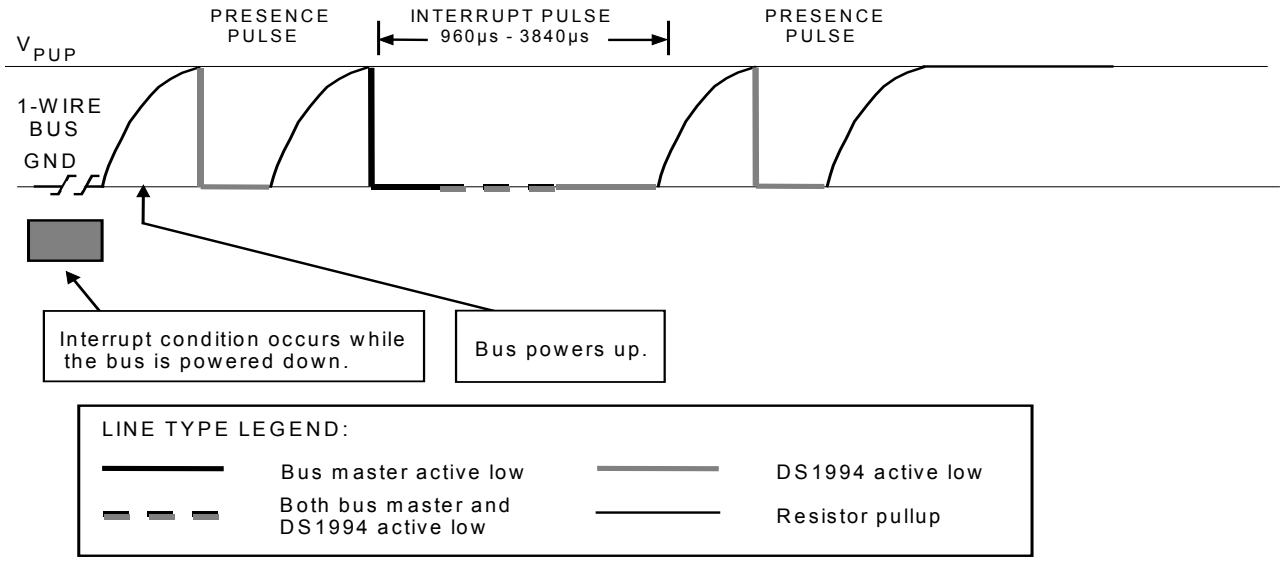


Figure 15. TYPE 2 INTERRUPT (SPECIAL CASE)



PHYSICAL SPECIFICATIONS

Size	See mechanical drawing
Weight	3.3 grams (F5 package)
Humidity	90% RH at 50°C
Altitude	10,000 feet
Expected Service Life	10 years at 25°C
Safety	Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus, Approved under Entity Concept for use in Class I, Division 1, Group A, B, C, and D Locations

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	-40°C to +70°C
Storage Temperature	-40°C to +70°C

** This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

DC ELECTRICAL CHARACTERISTICS

(V_{PUP} = 2.8V to 6.0V; -40°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Logic 1 (Note 1)	V_{IH}	2.2			V
Logic 0 (Note 1)	V_{IL}	-0.3		+0.8	V
Output Logic Low at 4mA (Note 1)	V_{OL}			0.4	V
Output Logic High (Notes 1, 2)	V_{OH}		V_{PUP}		V
Input Load Current (Note 3)	I_L		5		µA

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
I/O (1-Wire) (Notes 6, 8)	$C_{IN/OUT}$		100	800	pF

AC ELECTRICAL CHARACTERISTICS

(V_{PUP} = 2.8V to 6.0V; -40°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Time Slot	t_{SLOT}	60		120	µs
Write 1 Low Time	t_{LOW1}	1		15	µs
Write 0 Low Time	t_{LOW0}	60		120	µs
Read Data Valid	t_{RDV}	exactly 15			µs
Release Time	$t_{RELEASE}$	0	15	45	µs
Read Data Setup (Note 5)	t_{SU}			1	µs
Interrupt	t_{INT}	960		4800	µs
Recovery Time	t_{REC}	1			µs
Reset Time High (Note 4)	t_{RSTH}	480			µs

Reset Time Low (Note 7)	t_{RSTL}	480		960	µs
Presence Detect High	t_{PDH}	15		60	µs
Presence Detect Low	t_{PDL}	60		240	µs

Note 1: All voltages are referenced to ground.
Note 2: V_{PUP} = external pullup voltage.
Note 3: Input load is to ground.
Note 4: An additional reset or communication sequence cannot begin until the reset high time has expired.
Note 5: Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1µs of this falling edge and remains valid for 14µs minimum. (15µs total from falling edge on 1-Wire bus.)
Note 6: Capacitance on the data line could be 800pF when power is first applied. If a 5kΩ resistor is used to pull up the data line to V_{PUP}, 5µs after power has been applied, the parasite capacitance does not affect normal communications.
Note 7: The reset low time (t_{RSTL}) should be restricted to a maximum of 960µs to allow interrupt signaling; otherwise, it could mask or conceal interrupt pulses.
Note 8: Guaranteed by design, not production tested.