DS1258W
3.3V 128k x 16 Nonvolatile SRAM

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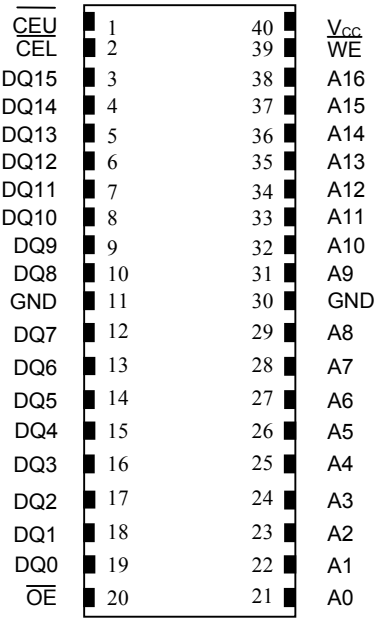
FEATURES

- 10-Year Minimum Data Retention in the Absence of External Power
- Data is Automatically Protected During a Power Loss
- Separate Upper Byte and Lower Byte Chip Select Inputs
- Unlimited Write Cycles
- Low-Power CMOS
- Read and Write Access Times as Fast as 100ns
- Lithium Energy Source is Electrically Disconnected to Retain Freshness Until Power is Applied for the First Time
- Optional Industrial Temperature Range of -40°C to +85°C, Designated IND

PIN ASSIGNMENT



40-Pin Encapsulated Package
740mil Extended

PIN DESCRIPTION

A0 - A16	- Address Inputs
DQ0 - DQ15	- Data In/Data Out
$\overline{CEU}$	- Chip Enable Upper Byte
$\overline{CEL}$	- Chip Enable Lower Byte
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
V_{CC}	- Power (+3.3V)
GND	- Ground

DESCRIPTION

The DS1258W 3.3V 128k x 16 Nonvolatile SRAM is a 2,097,152-bit, fully static, nonvolatile (NV) SRAM, organized as 131,072 words by 16 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry, which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. DIP-package DS1258W devices can be used in place of solutions which build nonvolatile 128k x 16 memory by utilizing a variety of discrete components. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing.

READ MODE

The DS1258W executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and either/both of $\overline{CEU}$ or $\overline{CEL}$ (Chip Enables) are active (low) and $\overline{OE}$ (Output Enable)is active (low). The unique address specified by the 17 address inputs (A0-A16) defines which of the 131,072 words of data is accessed. The status of $\overline{CEU}$ and $\overline{CEL}$ determines whether all or part of the addressed word is accessed. If $\overline{CEU}$ is active with $\overline{CEL}$ inactive, then only the upper byte of the addressed word is accessed. If $\overline{CEU}$ is inactive with $\overline{CEL}$ active, then only the lower byte of the addressed word is accessed. If both the $\overline{CEU}$ and $\overline{CEL}$ inputs are active (low), then the entire 16-bit word is accessed. Valid data will be available to the 16 data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CEU}$, $\overline{CEL}$ and $\overline{OE}$ access times are also satisfied. If $\overline{CEU}$, $\overline{CEL}$, and $\overline{OE}$ access times are not satisfied, then data access must be measured from the later-occurring signal, and the limiting parameter is either t_{CO} for $\overline{CEU}$, $\overline{CEL}$, or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1258W executes a write cycle whenever $\overline{WE}$ and either/both of $\overline{CEU}$ or $\overline{CEL}$ are active (low) after address inputs are stable. The unique address specified by the 17 address inputs (A0-A16) defines which of the 131,072 words of data is accessed. The status of $\overline{CEU}$ and $\overline{CEL}$ determines whether all or part of the addressed word is accessed. If $\overline{CEU}$ is active with $\overline{CEL}$ inactive, then only the upper byte of the addressed word is accessed. If $\overline{CEU}$ is inactive with $\overline{CEL}$ active, then only the lower byte of the addressed word is accessed. If both the $\overline{CEU}$ and $\overline{CEL}$ inputs are active (low), then the entire 16-bit word is accessed. The write cycle is terminated by the earlier rising edge of $\overline{CEU}$ and/or $\overline{CEL}$, or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CEU}$ and/or $\overline{CEL}$, and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

READ/WRITE FUNCTION Table 1

$\overline{OE}$	$\overline{WE}$	$\overline{CEL}$	$\overline{CEU}$	V_{CC} CURRENT	DQ0-DQ7	DQ8-DQ15	CYCLE PERFORMED
H	H	X	X	I_{CCO}	High-Z	High-Z	Output Disabled
L	H	L	L	I_{CCO}	Output	Output	Read Cycle
L	H	L	H		Output	High-Z	
L	H	H	L		High-Z	Output	
X	L	L	L	I_{CCO}	Input	Input	Write Cycle
X	L	L	H		Input	High-Z	
X	L	H	L		High-Z	Input	
X	X	H	H	I_{CCS}	High-Z	High-Z	Output Disabled

DATA RETENTION MODE

The DS1258W provides full functional capability for V_{CC} greater than 3.0V, and write-protects by 2.8V. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write-protect themselves, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 2.5V, a power-switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 2.5V, the power switching circuit

connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 3.0V.

FRESHNESS SEAL

Each DS1258W device is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than 3.0V, the lithium energy source is enabled for battery backup operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +4.6V
Operating Temperature Range	0°C to 70°C, -40°C to +85°C for Industrial Parts
Storage Temperature Range	-40°C to +70°C, -40°C to +85°C for Industrial Parts
Soldering Temperature	See IPC/JEDEC J-STD-020A Specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		0.4	V	

DC ELECTRICAL CHARACTERISTICS (t_A: See Note 10) (V_{CC} = 3.3V ± 0.3V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-2.0		+2.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.2V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CEU}$, $\overline{CEL}$ =2.2V	I_{CCS1}		100	450	µA	
Standby Current $\overline{CEU}$, $\overline{CEL}$ =V_{CC}-0.2V	I_{CCS2}		60	250	µA	
Operating Current	I_{CCO1}			100	mA	
Write Protection Voltage	V_{TP}	2.8	2.9	3.0	V	

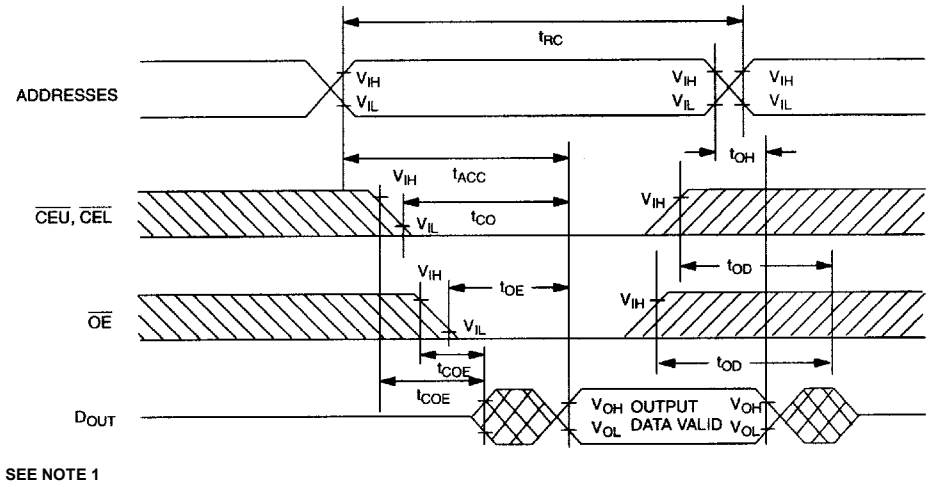
CAPACITANCE (t_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		20	25	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

DC ELECTRICAL CHARACTERISTICS (t_A: See Note 10) (V_{CC} = 3.3V ± 0.3V)

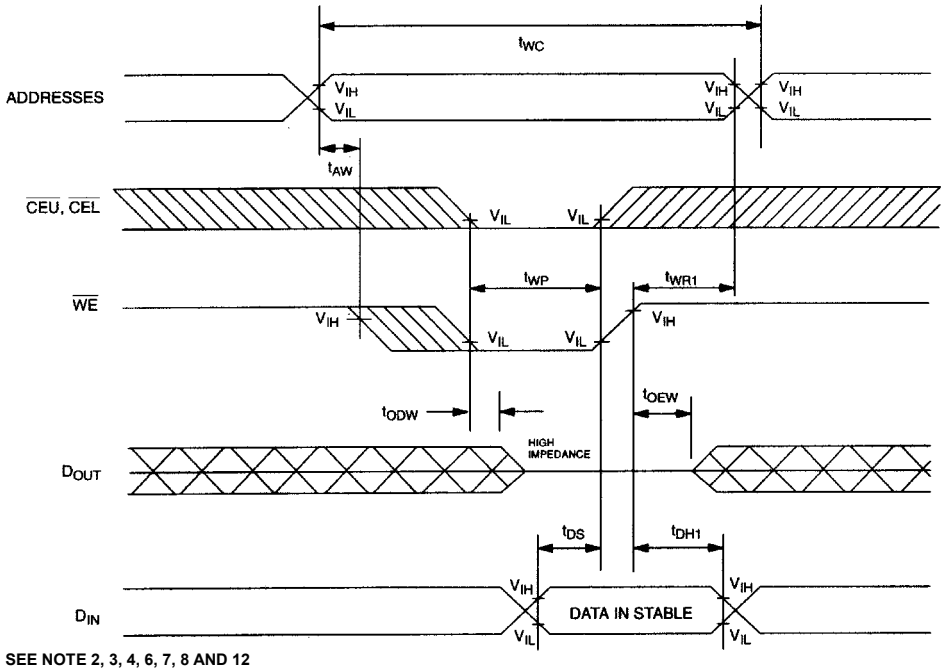
PARAMETER	SYMBOL	DS1258W-100		DS1258W-150		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	100		150		ns	
Access Time	t_{ACC}		100		150	ns	
$\overline{OE}$ to Output Valid	t_{OE}		50		70	ns	
$\overline{CE}$ to Output Valid	t_{CO}		100		150	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	t_{COE}	5		5		ns	5
Output High-Z from Deselection	t_{OD}		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	100		150		ns	
Write Pulse Width	t_{WP}	75		100		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	5 20		5 20		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	40		60		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 20		0 20		ns ns	12 13

READ CYCLE



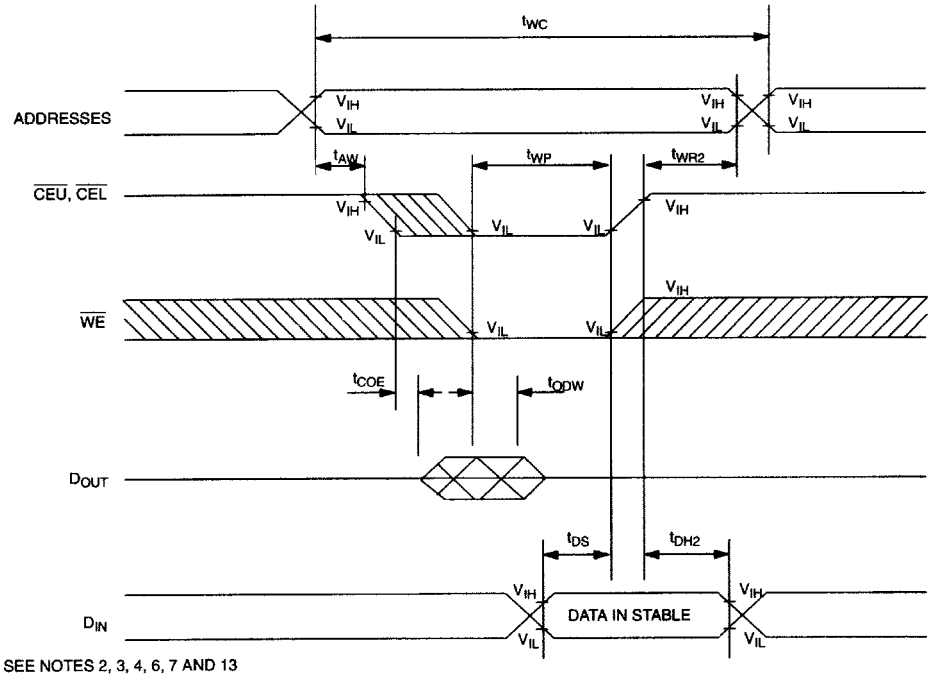
SEE NOTE 1

WRITE CYCLE 1



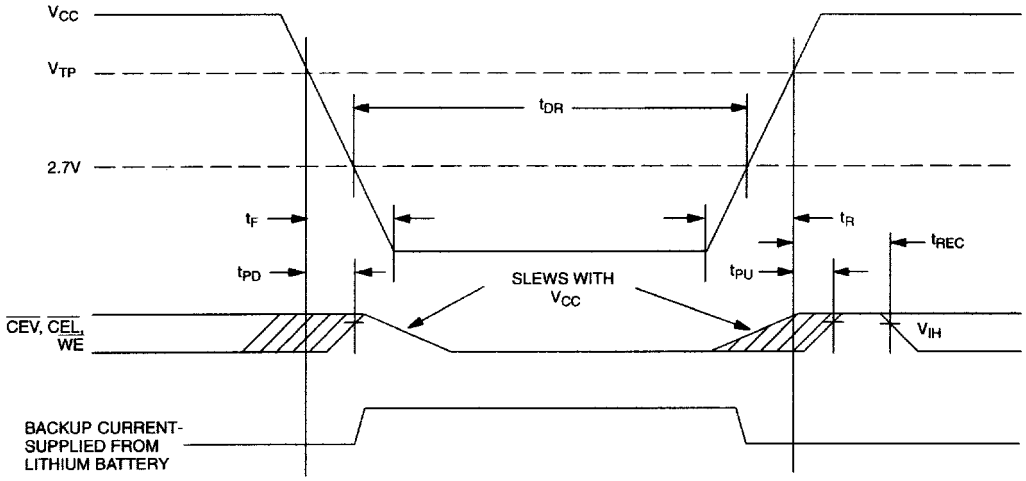
SEE NOTE 2, 3, 4, 6, 7, 8 AND 12

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7 AND 13

POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fail Detect to $\overline{CE}$ and $\overline{WE}$ Inactive	t_{PD}			1.5	µs	11
V_{CC} slew from V_{TP} to 0V	t_F	150			µs	
V_{CC} slew from 0V to V_{TP}	t_R	150			µs	
V_{CC} Valid to $\overline{CE}$ and $\overline{WE}$ Inactive	t_{PU}			2	ms	
V_{CC} Valid to End of Write Protection	t_{REC}			125	ms	

(t_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1) $\overline{WE}$ is high for a Read Cycle.
2) $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3) t_{WP} is specified as the logical AND of $\overline{CEU}$ or $\overline{CEL}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CEU}$, $\overline{CEL}$ or $\overline{WE}$ going low to the earlier of $\overline{CEU}$, $\overline{CEL}$ or $\overline{WE}$ going high.
4) t_{DS} is measured from the earlier of $\overline{CEU}$ or $\overline{CEL}$ or $\overline{WE}$ going high.
5) These parameters are sampled with a 5pF load and are not 100% tested.
6) If the $\overline{CEU}$ or $\overline{CEL}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in the output buffers remain in a high impedance state during this period.
7) If the $\overline{CEU}$ or $\overline{CEL}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state during this period.
8) If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CEU}$ or $\overline{CEL}$ low transition, the output buffers remain in a high impedance state during this period.
9) Each DS1258W has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10) All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0 to +70°C. For industrial products, this range is -40°C to +85°C.
11) In a power-down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12) t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
13) t_{WR2}, t_{DH2} are measured from $\overline{CEU}$ OR $\overline{CEL}$ going high.
14) DS1258W DIP modules are recognized by Underwriters Laboratory (U.L.®) under file E99151.

DC TEST CONDITIONS

Outputs Open
Cycle = 200ns
All voltages are referenced to ground

AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels:
0.0V to 2.7V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input pulse Rise and Fall Times: 5ns

ORDERING INFORMATION

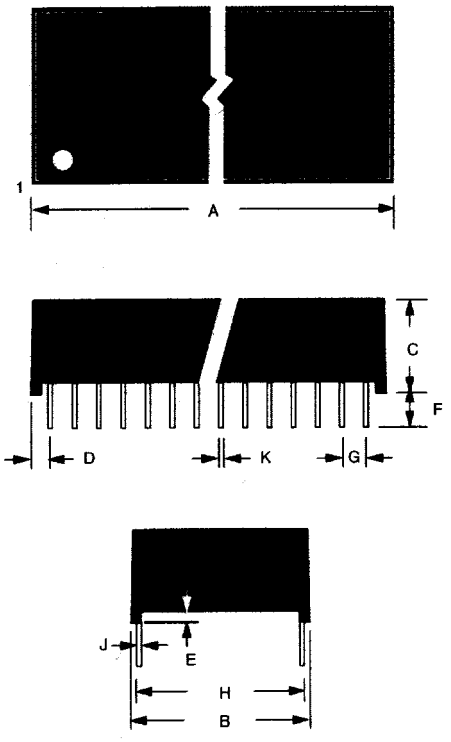
DS1258 WP - SSS - III

Operating Temperature Range
blank: 0° to +70°C
IND: -40° to +85°C

Access Speed
100: 100ns
150: 150ns

Package Type
blank: 40-pin (600mil) DIP

DS1258W NONVOLATILE SRAM 40-PIN, 740-MIL EXTENDED MODULE



PKG	40-PIN	
DIM	MIN	MAX
A IN.	2.080	2.100
MM	52.83	53.34
B IN.	0.715	0.740
MM	18.16	18.80
C IN.	0.345	0.365
MM	8.76	9.27
D IN.	0.085	0.115
MM	2.16	2.92
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.025
MM	0.43	0.58