DS1085

EconOscillator Frequency Synthesizer

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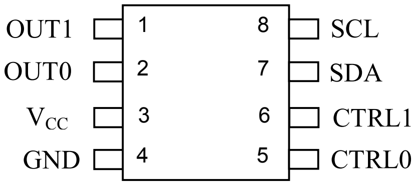
FEATURES

- User-Programmable Frequency Synthesizer
- Programmable From 8.1kHz to 133MHz
- Dual Synchronous Outputs
- 8.2MHz to 133MHz Reference Oscillator Output
- 8.1kHz to 133MHz Main Oscillator Output
- Three Resolution Options
- 2-Wire Serial Interface
- 0.75% Absolute Accuracy
- Nonvolatile (NV) Frequency Settings
- Single 5V Supply
- No External Timing Components
- Power-Down Mode

PIN ASSIGNMENT



SO (150mil)

PIN DESCRIPTION

OUT1	- Main Oscillator Output
OUT0	- Reference Oscillator Output
V_{CC}	- Power-Supply Voltage
GND	- Ground
CTRL1	- Control Pin for OUT1
CTRL0	- Control Pin for OUT0
SDA	- 2-Wire Serial Data Input/Output
SCL	- 2-Wire Serial Clock

ORDERING INFORMATION

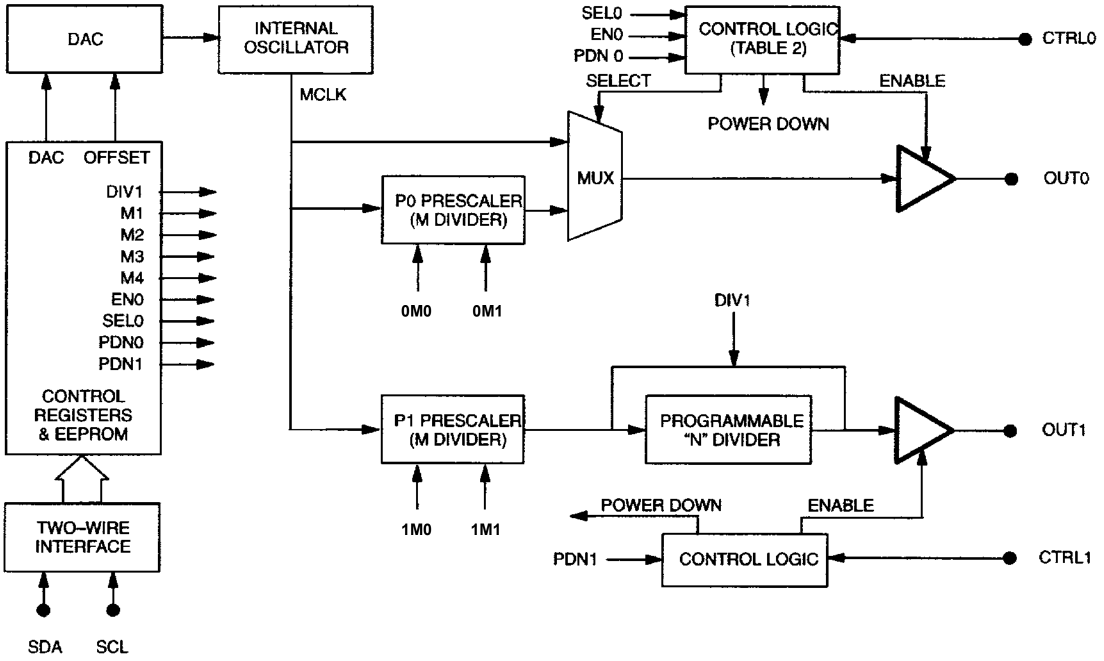
DEVICE	PACKAGE	STEP SIZE	OSCILLATOR OUTPUT RANGE
DS1085Z-10	150mil SO	10kHz	8.1kHz to 133MHz
DS1085Z-25	150mil SO	25kHz	8.1kHz to 133MHz
DS1085Z-50	150mil SO	50kHz	8.1kHz to 133MHz

DESCRIPTION

The DS1085 is a dual-output frequency synthesizer requiring no external timing components for operation. It can be used as a standalone oscillator or as a dynamically programmed, processor-controlled peripheral device. An internal master oscillator can be programmed from 66MHz to 133MHz with three resolution options of 10kHz, 25kHz, and 50kHz. A programmable, 3-bit prescaler (divide-by-1, 2, 4, or 8) permits the generation of a reference oscillator output (OUT0) from the master, ranging from 8.2MHz to 133MHz. A second independent prescaler and a 1-to-1025 divider allows the generation of a main oscillator output (OUT1) from 8.1kHz to 133MHz. The two outputs, although synchronous with the master, can be independently programmed. The combination of programmable master oscillator, prescalers, and dividers allows the generation of thousands of user-specified frequencies. All master oscillator, prescaler, and divider settings are stored in NV (EEPROM) memory, providing a default value on power-up that allows it to be used as a standalone oscillator. A 2-wire serial interface allows in-circuit, on-the-fly programming of the master oscillator, prescalers (P0 and P1), and divider (N). This allows dynamic frequency modification, if required, or, for fixed-frequency applications, the DS1085 can be used with factory- or user-programmed values.

External control inputs, CTRL1 and CTRL0, enable or disable the two oscillator outputs. Both outputs feature a synchronous enable that ensures no output glitches when the output is enabled and a constant time interval (for a given frequency setting) from an enable signal to the first output transition. These inputs also can be configured to disable the master oscillator, putting the device into a low-power mode for power-sensitive applications.

Figure 1. DS1085 BLOCK DIAGRAM



OVERVIEW

A block diagram of the DS1085 is shown in Figure 1. The DS1085 consists of five major components:

- Master oscillator control DAC
- Internal master oscillator (66MHz to 133MHz)
- Prescalers (divide-by-1, 2, 4, or 8)
- Programmable divider (divide-by-1 to 1025)
- Control registers

The internal master oscillator provides the reference clock (MCLK), which is fed to the prescalers and programmable dividers. The frequency of the oscillator can be user-programmed over a two-to-one range in increments equal to the step size, by means of a 10-bit control DAC. The master oscillator range is 66MHz to 133MHz, which is larger than the range possible with the 10-bit DAC resolution and available step sizes. Therefore, an additional register (OFFSET) is provided that can be used to select the range of frequency over which the DAC is used (see Table 1).

Table 1. DEVICE COMPARISONS BY PART NUMBER

PART NUMBER	STEP SIZE (kHz)	DAC SPAN (MHz)	OFFSET SIZE (MHz)
DS1085Z-10	10	10.24	5.12
DS1085Z-25	25	25.60	6.40
DS1085Z-50	50	51.20	6.40

For further description of use of the OFFSET register, see the *REGISTER FUNCTIONS* section.

The master clock can be routed directly to the outputs (OUT0 and OUT1) or through separate prescalers (P0 and P1). In the case of OUT1, an additional programmable divider (N) can be used to generate frequencies down to 8.1kHz.

The prescaler (P0) divides MCLK by 1, 2, 4, or 8 before routing MCLK to the reference output (OUT0) pin.

The prescaler (P1) divides MCLK by 1, 2, 4, or 8 before routing MCLK to the programmable divider (N), and, ultimately, the main output (OUT1) pin.

The programmable divider (N) divides the prescaler output (P1) by any number selected between two and 1025 (10 bits) to provide the main output (OUT1), or it can be bypassed altogether by use of the DIV1 register bit. The value of N is stored in the DIV register.

The control registers are user-programmable through a 2-wire serial interface to determine operating frequency (values of DAC, OFFSET, P0, P1, and N) and modes of operation. Once programmed, the register settings are nonvolatile and only need reprogramming if it is desired to reconfigure the device.

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	OUT1	This main oscillator output frequency is determined by the control register settings for the oscillator (DAC and OFFSET), prescaler P1 (mode bits 1M0 and 1M1), and divider N (DIV).
2	OUT0	The reference output is taken from the output of the reference select mux. Its frequency is determined by the control register settings for prescaler P0 (mode bits 0M0 and 0M1) (see Table 2).
3	V_{CC}	Power Supply
4	GND	Ground
5	CTRL0	A multifunction control input pin that can be programmed to function as a mux select, output enable, and/or a power-down. Its function is determined by the user-programmable control register values of EN0, SEL0, and PDN0 (see Table 2).
6	CTRL1	A multifunction control input pin that can be programmed to function as an output enable and/or a power-down. Its function is determined by the user-programmable control register value of PDN1 (see Table 3).
7	SDA	I/O pin for the 2-wire serial interface used for data transfer.
8	SCL	Input pin for the 2-wire serial interface used to synchronize data movement over the serial interface.

Table 2. DEVICE MODE USING OUT0

EN0 (BIT)	SEL0 (BIT)	PDN0 (BIT)	CTRL0 (PIN)	OUT0 (PIN)	CTRL0 FUNCTION	DEVICE MODE
0	0	0	1	High-Z	Power-Down*	Power-Down***
			0	High-Z		Active
0	1	0	1	MCLK/M	Mux Select	Active
			0	MCLK		
1	0	0	1	High-Z	Output Enable	Active
			0	MCLK		
1	1	0	1	High-Z	Output Enable	Active**
			0	MCLK/M		
X	0	1	1	High-Z	Power-Down	Power-Down
			0	MCLK		Active
X	1	1	1	High-Z	Power-Down	Power-Down
			0	MCLK/M		Active

**This mode is for applications where OUT0 is not used, but CTRL0 is used as a device shutdown.*
***Factory default setting.*
****See standby (power-down) current specification for power-down current range.*

Table 3. DEVICE MODE USING OUT1

PDN1 (BIT)	CTRL1 (PIN)	CTRL1 FUNCTION	OUT1 (PIN)	DEVICE MODE
0	0	Output Enable	OUT CLK	Active*
0	1		High-Z	
1	0	Power-Down	OUT CLK	Active
1	1		High-Z	Power-Down

**Factory default setting.*

NOTE:

Both CTRL0 and CTRL1 can be configured as power-downs. They are internally “OR” connected so either of the control pins can be used to provide a power-down function for the whole device, subject to appropriate settings of the PDN0 and PDN1 register bits (see Table 4).

Table 4. SHUTDOWN CONTROL WITH PDN0 AND PDN1

PDN0 (BIT)	PDN1 (BIT)	SHUTDOWN CONTROL
0	0	NONE
0	1	CTRL1
1	0	CTRL0
1	1	CTRL1 OR CTRL0

REGISTER FUNCTIONS

The user-programmable registers can be used to determine the mode of operation (MUX), operating frequency (DAC, OFFSET, DIV), and bus settings (ADDR). The functions of the registers are described in this section, but details of how these registers are programmed can be found in a later section. The register settings are nonvolatile, with the values being stored automatically or as required in EEPROM when the registers are programmed through the SDA and SCL pins.

DAC WORD (Address 08h)

MSB							LSB	MSB							LSB
d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	X	X	X	X	X	X
First Data Byte								Second Data Byte							

X = Don't care.

The DAC word (d0–d9) controls the frequency of the master oscillator. The resolution of this register depends on the step size of the device. The absolute frequency of the device also depends on the value of the OFFSET register (see Table 5 and 6).

Table 5. DEFAULT DAC SETTINGS

DS1085Z-10			DS1085Z-25			DS1085Z-50		
Frequency	**DAC**	**Offset**	**Frequency**	**DAC**	**Offset**	**Frequency**	**DAC**	**Offset**
97.1MHz	500	OS	104.6MHz	600	OS	101.8MHz	500	OS

For any given value of OFFSET the master oscillator frequency can be derived as follows:

Frequency = Min Frequency + DAC x Step Size

where: Min frequency is the lowest frequency shown in Table 6 for the corresponding offset.
DAC is the value of the DAC register (0–1023).
Step size is the step size of the device (10kHz, 25kHz, or 50kHz).
OS is the decimal, integer value of the five MSBs of the RANGE register.

OFFSET BYTE (Address 0Eh)

MSB							LSB
X	X	X	O4	O3	O2	O1	O0

X = Don't care.

The OFFSET byte (O0–O4) determines the range of frequencies that can be obtained within the absolute minimum and maximum range of the oscillator. Correct operation of the device is not guaranteed for values of OFFSET not shown in Table 6.

Table 6. FREQUENCY vs. OFFSET

	DS1085Z-10	**DS1085Z-25**	**DS1085Z-50**
OFFSET	**FREQUENCY RANGE**	**FREQUENCY RANGE**	**FREQUENCY RANGE**
OS - 10	—	—	—
OS - 9	—	—	—
OS - 8	—	—	—
OS - 7	—	—	—
OS - 6	61.4 to 71.6	51.2 to 76.8	38.4 to 89.6
OS - 5	66.5 to 76.8	57.6 to 83.2	44.8 to 96.0
OS - 4	71.6 to 81.9	64.0 to 89.6	51.2 to 102.4
OS - 3	76.7 to 87.0	70.4 to 96.0	57.6 to 108.8
OS - 2	81.9 to 92.1	76.8 to 102.4	64.0 to 115.2
OS - 1	87.0 to 97.2	83.2 to 108.8	70.4 to 121.6
OS*	92.1 to 102.3	89.6 to 115.2	76.8 to 128.0
OS + 1	97.2 to 107.5	96.0 to 121.6	83.2 to 134.4
OS + 2	102.3 to 112.6	102.4 to 128.0	89.6 to 140.8
OS + 3	107.5 to 117.7	108.8 to 134.4	96.0 to 147.2
OS + 4	112.6 to 122.8	115.2 to 140.8	102.4 to 153.6
OS + 5	117.7 to 127.9	121.6 to 147.2	108.8 to 160.0
OS + 6	122.8 to 133.1	128.0 to 153.6	115.2 to 166.4

**OS is the OFFSET default setting. OS is the integer value of the five MSBs of RANGE register.*

These ranges include values outside the oscillator range of 66MHz to 133MHz. When using these ranges, values of DAC must be chosen to keep the oscillator within range. Correct operation of the device is not guaranteed outside the range 66MHz to 133MHz.

MUX WORD (Address 02h)

The MUX word controls several functions. Its bits are organized as follows:

	MSB							LSB	MSB							LSB
NAME	*****	**PDN1**	**PDN0**	**SEL0**	**EN0**	**0M1**	**0M0**	**1M1**	**1M0**	**DIV1**	**–**	**–**	**–**	**–**	**–**	**–**
Default Setting	0	0	0	1	1	0	0	0	0	0	X	X	X	X	X	X

**This bit must be set to zero.*
X = Don't care.

The functions of the individual bits are described in the following paragraphs.

DIV1 (Default Setting = 0)

This bit allows the output of the prescaler P1 to be routed directly to the OUT1 pin (DIV1 = 1). In this condition, the N divider is bypassed so the programmed value of N is ignored. If DIV1 = 0, the N divider functions normally.

EN0 (Default Setting = 1)

If EN0 = 1 and PDN0 = 0, the CTRL0 pin functions as an output enable for OUT0, the frequency of the output being determined by the SEL0 bit.

If PDN0 = 1, the EN0 bit is ignored, CTRL0 functions as a power-down, and OUT0 is always enabled on power-up, its frequency being determined by the SEL0 bit.

If EN0 = 0, the function of CTRL0 is determined by the SEL0 and PDN0 bits (see Table 2).

SEL0 (Default Setting = 1)

If SEL0 = 1 and EN0 = PDN0 = 0, the CTRL0 pin determines whether the prescaler is bypassed, controlling the output frequency.

If CTRL0 = 0, the output frequency equals MCLK.

If CTRL0 = 1, the output frequency equals MCLK/M.

If either EN0 or PDN0 = 1, the CTRL0 pin functions as an output enable or power-down and the SEL0 bit determines whether the prescaler is bypassed, thus controlling the output frequency.

If SEL0 = 0, the output is MCLK, the master clock frequency.

If SEL0 = 1, the output is the output frequency of the M prescaler (see Table 2).

PDN0 (Default Setting = 0)

If PDN0 = 1, CTRL0 performs a power-down function, regardless of the setting of the other bits.

If PDN0 = 0, the function of CTRL0 is determined by the values of EN0 and SEL0 (see Table 2).

0M0, 0M1, 1M0, 1M1 (Default Setting = 0)

These bits set the prescaler’s (P0 and P1) divide by number (M) to 1, 2, 4, or 8 (see Table 7a and 7b).

Table 7a. PRESCALER P0 DIVISOR M SETTINGS

0M1	0M0	PRESCALER P0 DIVISOR "M"
0	0	1*
0	1	2
1	0	4
1	1	8

**Factory Default Setting*

Table 7b. PRESCALER P1 DIVISOR M SETTINGS

1M1	1M0	PRESCALER P1 DIVISOR "M"
0	0	1*
0	1	2
1	0	4
1	1	8

**Factory Default Setting*

NOTE:

When EN0 = SEL0 = PDN0 = 0, CTRL0 also functions as a power-down. This is a special case for situations when OUT0 is not used. Under these conditions all the circuitry associated with OUT0 is powered down. OUT0 is powered down (see Table 2).

PDN1 (Default Setting = 0)

If PDN1 = 1, CTRL1 functions as a power-down (see Table 3).

If PDN1 = 0, CTRL1 functions as an output enable for OUT1 (see Table 3).

NOTES FOR OUTPUT ENABLE AND POWER-DOWN:

1) Both enables are "smart" and wait for the output to be low before going to High-Z.
2) A power-down sequence first disables both outputs before powering down the device.
3) On power-up, the outputs are disabled until the clock has stabilized (~8000 cycles).
4) In power-down mode the device cannot be programmed.
5) A power-down command must persist for at least two cycles of the lowest output frequency plus 10µs.

DIV WORD (N) (Address 01h)

MSB							LSB	MSB							LSB
N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	X	X	X	X	X	X
First Data Byte								Second Data Byte							

X = Don't care.

N

The DIV word sets the programmable divider. These 10 bits (N0–N9) determine the value of the programmable divider (N). The range of divisor values is from two to 1025, and is equal to the programmed value of N plus 2 (see Table 8).

Table 8. PROGRAMMABLE DIVISOR N VALUES

BIT VALUE	DIVISOR (N)
00000000 00XXXXXX	2*
00000000 01XXXXXX	3
—	—
—	—
—	—
—	—
11111111 11XXXXXX	1025

**Factory Default Setting*

ADDR BYTE (Address 0Dh)

MSB LSB

NAME	—	—	—	—	WC	A2	A1	A0
Factory Default	X	X	X	X	0	0	0	0

X = Don't care.

A2, A1, A0 (Default Setting = 000)

These are the device select bits that determine the 2-wire address of the device.

WC (Default Setting = 0)

This bit determines when/if the EEPROM is written to after register contents have been changed. If WC = 0, EEPROM is written automatically after a write register command. If WC = 1, the EEPROM is only written when the "WRITE" command is issued. In applications where the register contents are frequently rewritten, WC should be set to 1; otherwise, it is necessary to wait for an EEPROM write cycle to complete (up to 10ms) between writing to the registers. Regardless of the value of the WC bit, the value of the ADDR register (A2, A1, A0) is always written immediately to the EEPROM.

RANGE REGISTER (Address 37h)

MSB LSB

OS5	OS4	OS3	OS2	OS1	X	X	X	X	X	X	X	X	X	X	X

The first five bits of the RANGE register contain the default OFFSET value. The decimal value of the RANGE register is the value OS that is referred to in Table 6. The RANGE register is read-only.

COMMAND SET

Data and control information is read from and written to the DS1085 in the format shown in Figure 3. To write to the DS1085, the master issues the slave address of the DS1085 and the $R/\overline{W}$ bit is set to 0. After receiving an acknowledge, the bus master provides a command protocol. After receiving this protocol, the DS1085 issues an acknowledge, and then the master can send data to the DS1085. If the DS1085 is to be read, the master must send the command protocol as before, and then issue a repeat START condition and then the control byte again, this time with the $R/\overline{W}$ bit set to 1 to allow reading of the data from the DS1085. The command set for the DS1085 is as follows:

Access DAC [08h]

If $R/\overline{W}$ is 0, this command writes to the DAC register. After issuing this command, the next data byte values are written into the DAC register. If $R/\overline{W}$ is 1, the next data bytes read are the values stored in the DAC register. This is a 2-byte transfer, the first byte contains the eight MSBs, the second byte contains the two LSBs in the most significant positions of the data byte. The remaining six bits are ignored and can be written with any value (if read, these bits are 0).

Access OFFSET [0Eh]

If $R/\overline{W}$ is 0, this command writes to the OFFSET register. After issuing this command, the next data byte value is written into the OFFSET register. If $R/\overline{W}$ is 1, the next data byte read is the value stored in the OFFSET register. This is a single byte transfer of which only the five LSBs (last five bits) are used. The remaining three bits can be written with any value to complete the data byte (if read, these bits are 1).

Access DIV [01h]

If $R/\overline{W}$ is 0, this command writes to the DIV register. After issuing this command, the next data byte values are written into the DIV register. If $R/\overline{W}$ is 1, the next data bytes read are the values stored in the DIV register. This register has a 10-bit value. The upper eight bits are sent first, followed by a second byte that contains the two LSBs of the register value in the most significant positions of the data byte. The remaining six bits are ignored and can be set to any value (if read, these bits are 0).

Access MUX [02h]

If $R/\overline{W}$ is 0, this command writes to the MUX register. After issuing this command, the next data byte values are written into the MUX register. If $R/\overline{W}$ is 1, the next data bytes read are the values stored in the MUX register. This register has a 10-bit value. The upper eight bits are sent first, followed by a second byte that contains the two LSBs of the register value in the most significant positions of the data byte. The remaining six bits are ignored and can be set to any value (if read, these bits are 0).

Access ADDR [0Dh]

If $R/\overline{W}$ is 0, this command writes to the ADDR register. After issuing this command, the next data byte value is written into the ADDR register. If $R/\overline{W}$ is 1, the next data byte read is the value stored in the ADDR register. This is a single-byte transfer. This register has a 5-bit value, the first three bits of a write can be any value followed by the five active bits (if read, the first three bits are 0).

Access RANGE [37h]

If $R/\overline{W}$ is 1, the next data bytes read are the values stored in the RANGE register. This register has a 14-bit value. The upper eight bits are sent first, followed by a second byte that contains the five LSBs of the register value in the most significant positions of the data byte. The upper five MSBs of the first byte contain the OS value for the frequency adjust Table 6. The register is read-only.

Write E2 [3Fh]

If WC = 0, the EEPROM is automatically written to at the end of each write command. This is a DEFAULT condition. In this case, the command “WRITE E2” is not needed. If WC = 1, the EEPROM is only written to when the “WRITE E2” command is issued. On receipt of the “WRITE E2” command, the contents of the DIV and MUX registers are written into the EEPROM, thus locking in the register settings. This is a single-byte transfer.

EXCEPTION: The ADDR register is always automatically written to EEPROM after a write, regardless of the value of WC.

2-WIRE SERIAL DATA BUS

The DS1085 communicates through a 2-wire serial interface. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master." The devices that are controlled by the master are "slaves." A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The DS1085 operates as a slave on the 2-wire bus. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (see Figure 2):

- Data transfer can be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

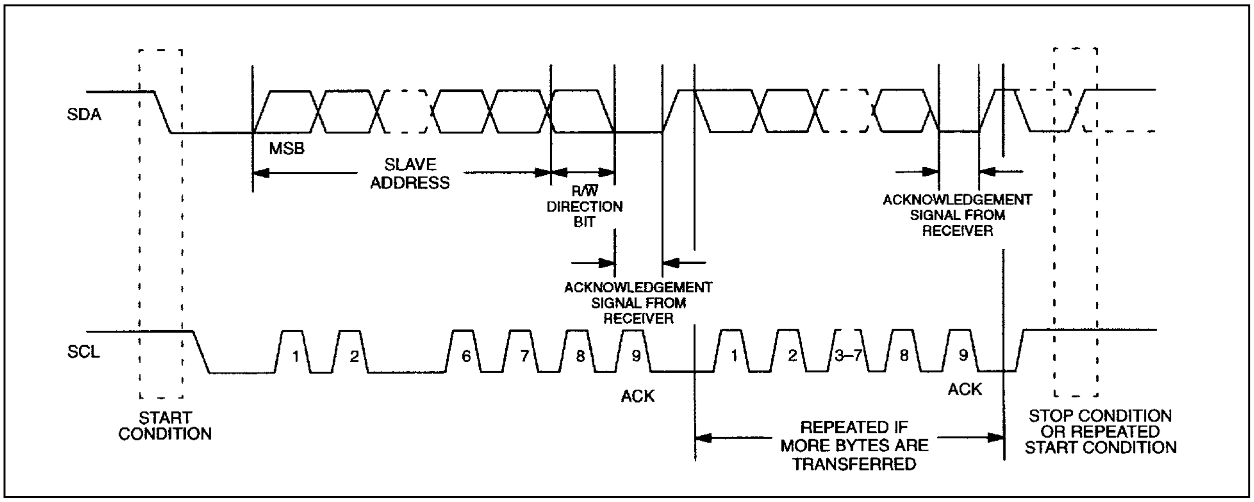
Within the bus specifications a regular mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The DS1085 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the byte has been received. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. When the DS1085 EEPROM is being written to, it is not able to perform additional responses. In this case, the slave DS1085 sends a not acknowledge to any data transfer request made by the master. It resumes normal operation when the EEPROM operation is complete.

A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 2. DATA TRANSFER ON 2-WIRE SERIAL BUS



Figures 2, 3, and 4 detail how data transfer is accomplished on the 2-wire bus. Depending upon the state of the R/W bit, two types of data transfer are possible:

1) **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

2) **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not acknowledge is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released.

The DS1085 can operate in the following two modes:

1) **Slave receiver mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.

2) **Slave transmitter mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1085 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

SLAVE ADDRESS

A control byte is the first byte received following the START condition from the master device. The control byte consists of a 4-bit control code; for the DS1085, this is set as 1011 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). The address bits to which the DS1085 responds are factory set to 000, but can be altered by writing new values to the ADDR register. After the new address is written, the DS1085 responds only to the new address bit values. The master uses this to select which of eight devices are to be accessed. The set bits are in effect the three LSBs of the slave address. The last bit of the control byte (R/W) defines the operation to be performed. When set to a 1, a read operation is selected; when set to a 0, a write operation is selected. Following the START condition, the DS1085 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the 1011 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line.

Figure 3. TIMING DIAGRAM

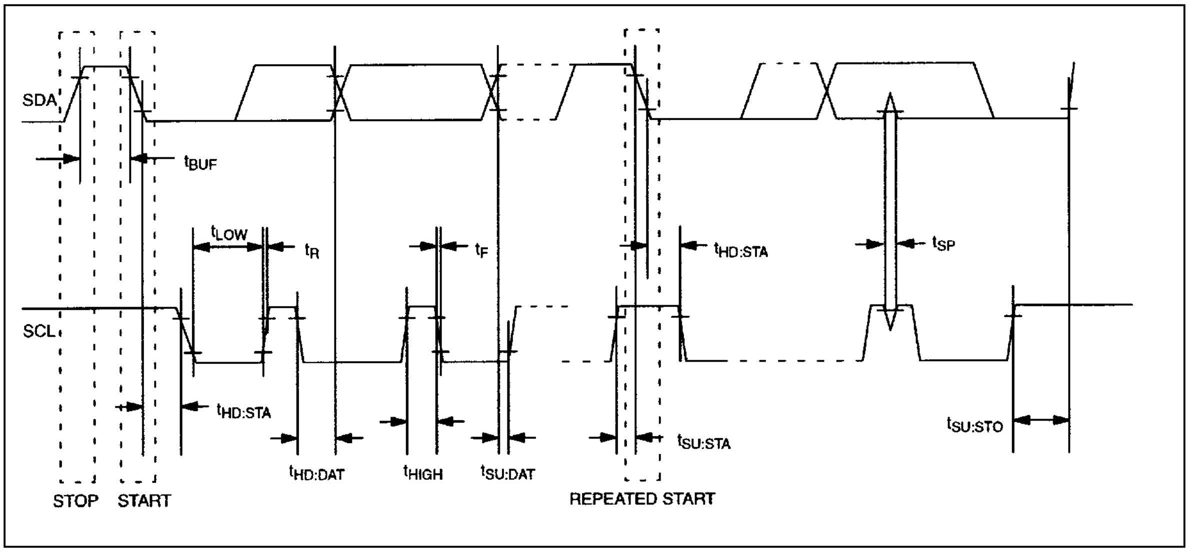
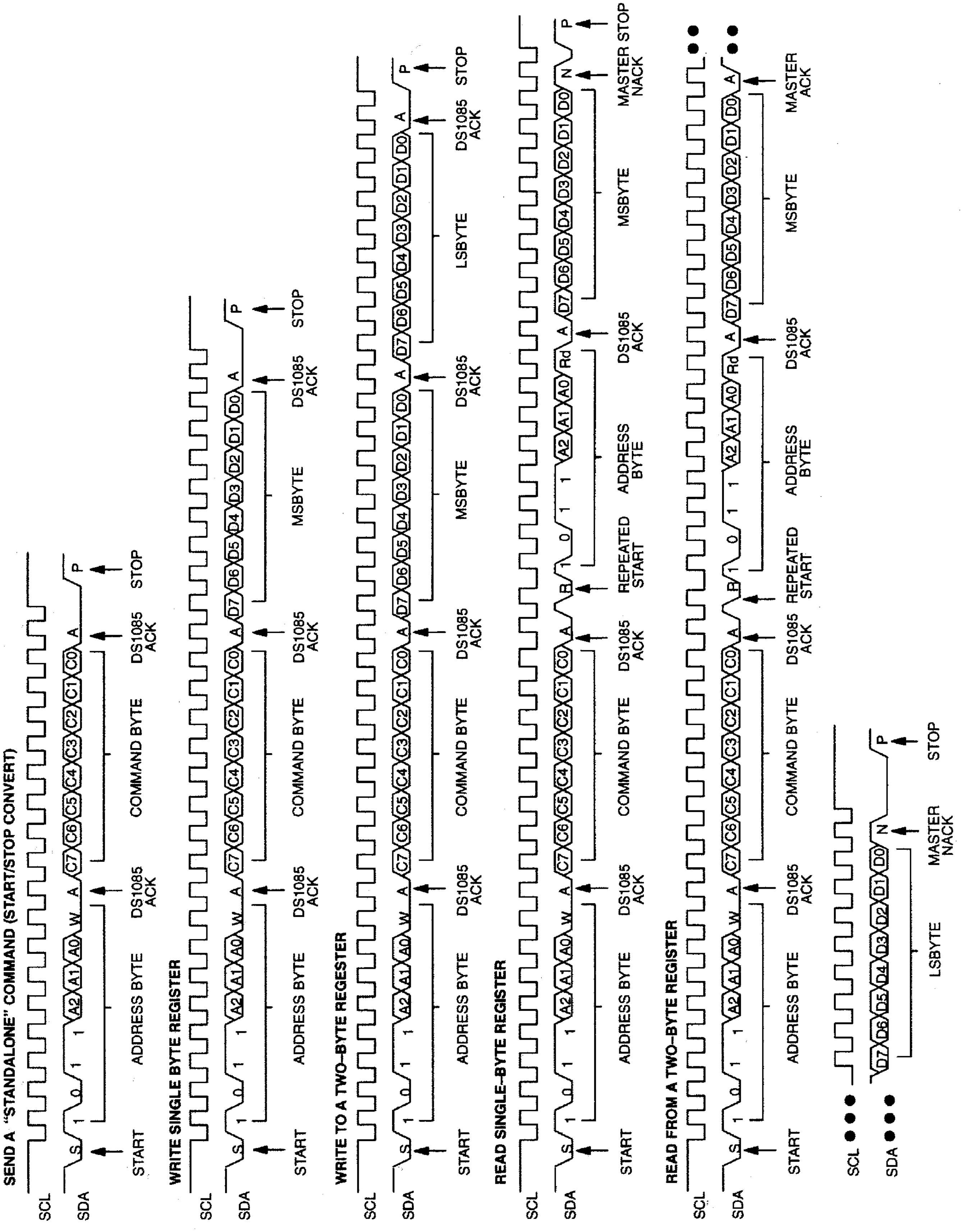


Figure 4. 2-WIRE SERIAL COMMUNICATION WITH DS1085



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.5V to +6.0V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See IPC/JEDEC J-STD-020A

** This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±5%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5	5.25	V	1
High-Level Output Voltage (OUT1, OUT0)	V_{OH}	I_{OH} = -4mA, V_{CC} = min	2.4			V	
Low-Level Output Voltage (OUT1, OUT0)	V_{OL}	I_{OL} = 4mA			0.4	V	
High-Level Input Voltage	V_{IH}	SDA, SCL	0.7 x Vcc		Vcc + 0.3	V	
		CTRL0,CTRL1	2				
Low-Level Input Voltage	V_{IL}	SDA, SCL	-0.3		0.3 x Vcc	V	
		CTRL0,CTRL1			0.8		
High-Level Input Current (CTRL1, CTRL0, SDA, SCL)	I_{IH}	V_{CC} = 5.25V			1	µA	
Low-Level Input Current (CTRL1, CTRL0, SDA, SCL)	I_{IL}	V_{IL} = 0	-1			µA	
Supply Current (Active)	I_{CC}	C_L = 15pF (both outputs, at default frequency)			50	mA	
Standby Current (Power-Down)	I_{CCQ}	Power-down mode			5	mA	

MASTER OSCILLATOR CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Master Oscillator Range	f_{OSC}		66		133	MHz	7
Default Master Oscillator Frequency	f_0	-10 Version -25 Version -50 Version		97.1 104.6 101.8		MHz	
Master Oscillator Frequency Tolerance	$\frac{\Delta f_0}{f_0}$	V_{CC} = 5V, T_A = +25°C				%	2, 17
		Default freq.	-0.75		+0.75		
		DAC step size	-0.75		+0.75		
Voltage Frequency Variation	$\frac{\Delta f_V}{f_0}$	Overvoltage range, T_A = +25°C				%	3
		default freq.	-1.0		+1.0		
		DAC Step Size	-1.0		+1.0		
Temperature Frequency Variation	$\frac{\Delta f_T}{f_0}$	Overtemperature range, V_{CC} = 5V default freq.	-0.5		+0.5	%	4, 5
		133MHz	-0.5		+0.5		
		66MHz	-1.0		+1.0		
Integral Nonlinearity of Frequency DAC	INL	DAC range	-0.3		+0.3	%	6
		Entire range	-0.4		+0.4	%	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Frequency Stable After DIV Change					1	Period	
Frequency Stable After DAC or OFFSET Change				0.2	1	ms	8
Power-Up Time	$t_{por} + t_{stab}$			0.1	0.5	ms	9
Enable of OUT0/1 After Exiting Power-Down Mode	t_{stab}				500	µs	
OUT0/1 High-Z After Entering Power-Down Mode	t_{stab}				1	ms	
Load Capacitance	C_L			15	50	pF	10
Output Duty Cycle (OUT0, OUT1)			40		60	%	

AC ELECTRICAL CHARACTERISTICS: 2-WIRE INTERFACE

(V_{CC} = 5V ±5%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
SCL Clock Frequency	f_{SCL}	Fast mode			400	kHz	14
		Standard mode			100		
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast mode	1.3			µs	
		Standard mode	4.7				
Hold Time (Repeated) START Condition	$t_{HD:STA}$	Fast mode	0.6			µs	11
		Standard mode	4.0				
LOW Period of SCL	t_{LOW}	Fast mode	1.3			µs	
		Standard mode	4.7				
HIGH Period of SCL	t_{HIGH}	Fast mode	0.6			µs	
		Standard mode	4.0				
Setup Time for a Repeated START	$t_{SU:STA}$	Fast mode	0.6			µs	
		Standard mode	4.7				
Data Hold Time	$t_{HD:DAT}$	Fast mode	0		0.9	µs	12, 13
		Standard mode	0				
Data Setup Time	$t_{SU:DAT}$	Fast mode	100			ns	14
		Standard mode	250				
Rise Time of Both SDA and SCL Signals	t_R	Fast mode	20 + $0.1C_B$		300	ns	15
		Standard mode			1000		
Fall Time of Both SDA and SCL Signals	t_F	Fast mode	20 + $0.1C_B$		300	ns	15
		Standard mode			1000		
Setup Time for STOP	$t_{SU:STO}$	Fast mode	0.6			µs	
		Standard mode	4.0				
Capacitive Load for each Bus Line	C_B				400	pF	15
NV Write-Cycle Time	t_{WR}				10	ms	16

NOTES:

1) All voltages are referenced to ground.
2) This is the absolute accuracy of the master oscillator frequency at the default settings.
3) This is the percent frequency change that is observed in output frequency with changes in voltage from nominal voltage at a temperature of T_A = +25°C.
4) This is the percentage frequency change from the +25°C frequency due to temperature at a nominal voltage of 5V.
5) The maximum temperature change varies with the master frequency setting. The minimum occurs at the default master frequency ($f_{default}$). The maximums occur at the extremes of the master oscillator frequency range (66MHz or 133MHz). (See Figure 5 below.)
6) The integral nonlinearity of the frequency adjust DAC is a measure of the deviation from a straight line drawn between the two endpoints of a range.
7) DAC and OFFSET register settings must be configured to maintain the clock frequency within this range. Correct operation of the device is not guaranteed if these limits are exceeded.
8) Frequency settles faster for small charges in value. During a change, the frequency changes smoothly from the original value to the new value.

9) This indicates the time taken between power-up and the outputs becoming active. An on-chip delay is intentionally introduced to allow the oscillator to stabilize. t_{stab} is equivalent to approximately 8000 clock cycles and hence depends on the programmed clock frequency.

10) Output voltage swings can be impaired at high frequencies combined with high-output loading.

11) After this period, the first clock pulse is generated.

12) A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH\ MIN}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

13) The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

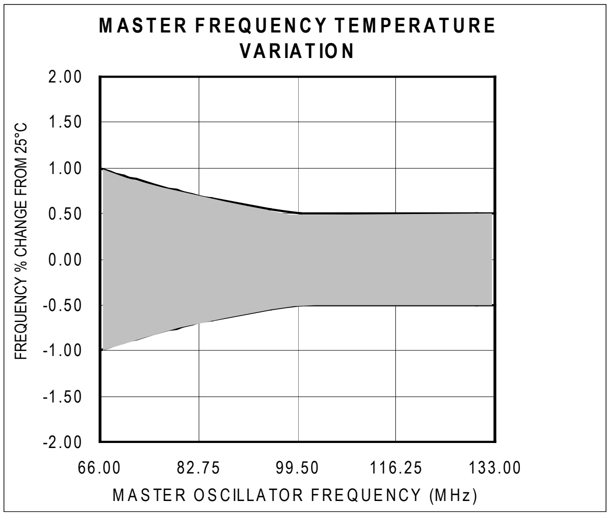
14) A fast-mode device can be used in a standard mode system, but the requirement $t_{SU:DAT} > 250$ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line at least $t_{R\ MAX} + t_{SU:DAT}$ = 1000ns + 250ns = 1250ns before the SCL line is released.

15) C_B—total capacitance of one bus line in picofarads; timing referenced to $0.9V_{CC}$ and $0.1V_{CC}$.

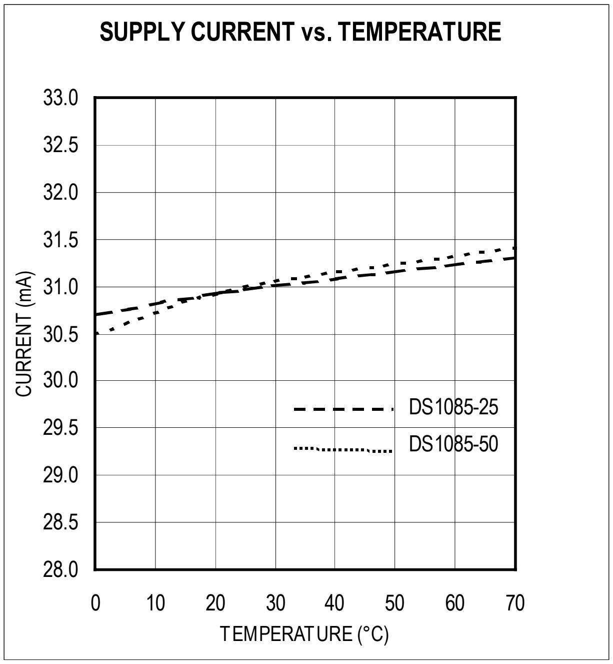
16) EEPROM write begins after a STOP condition occurs.

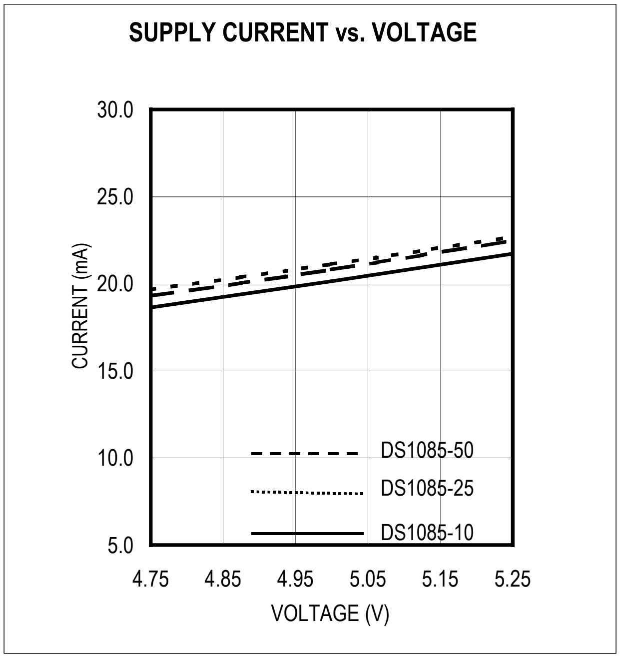
17) Typical frequency shift due to aging is ±0.5%. Aging stressing includes Level 1 moisture reflow preconditioning (24hr +125°C bake, 168hr 85°C/85%RH moisture soak, and 3 solder reflow passes +240 +0/-5°C peak) followed by 1000hr max V_{CC} biased 125°C HTOL, 1000 temperature cycles at -55°C to +125°C, 96hr 130°C/85%RH/5.5V HAST and 168hr 121°C/2 ATM Steam/Unbiased Autoclave.

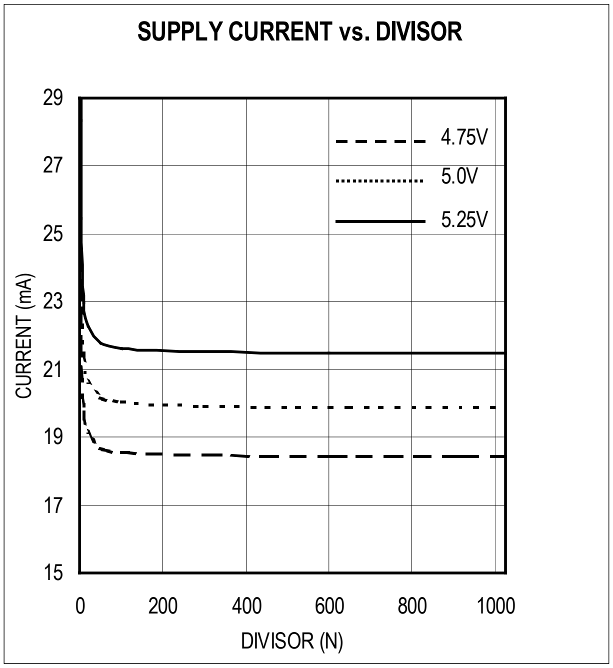
Figure 5. MASTER FREQUENCY TEMPERATURE VARIATION

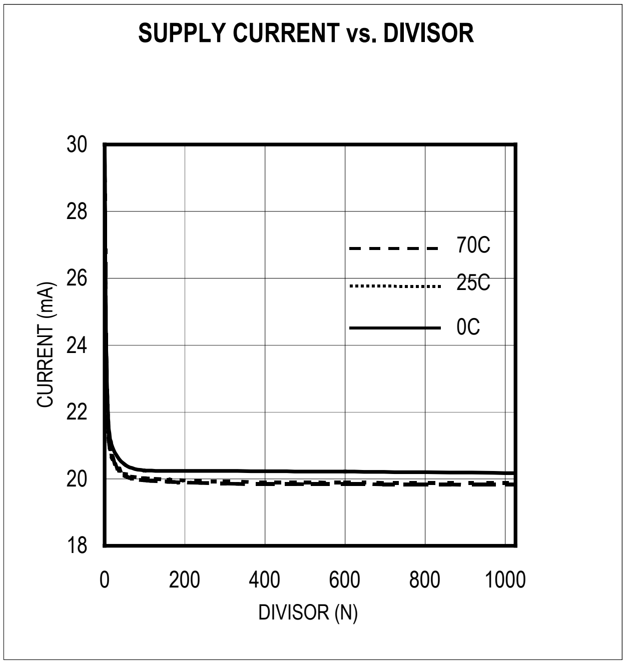


TYPICAL OPERATING CHARACTERISTICS (V_{CC} = 5V ±5%, T_A = 0°C to +70°C.)









TYPICAL OPERATING CHARACTERISTICS (continued)

(V_{CC} = 5V ± 5%, T_A = 0°C to +70°C.)