National Semiconductor

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DP8440-40/DP8440-25/DP8441-40/DP8441-25 microCMOS Programmable 16/64 Mbit Dynamic RAM Controller/Driver

General Description

The DP8440/41 Dynamic RAM Controllers provide an easy interface between dynamic RAM arrays and 8-, 16-, 32- and 64-bit microprocessors. The DP8440/41 DRAM Controllers generate all necessary control and timing signals to successfully interface and design dynamic memory systems. With significant enhancements over the DP8420/21/22 predecessors, the DP8440/41 are suitable for high performance memory systems. These controllers support page and burst accesses for fast page, static column and nibble DRAMs. Refreshes and accesses are arbitrated on chip. $\overline{RAS}$ low time during refresh and $\overline{RAS}$ precharge time are guaranteed by these controllers. Separate precharge counters for each $\overline{RAS}$ output avoid delayed back to back accesses due to precharge when using memory interleaving. Programmable features make the DP8440/41 DRAM Controllers flexible enough to fit many memory systems.

Features

- 40 MHz and 25 MHz operation
- Page detection
- Automatic CPU burst accesses
- Support 1/4/16/64 Mbits DRAMs
- High capacitance drivers for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and Q outputs
- Support for fast page, static column and nibble mode DRAMs
- High precision PLL based delay line
- Byte enable for word size up to 32 bits on the DP8440 or 64 bits on the DP8441
- Automatic Internal Refresh
- Staggered $\overline{RAS}$-Only refresh
- Burst and $\overline{CAS}$-before-$\overline{RAS}$ refresh
- Error scrubbing during refresh
- TRI-STATE® outputs
- Easy interface to all major microprocessors

Block Diagram

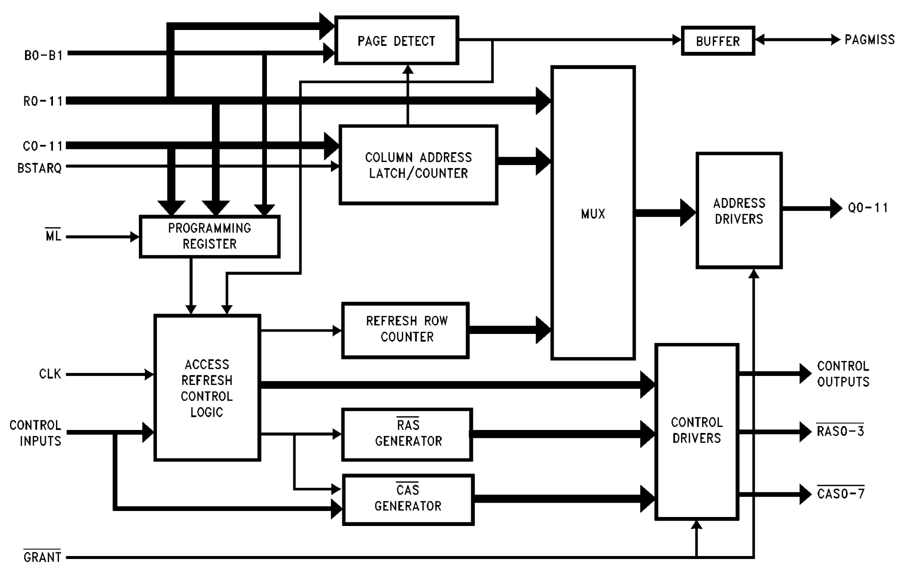

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FIGURE 1

DRAM Controller	Maximum Clock Frequency	Package Type	Bus Width Supporting	Largest DRAM Possible
DP8440V-40	40 MHz	84-Pin PLCC	8, 16, 32	16 Mbits
DP8440VLJ-40	40 MHz	100-Pin PQFP	8, 16, 32	16 Mbits
DP8440VLJ-25	25 MHz	100-Pin PQFP	8, 16, 32	16 Mbits
DP8441VLJ-40	40 MHz	100-Pin PQFP	8, 16, 32, 64	64 Mbits
DP8441VLJ-25	25 MHz	100-Pin PQFP	8, 16, 32, 64	64 Mbits

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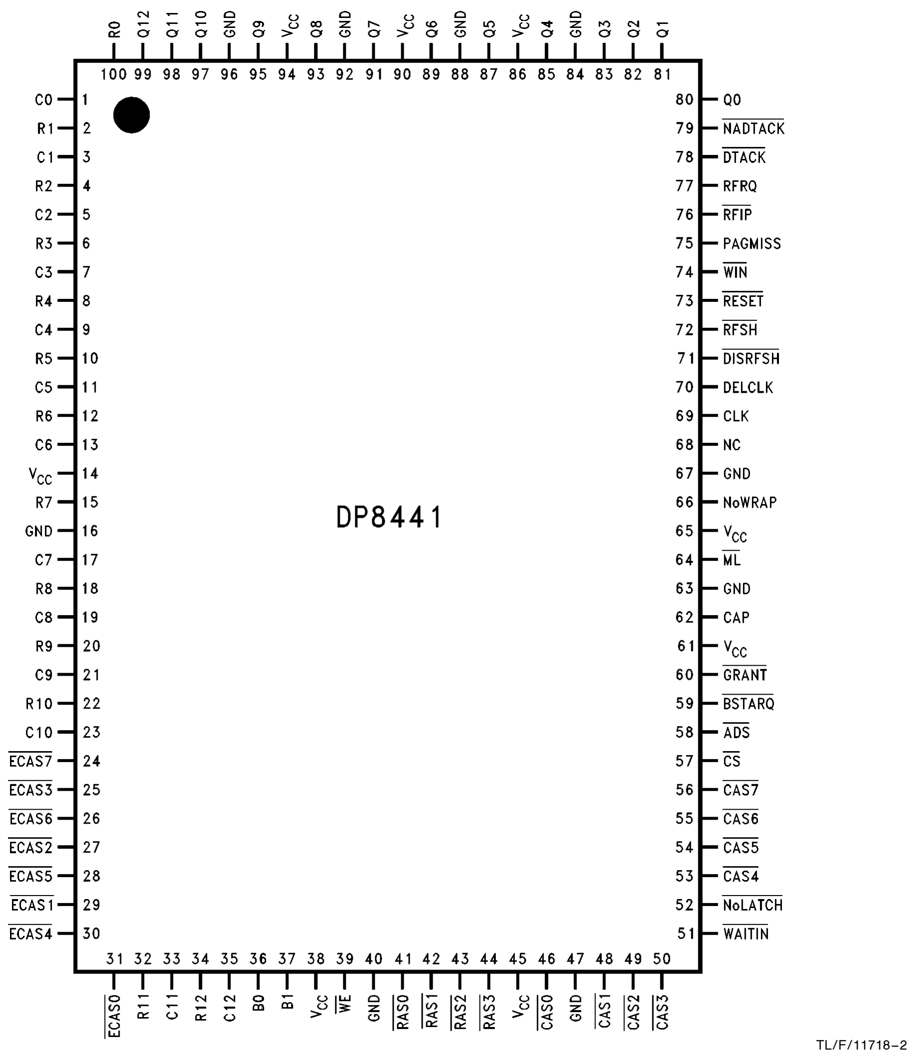
1.0 Connection Diagrams

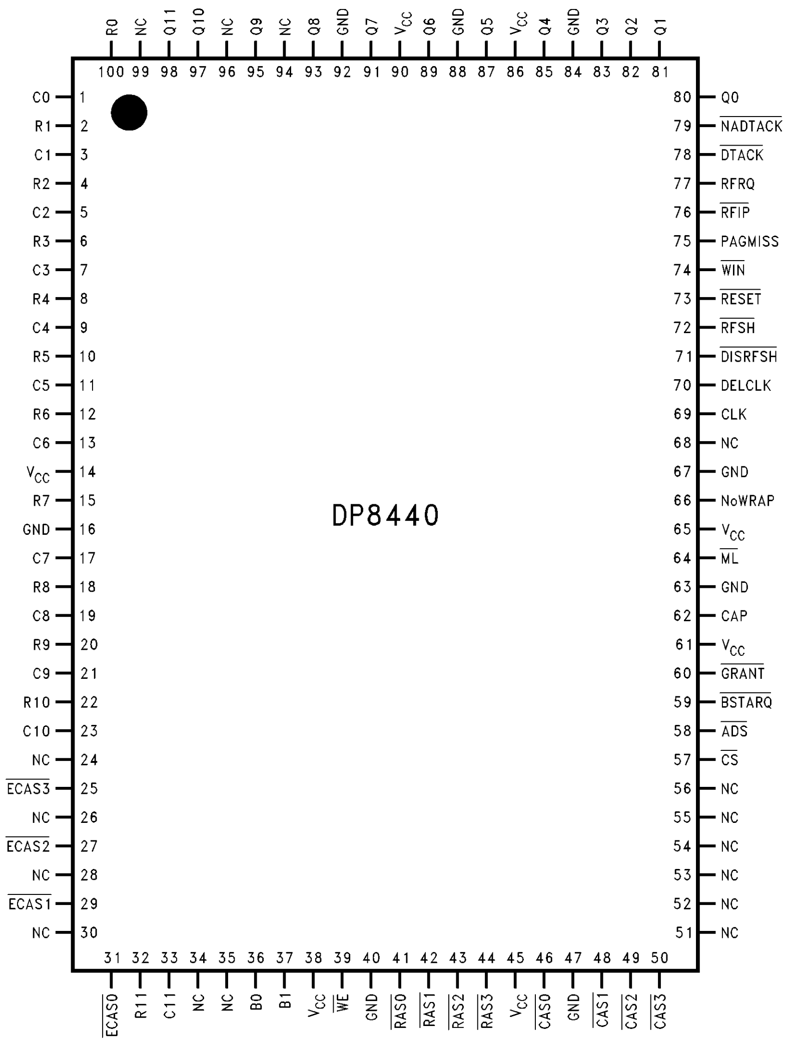


Top View

FIGURE 2

Order Number DP8441VLJ-40 (40 MHz Operation), DP8441VLJ-25 (25 MHz Operation)
See NS Package Number VLJ100A

1.0 Connection Diagrams (Continued)



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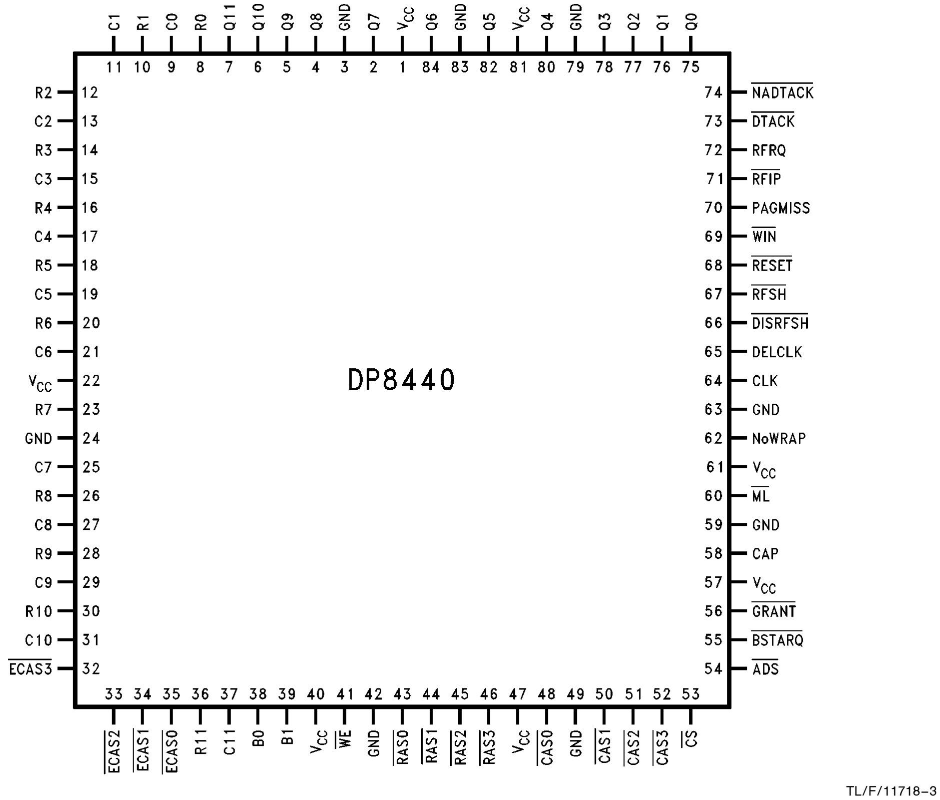
Top View

FIGURE 3

Order Number DP8440VLJ-40 (40 MHz Operation), DP8440VLJ-25 (25 MHz Operation)
See NS Package Number VLJ100A

1.0 Connection Diagrams (Continued)



Top View

FIGURE 4

Order Number DP8440V-40 (40 MHz Operation)
See NS Package Number V84A

2.0 Functional Introduction

Reset and Programming: After the power up, the DP8440/41 must be reset and programmed before it can be used to access the DRAM. The chip is programmed through the address bus.

Initialization Period: After programming, the DP8440/41 enter a 60 ms initialization period. During this time the DP8440/41 perform refreshes to the DRAM. Further warm up cycles are unnecessary. The user must wait until the initialization is over to access the memory.

Modes of Operation: The DP8440/41 are synchronous DRAM controllers. Every access is synchronized to the system clock. The controllers can be programmed in Page Mode or Normal Mode. Burst accesses are dynamically requested through the input BSTARQ.

Opening Access: They involve a new row address. Regardless of the access mode programmed, opening accesses behave in the same way. $\overline{ADS}$ and $\overline{CS}$ initiate and qualify every access. After asserting the $\overline{ADS}$, the DP8440/41 will assert $\overline{RAS}$ from the next rising edge of the CLK. The DP8440/41 will hold the row address on the DRAM address bus and guarantee that the row address is held for the Row Address Hold Time (t_{RAH}) programmed. The DRAM controller will then switch the internal multiplexor to place the column address on the DRAM address bus and assert $\overline{CAS}$. $\overline{DTACK}$ will wait the programmed number of wait states before asserting to indicate the end of the access.

Normal Access: If the controller is programmed in Normal Mode (B1 = 1), $\overline{RAS}$ will assert and negate after the programmed $\overline{RAS}$ low time. The user can perform burst access if desired.

Page Access: The DP8440/41 have an internal page comparator. This feature enables the user to do a series of accesses without negating $\overline{RAS}$ for as long as the row address remains unchanged. The user needs to provide a new address for every access. The page comparator can also be programmed as an input. This is beneficial for CPUs that have an internal page comparator. The user can do burst accesses while in page if desired.

Burst Access: These controllers can also generate new addresses to burst a specific number of locations. The user can choose to burst in a wrap around fashion for 2, 4, 8, 16 locations. Or, if the input NoWRAP is asserted, the controller will burst consecutive locations and the column address will not wrap around. The controller must be programmed in Latch Mode to generate the burst addresses.

Refresh Modes: The DP8440/41 can perform Automatic Internal Refreshes, or Externally Controlled Refreshes. During a long page access the controller can queue up to six refresh requests and burst refresh the addresses missed when the access finishes.

Refresh Types: The DP8440/41 can be programmed to do all $\overline{RAS}$ Refresh, Staggered Refresh, Error Scrubbing during Refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh.

Wait Support: These controllers provide wait logic for all three types of accesses. The user needs to program the desired number of wait states for opening, page and burst accesses.

$\overline{RAS}$ and $\overline{CAS}$ Configurations: The $\overline{RAS}$ outputs can be programmed to drive one, two or four banks of memory and the $\overline{CAS}$ drivers can be programmed for byte writing in buses up to 64 bits wide.

TRI-STATE Outputs and Multiporting: The $\overline{GRANT}$ input can be used for multi-porting. When high this input will TRI-STATE the outputs, allowing another controller to drive the DRAM.

Other Features: Independent $\overline{RAS}$ precharge counters allow memory interleaving, thus back to back access to different memory banks is not delayed due to precharge.

The output $\overline{NADTACK}$ can be used to pipeline one address, getting the next access to start one clock early.

The input NoWRAP will increment the address during a burst access in a linear fashion. This is convenient for graphics or long page access.

Terminology: This paragraph explains the terminology used in this data sheet. The terms negated and asserted are used. For example, $\overline{ECAS0}$ asserted means the $\overline{ECAS0}$ input is at logic 0. The term NoWRAP asserted means that NoWRAP is at logic 1.

3.0 Signal Descriptions

3.1 ADDRESS AND CONTROL SIGNALS

Pin Name	Device (if not Applicable to All)	Input/ Output	Description
R0–11 R0–12	DP8440 DP8441	I	**ROW ADDRESS:** These inputs are used to specify the row address during an access to the DRAM. They are also used to program the chip when $\overline{\text{ML}}$ is asserted.
C0–11 C0–12	DP8440 DP8441	I	**COLUMN ADDRESS:** These inputs are used to specify the column address during an access to the DRAM. They are also used to program the chip when $\overline{\text{ML}}$ is asserted.
B0–B1		I	**BANK SELECT:** Depending on programming, these inputs are used to select group $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ outputs to assert during an access. They are also used to program the chip when the $\overline{\text{ML}}$ is asserted.
$\overline{\text{ECAS}}$0–3 $\overline{\text{ECAS}}$0–7	DP8440 DP8441	I	**ENABLE CAS:** These inputs asserted enable a single or group of $\overline{\text{CAS}}$ outputs. In combination with the B0, B1 and the programming selection, these inputs select which $\overline{\text{CAS}}$ outputs will assert during an access. The $\overline{\text{ECAS}}$ signals can also be used to toggle a group of $\overline{\text{CAS}}$ outputs during page or burst mode accesses. They are also used to program the chip when $\overline{\text{ML}}$ is asserted.
NoWRAP (EXTNDRF)		I	**NO WRAP:** Asserting this signal causes the column address to be incremented sequentially by one. The column address will not wrap around if NoWRAP is asserted. When $\overline{\text{RFIP}}$ is asserted, this signal is an EXTNDRF, used to extend refresh by any number of CLK periods until EXTNDRF is negated.
$\overline{\text{NoLATCH}}$	DP8441	I	**COLUMN ADDRESS LATCH DISABLE:** This input will disable $\overline{\text{ADS}}$ from latching the column address when Latch Mode is selected.
$\overline{\text{ADS}}$		I	**ADDRESS STROBE:** This input starts every access. Depending on programming this input could latch the column address from the rising edge.
$\overline{\text{CS}}$		I	**CHIP SELECT:** This input signal must be asserted to enable $\overline{\text{ADS}}$ to start an access.
$\overline{\text{DTACK}}$		O	**DATA TRANSFER ACKNOWLEDGE:** This output can be programmed to insert wait states into a CPU access cycle. $\overline{\text{DTACK}}$ negated signifies a wait condition, when asserted signifies that the access has taken place. This signal can be delayed a number of positive or negative edges of clock. During burst accesses, $\overline{\text{DTACK}}$ transitions increment the column address.
$\overline{\text{NADTACK}}$		O	**NEXT ADDRESS or EARLY DTACK:** This output asserts one clock cycle before $\overline{\text{DTACK}}$. This output can be used to request the next address in a sort of pipelining fashion or it provides more time when $\overline{\text{DTACK}}$ needs to be generated externally.
$\overline{\text{WAITIN}}$	DP8441	I	**WAIT INPUT:** This input asserted delays $\overline{\text{DTACK}}$ for one extra clock period.
$\overline{\text{GRANT}}$		I	**MEMORY ACCESS GRANT:** The $\overline{\text{GRANT}}$ input functions as an output enable. If negated, it forces the outputs to a TRI-STATE condition.
PAGMISS		I/O	**PAGE MISS:** When programmed as an output, this signal asserts when either the row or the bank address changes from the previous access cycle or the column address has been incremented beyond the page boundary. If this pin is programmed as an input, it is the responsibility of the system to tell the controller if the next access is within the page. Useful for CPUs with internal page comparators, PAGMISS is valid only if $\overline{\text{ADS}}$ and $\overline{\text{CS}}$ are asserted.
$\overline{\text{BSTARQ}}$/ BSTARQ		I	**BURST ACCESS REQUEST:** This input enables the Burst Access Mode. This input can be programmed to be active high or active low.

3.0 Signal Descriptions (Continued)

3.2 DRAM CONTROL SIGNALS

Pin Name	Device (if not Applicable to All)	Input/ Output	Description
Q0–11 Q0–12	DP8440 DP8441	O	**DRAM ADDRESS:** These output signals are the multiplexed outputs of the R0–11/12 and C0–11/12 and form the DRAM address bus. These outputs contain the refresh address whenever $\overline{\text{RFIP}}$ is asserted. They have high capacitive drivers with 20Ωs series damping resistors.
$\overline{\text{RAS}}$0–3		O	**ROW ADDRESS STROBES:** These outputs are asserted to latch the row address contained on the outputs Q0–11/12 into the DRAM. When $\overline{\text{RFIP}}$ is asserted, the $\overline{\text{RAS}}$ outputs are used to latch the refresh row address contained on the Q0–11/12 outputs into the DRAM. These outputs have high capacitive drivers with 20Ω series damping resistors.
$\overline{\text{CAS}}$0–3 $\overline{\text{CAS}}$0–7	DP8440 DP8441	O	**COLUMN ADDRESS STROBES:** These outputs are asserted to latch the column address contained on the outputs Q0–11/12 into the DRAM. When $\overline{\text{RFIP}}$ is asserted and $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh is selected, the $\overline{\text{CAS}}$ outputs will assert 1T (one clock period) before the $\overline{\text{RAS}}$ outputs are asserted. These outputs have high capacitive drivers with 20Ω series damping resistors.
$\overline{\text{WE}}$		O	**WRITE ENABLE:** This output asserted specifies a write operation to the DRAM. When negated, this output specifies a read operation to the DRAM. This output has a high capacitive driver and a 20Ω series damping resistor.
$\overline{\text{WIN}}$		I	**WRITE ENABLE IN:** This input is used to signify a write operation to the DRAM. The $\overline{\text{WE}}$ output will follow this input. Also, this input controls the precharge time for Read and Write during Burst Mode Access.

3.3 REFRESH SIGNALS

Pin Name	Device (if not Applicable to All)	Input/ Output	Description
RFRQ		O	**REFRESH REQUEST:** When RFRQ is asserted, it specifies that 15 μs or 120 μs have passed. If $\overline{\text{DISRFSH}}$ is negated and the controller is not into an access cycle, the DP8440/41 will perform an internal refresh. If $\overline{\text{DISRFSH}}$ is asserted, RFRQ can be used to externally request a refresh by asserting the input $\overline{\text{RFSH}}$.
$\overline{\text{RFIP}}$		O	**REFRESH IN PROGRESS:** This output is asserted prior to a refresh cycle and is negated when all the $\overline{\text{RAS}}$ outputs are negated for that refresh.
$\overline{\text{RFSH}}$		I	**REFRESH:** This input asserted with $\overline{\text{DISRFSH}}$ already asserted will request a refresh. If this input is continually asserted, the DP8440/41 will perform refresh cycles in a burst refresh fashion until the input is negated. If $\overline{\text{RFSH}}$ is asserted with $\overline{\text{DISRFSH}}$ negated, the internal refresh address counter is cleared. This technique is useful for burst refreshes.
$\overline{\text{DISRFSH}}$		I	**DISABLE REFRESH:** This input is used to disable internal refreshes and must be asserted when using $\overline{\text{RFSH}}$ for externally requested refreshes.

3.4 RESET AND PROGRAMMING SIGNALS

Pin Name	Device (if not Applicable to All)	Input/ Output	Description
$\overline{\text{ML}}$		I	**MODE LOAD:** This input signal, when low, enables the internal programming register that stores the programming information.
$\overline{\text{RESET}}$		I	**SYSTEM RESET:** Reset forces the DP8440/41 to be set at a known state. V_{CC}, CLK and DELCLK have to reach their proper DC and AC specifications for at least 1 ms before negating the $\overline{\text{RESET}}$ signal. All outputs are negated when $\overline{\text{RESET}}$ is asserted.

3.0 Signal Descriptions (Continued)

3.5 CLOCK INPUTS

Pin Name	Device (if not Applicable to All)	Input/ Output	Description
CLK		I	**SYSTEM CLOCK:** This input may be in the range of 500 kHz to 40 MHz. This input is generally a constant frequency but it may be controlled externally to change frequencies for some arbitrary reason. This input provides the clock to the internal state machine that arbitrates between accesses and refreshes. This clock's positive edges and negative edges are used to extend the $\overline{\text{DTACK}}$ signal. This clock is also used as a reference for the $\overline{\text{RAS}}$ precharge time, the $\overline{\text{RAS}}$ low during refresh time and $\overline{\text{CAS}}$ precharge time.
DELCLK		I	**DELAY LINE CLOCK:** The clock input DELCLK, may be in the range of 10 MHz to 40 MHz and should be a multiple of 2 to have the DP8440/41 switching characteristics hold. If DELCLK is not one of the above frequencies, the accuracy of the internal delay line will suffer. This happens because the phase lock loop that generates the delay line assumes an input clock frequency multiple of 2 MHz. For example, if DELCLK input is 17 MHz and we choose to divide by 8 (program bits C0–3), this will produce 2.125 MHz which is 6.25% off of 2 MHz. Therefore, the DP8440/41 delay line will produce delays that are shorter (faster delays) than intended. If divide by 9 was chosen, the delay line would produce longer delays (slower delays) than intended (1.89 MHz instead of 2 MHz). This clock is also divided to create the internal refresh clock.

3.6 POWER SIGNALS AND CAPACITOR INPUT

Pin Name	Device (if not Applicable to All)	Input/ Output	Description
V_{CC}		I	**POWER:** Supply Voltage.
GND		I	**GROUND:** Supply Voltage Reference.
CAP		I	**CAPACITOR:** This input is used by the internal PLL for stabilization. The value of the ceramic capacitor should be 0.1 μF and it should be connected between this input and ground.

4.0 Programming and Resetting

4.1 RESET

After power up, the DP8440/41 must be reset and programmed before it can be used to access the DRAM. Reset is accomplished by asserting the input $\overline{\text{RESET}}$ for at least 16 positive edges of CLK after V_{CC} stabilizes. After reset, the part can be programmed.

4.2 PROGRAMMING

Programming is accomplished by presenting a valid programming selection on the row, column, bank selects and $\overline{\text{ECAS}}$ inputs and toggling the $\overline{\text{ML}}$ input from low to high.

When $\overline{\text{ML}}$ goes high the part is programmed. After the first programming after a reset the part will enter a 60 ms initialization period. During this period the controller will refresh the memory, so further DRAM warm up cycles are not necessary. The user can program the part on the fly by pulsing $\overline{\text{ML}}$ low and high (provided that no refresh is in progress) while a valid programming selection is on the address bus. The part will not enter the initialization period when it is only re-programmed.

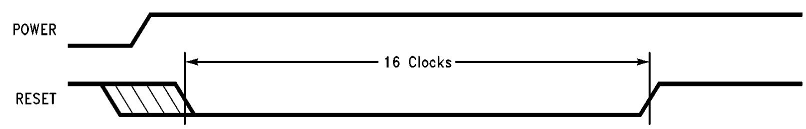


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FIGURE 5. Reset

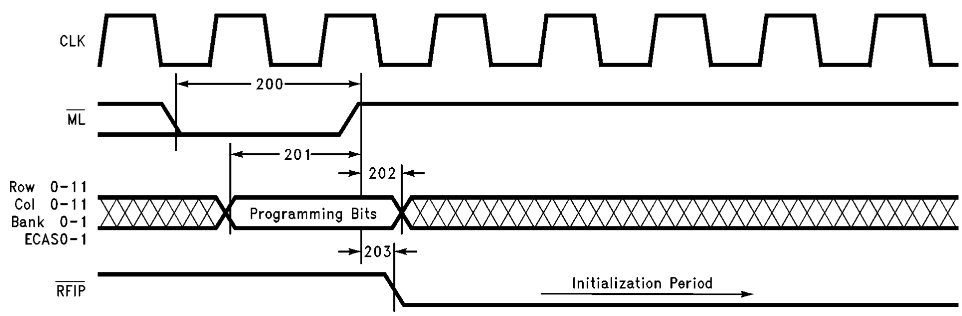

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FIGURE 6. Programming

Programming the DP8440/41

4.3 PROGRAMMING SELECTION

$\overline{RAS}$ LOW AND PRECHARGE TIME

R1	R0	
0	0	2T
0	1	3T
1	0	4T
1	1	5T

$\overline{DTACK}$ DURING OPENING ACCESS WILL ASSERT AFTER $\overline{RAS}$

R3	R2	
0	0	1T
0	1	2T
1	0	3T
1	1	4T

$\overline{DTACK}$ DURING BURST ACCESS WILL ASSERT AFTER $\overline{CAS}$

R5	R4	
0	0	0T
0	1	1T
1	0	2T
1	1	3T

$\overline{DTACK}$ DURING PAGE ACCESS WILL ASSERT AFTER $\overline{CAS}$

R7	R6	
0	0	0T
0	1	1T
1	0	2T
1	1	3T

PAGE SIZE SELECT

R9	R8	
0	0	512
0	1	1024
1	0	2048
1	1	4096

WRAP AROUND SIZE

R11	R10	
0	0	2
0	1	4
1	0	8
1	1	16

Programming the DP8440/41 (Continued)

4.3 PROGRAMMING SELECTION (Continued)

DIVISOR SELECT

C3	C2	C1	C0	
0	0	0	0	20
0	0	0	1	19
0	0	1	0	18
0	0	1	1	17
0	1	0	0	16
0	1	0	1	15
0	1	1	0	14
0	1	1	1	13
1	0	0	0	12
1	0	0	1	11
1	0	1	0	10
1	0	1	1	9
1	1	0	0	8
1	1	0	1	7
1	1	1	0	6
1	1	1	1	5

$\overline{RAS}$ AND $\overline{CAS}$ CONFIGURATIONS AND REFRESH BEHAVIOR

C5	C4	
0	0	All $\overline{RAS}$ and all $\overline{CAS}$ are selected. B0 and B1 are not used. All $\overline{RAS}$ refresh.

C5 = 0, C4 = 1

If C6 = 0 Non Error Scrubbing Selected. All CAS Selected. 2-Step Staggered Refresh.	B1	B0 is not Used
	0	RAS0−1
	1	RAS2−3

If C6 = 1 Error Scrubbing Selected. All RAS Refresh. CAS Pairs Selected.	B1	B0 is Not Used
	0	RAS0−1 and CAS0−1, CAS4−5
	1	RAS2−3 and CAS2−3, CAS6−7

C5 = 1, C4 = 0

If C6 = 0 Non Error Scrubbing Selected. All CASs Selected. 4-Step Staggered Refresh.	B1	B0	
	0	0	RAS0
	0	1	RAS1
	1	0	RAS2
	1	1	RAS3

If C6 = 1 Error Scrubbing Selected. All RAS Refresh. CAS Pairs Selected.	B1	B0	
	0	0	RAS0, CAS0−4
	0	1	RAS1, CAS1−5
	1	0	RAS2, CAS2−6
	1	1	RAS3, CAS3−7

C5 = 1, C4 = 1

If C6 = 0 Non Error Scrubbing. 2-Step Staggered Refresh. CAS Pairs Selected.	B1	B0 is not used.
	0	RAS0−1 and CAS0,1,4,5
	1	RAS2−3 and CAS2,3,6,7

If C6 = 1 Error Scrubbing Selected. All RAS Refresh. CAS Pairs Selected.	B1	B0 is not used.
	0	RAS0−1 and CAS0,1,4,5
	1	RAS2−3 and CAS2,3,6,7

ERROR SCRUBBING MODE SELECT

C6	
0	Staggered Refresh (Non Error Scrubbing)
1	Error Scrubbing (No $\overline{CAS}$-before-$\overline{RAS}$ and No Staggered Refresh)

Programming the DP8440/41 (Continued)

4.3 PROGRAMMING SELECTION (Continued)

ROW ADDRESS HOLD TIME SELECT t_{RAH}

C7	
0	10 ns
1	15 ns

PAGMISS INPUT OR OUTPUT SELECT

C8	
0	Input
1	Output

$\overline{CAS}$ PRECHARGE DURING BURST

C9	Read Cycle	Write Cycle
0	½T	1T
1	1T	2T

REFRESH MODE SELECT

C10	
0	$\overline{RAS}$ Only Refresh
1	$\overline{CAS}$-before-$\overline{RAS}$ Refresh

FINE TUNE REFRESH CYCLE

C11	
0	15 µs
1	120 µs

COLUMN ADDRESS COUNTER CONTROL SELECT

B0	
0	$\overline{DTACK}$ Falling Edge
1	$\overline{DTACK}$ Rising Edge

PAGE OR NORMAL MODE SELECT

B1	
0	Page Mode
1	Normal Mode

ADDRESS LATCH MODE

ECAS 0	
0	Latch Mode
1	Fall Through Mode

BURST REQUEST SELECT (BSTARQ INPUT)

ECAS1	
0	Active Low
1	Active High

$\overline{CAS}$ AND $\overline{DTACK}$ CLOCK EDGE SELECT

ECAS2	
0	Rising Edge
1	Falling Edge

RESERVED

ECAS3	
0	
1	

5.0 Accessing Modes

The DP8440/41 are synchronous machines. They allow the user to access the DRAM in three different ways, Page, Burst and Normal mode. Every one of these accesses starts in the same way, this datasheet calls it an Opening Access.

5.1 OPENING ACCESS

Every access starts with $\overline{ADS}$ and $\overline{CS}$ asserting. $\overline{ADS}$, $\overline{CS}$ and the address inputs must meet setup timings with respect to the next rising edge of CLK. The DP8440/41 places the row address on the Q outputs and $\overline{RAS}$ asserts from the rising edge of CLK that $\overline{ADS}$ is set up to. The DP8440/41 guarantees the programmed Row Address Hold Time, t_{RAH}, before switching the internal multiplexer to place the column address on the Q outputs. After the column address is valid on the Q outputs, the controller asserts $\overline{CAS}$. The DRAM controller always guarantees t_{ASC} of 0 ns. $\overline{DTACK}$ asserts after $\overline{RAS}$ according to the programming selection (R2–3). If the user programs Latch Mode, through programming bit $\overline{ECAS0}$, the DRAM controller latches the column address on the rising edge of $\overline{ADS}$ (Normal or Page Mode). If not, the controller keeps the latches in a fall through mode.

5.2 NORMAL MODE

When the controller is programmed in Normal Mode (B1 = 1), $\overline{RAS}$ asserts only for the programmed number of clocks selected by R0–1, $\overline{RAS}$ Low Time, and automatically negates from a rising clock edge. To finish the access, $\overline{CAS}$ negates from the same clock edge at which $\overline{DTACK}$ negates. After $\overline{RAS}$ negates, the DP8440/41 will guarantee the programmed number of positive edges of clock for $\overline{RAS}$ precharge. $\overline{RAS}$ will not assert for another access until precharge is met. *Figure 7* shows an opening access (Normal Mode) followed by a delayed access due to precharge (accessing the same bank). The second access is delayed by one clock period to meet precharge time requirements.

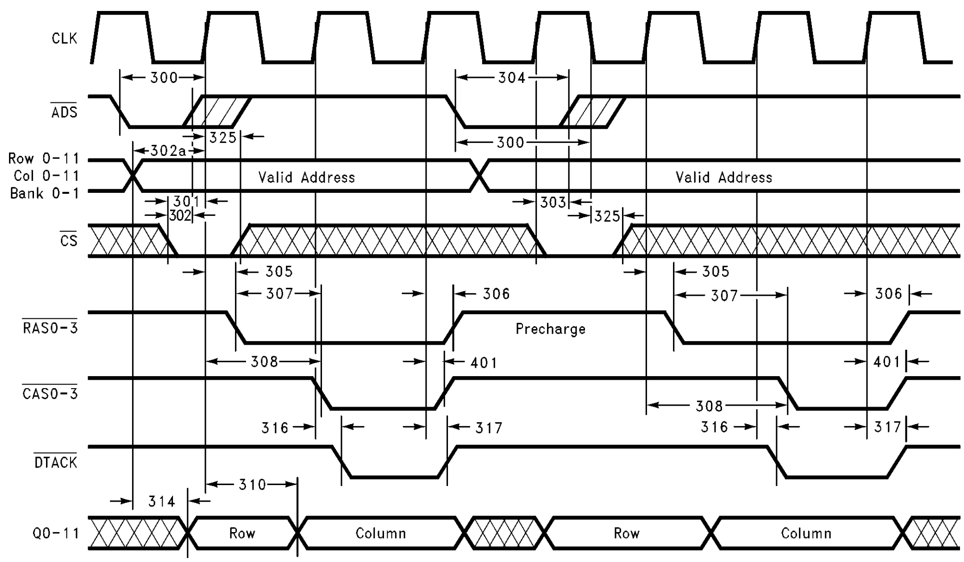

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FIGURE 7. A Normal Opening Access and Delayed Access ($\overline{RAS}$ Low Time is Programmed for 2 Clocks)

5.0 Accessing Modes (Continued)

5.3 PAGE MODE ACCESS

When the DP8440/41 is programmed for Page Accesses, every access after the opening access needs a new address and a new $\overline{\text{ADS}}$. During Page Mode the DRAM controller keeps $\overline{\text{RAS}}$ asserted until there is a page miss detected. When a new access is requested, **$\overline{\text{CAS}}$ asserts from the rising CLK edge that $\overline{\text{ADS}}$ is set up to for reads, and is delayed 1 clock for writes.** $\overline{\text{DTACK}}$ asserts according to the programming selection in bits R6–7. At the end of a page access only $\overline{\text{CAS}}$ and $\overline{\text{DTACK}}$ negate and they negate on the same clock edge.

During page accesses only $\overline{\text{CAS}}$ and $\overline{\text{DTACK}}$ toggle until there is a page miss. When a page miss is detected, the DP8440/41 will negate $\overline{\text{RAS}}$ and meet the programmed precharge time. CPUs with page comparators can program the DRAM controller's page comparator as an input. When this input asserts, it indicates that a page change has occurred, $\overline{\text{RAS}}$ will negate and the controller will meet the precharge time. *Figure 8* shows an opening access followed by two page accesses. The first page access is a "page hit," the second access is out of page.

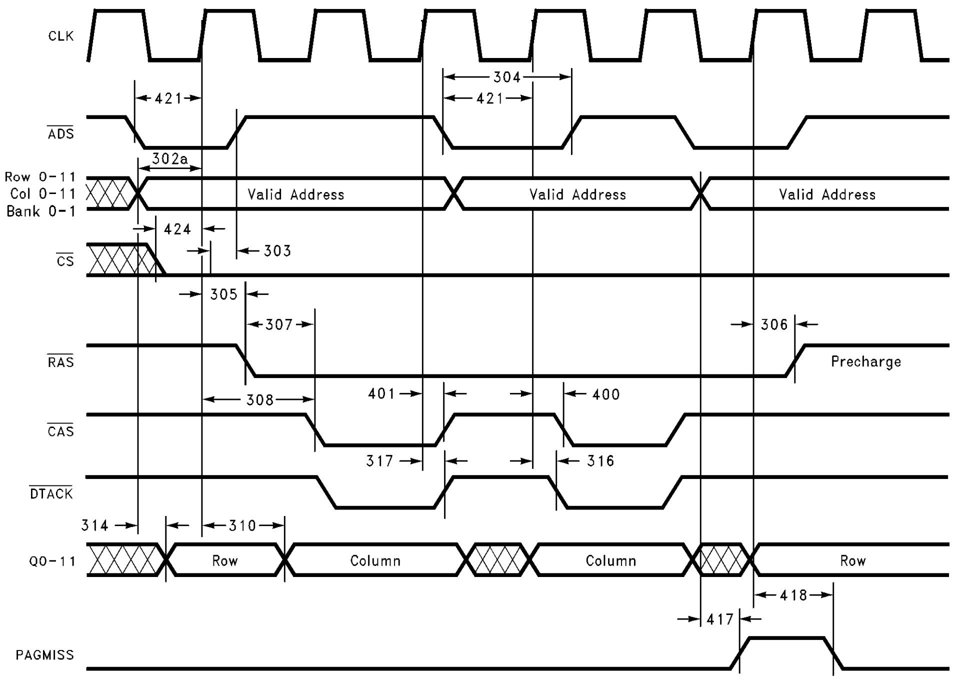

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FIGURE 8. Opening Access Followed by Page Accesses

5.0 Accessing Modes (Continued)

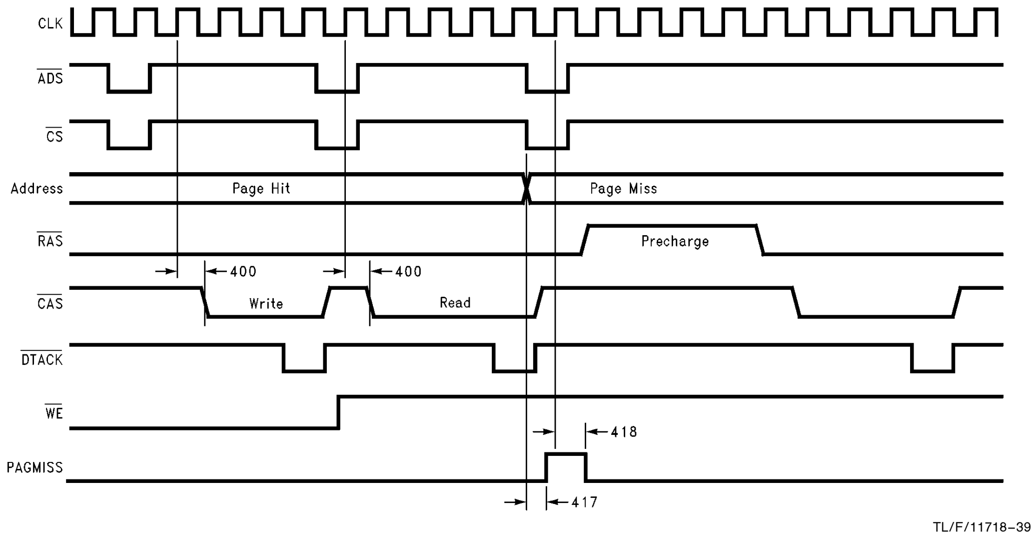

FIGURE 9. Page "Hit" Write and Read Followed by Page Miss (CAS Assertion for Write is Delayed One Clock)

5.4 BURST ACCESS

The DP8440/41 can also perform burst accesses to several locations in different wrap around sizes. The user requests burst accesses by asserting the input BSTARQ. BSTARQ must be negated before the last $\overline{\text{DTACK}}$. This input can be programmed to be active high or active low. The number of burst locations can be programmable to be modulo 2, 4, 8, or 16. If the beginning of the sequence does not start with 0, 00, 000 or 0000, the controller will wrap around. The user may choose not to wrap by asserting the input NoWRAP, in this case the controller will increment the column address linearly. A NoWRAP burst access cannot cross a page boundary unless the port is programmed in Page Mode, in which case a Page Miss occurs and the burst access terminates. Burst accesses can be requested at any time. The user can do burst accesses while in Page Mode (see Inner Page Burst), or in Normal Mode. The column address is incremented by $\overline{\text{DTACK}}$ transitions as programmed by B0. Thus, if $\overline{\text{DTACK}}$ is programmed as 0 T, the column address will not be incremented and the CPU must provide the addresses to burst. $\overline{\text{CAS}}$ and $\overline{\text{DTACK}}$ can be programmed to toggle from either clock edge. The $\overline{\text{CAS}}$ precharge time is programmable to 1 or ½ clocks during read accesses and 1 or 2 clocks during write accesses (½T = 10 ns minimum of $\overline{\text{CAS}}$ precharge).

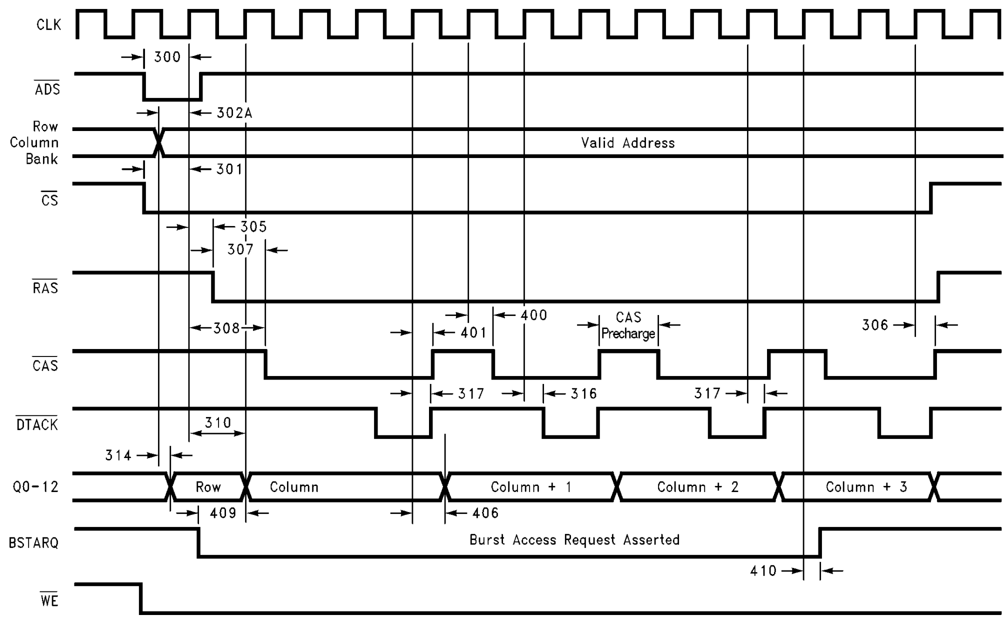

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FIGURE 10. Burst Write Access

Programming Selection	Bits	Mode
$\overline{\text{DTACK}}$ during Opening	R3 = 1, R2 = 0	3T
$\overline{\text{DTACK}}$ during Burst	R5 = 1, R4 = 0	2T
$\overline{\text{CAS}}$ Precharge during Burst	C9 = 0	Read: ½T, Write: 1T
Column Address Counter Control	BO = 1	$\overline{\text{DTACK}}$ Rising Edge
$\overline{\text{CAS}}$ and $\overline{\text{DTACK}}$ Edge Select	ECAS2 = 0	Rising Edge

FIGURE 11. Burst Write Access

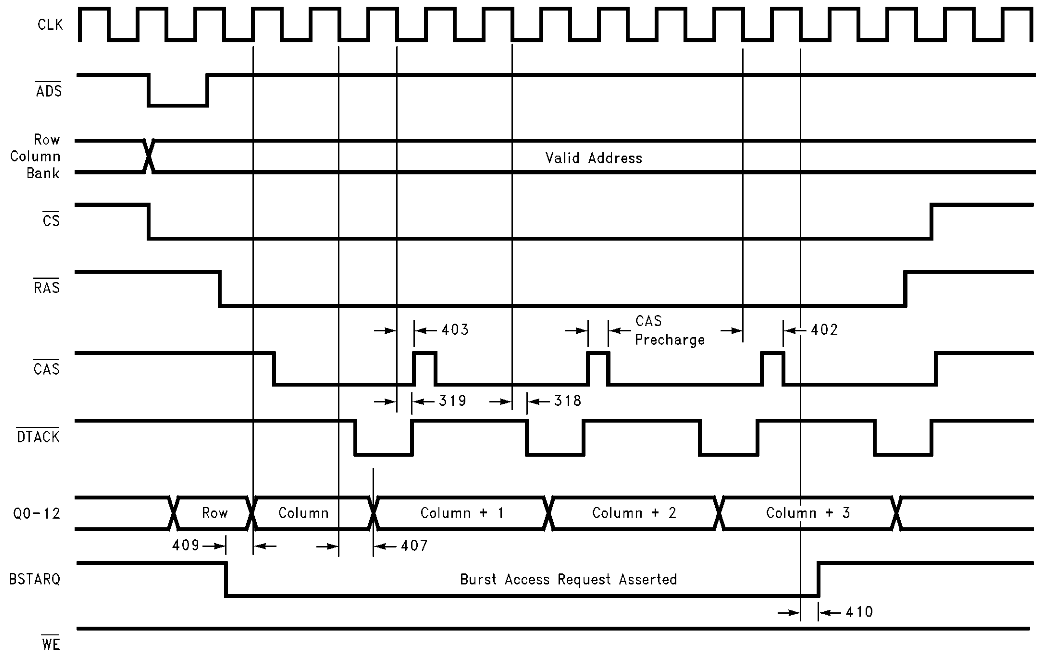

FIGURE 12. Burst Read Access

Programming Selection	Bits	Mode
$\overline{\text{DTACK}}$ during Opening	R3 = 1, R2 = 0	3T
$\overline{\text{DTACK}}$ during Burst	R5 = 1, R4 = 0	2T
$\overline{\text{CAS}}$ Precharge during Burst	C9 = 0	Read: ½T, Write: 1T
Column Address Counter Control	BO = 0	$\overline{\text{DTACK}}$ Falling Edge
$\overline{\text{CAS}}$ and $\overline{\text{DTACK}}$ Edge Select	ECAS2 = 0	Falling Edge

5.0 Accessing Modes (Continued)

5.5 INNER PAGE BURST ACCESS

If the user plans to burst within page access, the DP8440/41 must be programmed in Latch Mode. In this case, the DRAM latches the column address on the rising edge of $\overline{ADS}$. When the controller detects BSTARQ asserted, $\overline{DTACK}$ transitions will increment the column address in modulo 2, 4, 8, or 16 with wrap around at the boundaries for as long as BSTARQ is asserted. If the user asserts the input NoWRAP, the controller increments the address sequentially. After an InnerPage Burst, $\overline{RAS}$ will stay asserted until there is a page miss detected. *Figure 13* shows an opening access followed by a page access, two burst accesses and a new access in a different page (page miss).

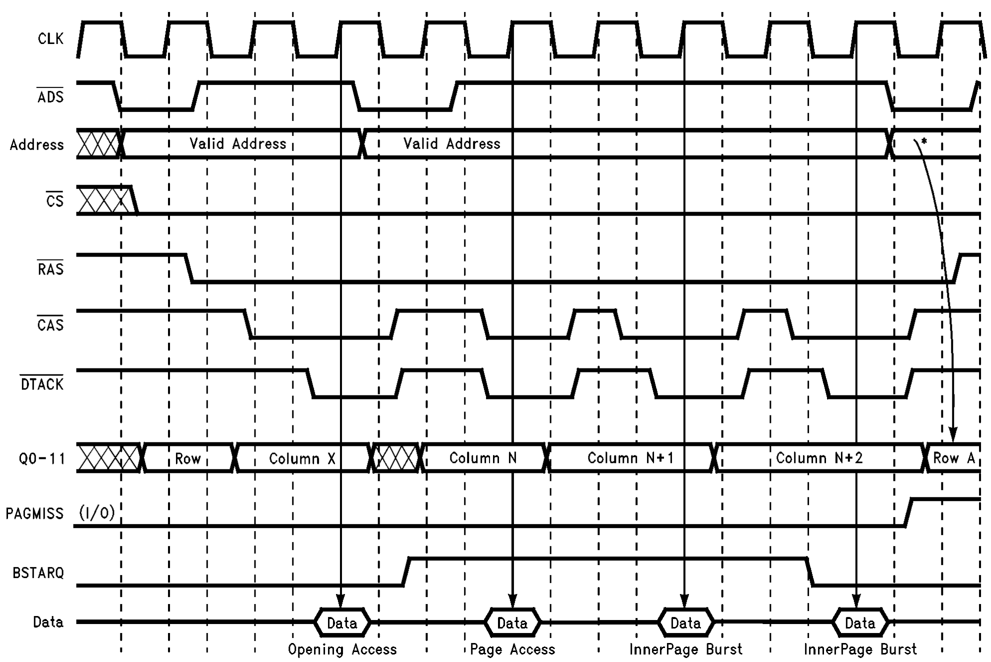

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FIGURE 13. Opening Access followed by a Page "HIT" Access with 2 Bursts

6.0 Refresh Modes

The DP8440/41 support auto-internal refresh, and externally control refresh. The DP8440/41 arbitrates between refreshes and accesses and guarantees precharge timings after every access and refresh. The DRAM controller will never interrupt an access in progress to do a refresh, nor will it interrupt a refresh in progress when an access is requested. After every refresh the DRAM controller will guarantee the programmed precharge time before $\overline{RAS}$ can assert for a new access or for a second refresh. The refresh period can be programmed for 15 µs or for 120 µs.

6.1 AUTO-INTERNAL REFRESH

This refresh scheme is completely transparent to the CPU. The DP8440/41 will refresh the DRAM every 15 µs or 120 µs, depending on the programming selection. When the refresh counter expires (every 15 µs or 120 µs) the RFRQ output asserts. On the next rising edge of clock $\overline{RFIP}$ asserts and, one clock period later, $\overline{RAS}$s assert. $\overline{RFIP}$ negates on the same clock edge that $\overline{RAS}$s negate. If the user is doing long page or burst accesses, the DP8440/41 will keep track of up to 6 missed refreshes. At the end of the access the DRAM controller will burst refresh the locations missed during the access.

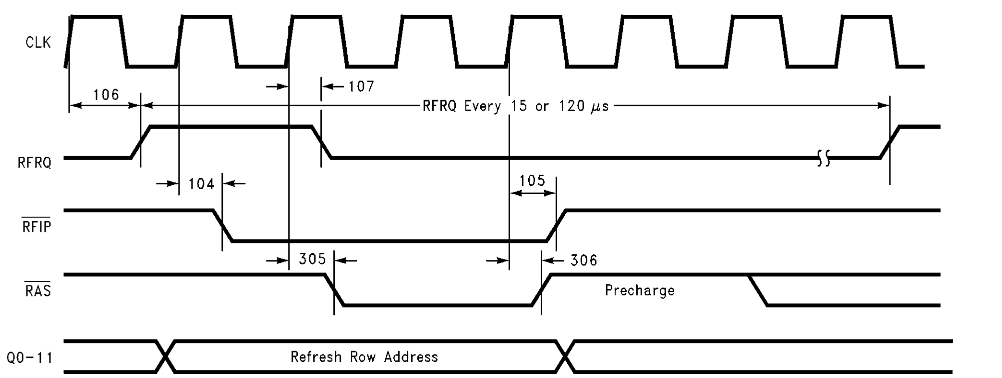

FIGURE 14. Autointernal Refresh (2T of $\overline{RAS}$ Low and Precharge)

6.2 EXTERNALLY CONTROLLED REFRESH

The user can perform externally controlled refreshes by asserting the $\overline{DISRFSH}$ and $\overline{RFSH}$ input signals. When these inputs assert, the DP8440/41 will perform a refresh as soon as possible. If the user keeps $\overline{RFSH}$ asserted with $\overline{DISRFSH}$ already asserted, the DRAM controller will burst refresh the memory for as long as the inputs are valid. The controller will guarantee the $\overline{RAS}$ low and $\overline{RAS}$ precharge times for every refresh. The user can choose to monitor the output RFRQ to externally request a refresh. When RFRQ asserts, it indicates that the refresh counter has expired.

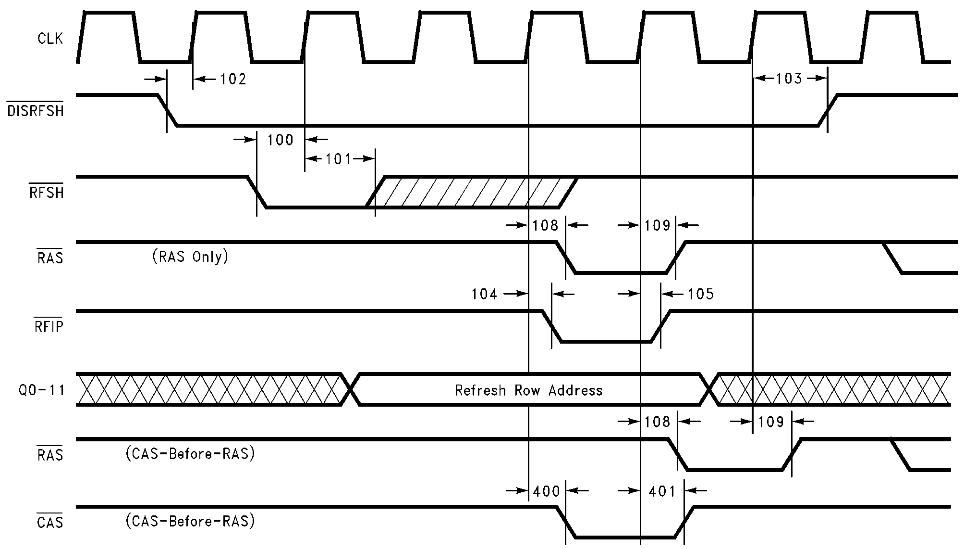

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FIGURE 15. Externally Controlled Refresh (2T of $\overline{RAS}$ Low and Precharge)

6.0 Refresh Modes (Continued)

6.3 ERROR SCRUBBING DURING REFRESH

The DP8440/41 supports error scrubbing during all $\overline{RAS}$ DRAM refreshes. Error scrubbing during refresh is selected through bits C4–C6 with bit C6 set during programming. Error scrubbing can not be used with staggered refresh. Error scrubbing during refresh allows a $\overline{CAS}$ or group of $\overline{CAS}$s to assert during the all $\overline{RAS}$ refresh as shown in *Figure 16*. This allows data to be read from the DRAM array and passed through an Error Detection And Correction Chip, EDAC. If the EDAC determines that the data contains a single bit error and corrects that error, the refresh cycle can be extended with the input extend refresh, EXTNDRF, and a read-modify-write operation can be performed by asserting $\overline{WE}$. It is the responsibility of the designer to ensure that $\overline{WE}$ is negated. The DP8440 has a 26-bit internal refresh address counter that contains the 12 row, 12 column and 2 bank addresses. The DP8441 has a 28-bit internal refresh address counter that contains the 13 row, 13 column and 2 bank addresses. These counters are configured as bank, column, row with the row address as the least significant bits. The bank counter bits are then used with the programming selection to determine which $\overline{CAS}$ or group of $\overline{CAS}$s will assert during a refresh.

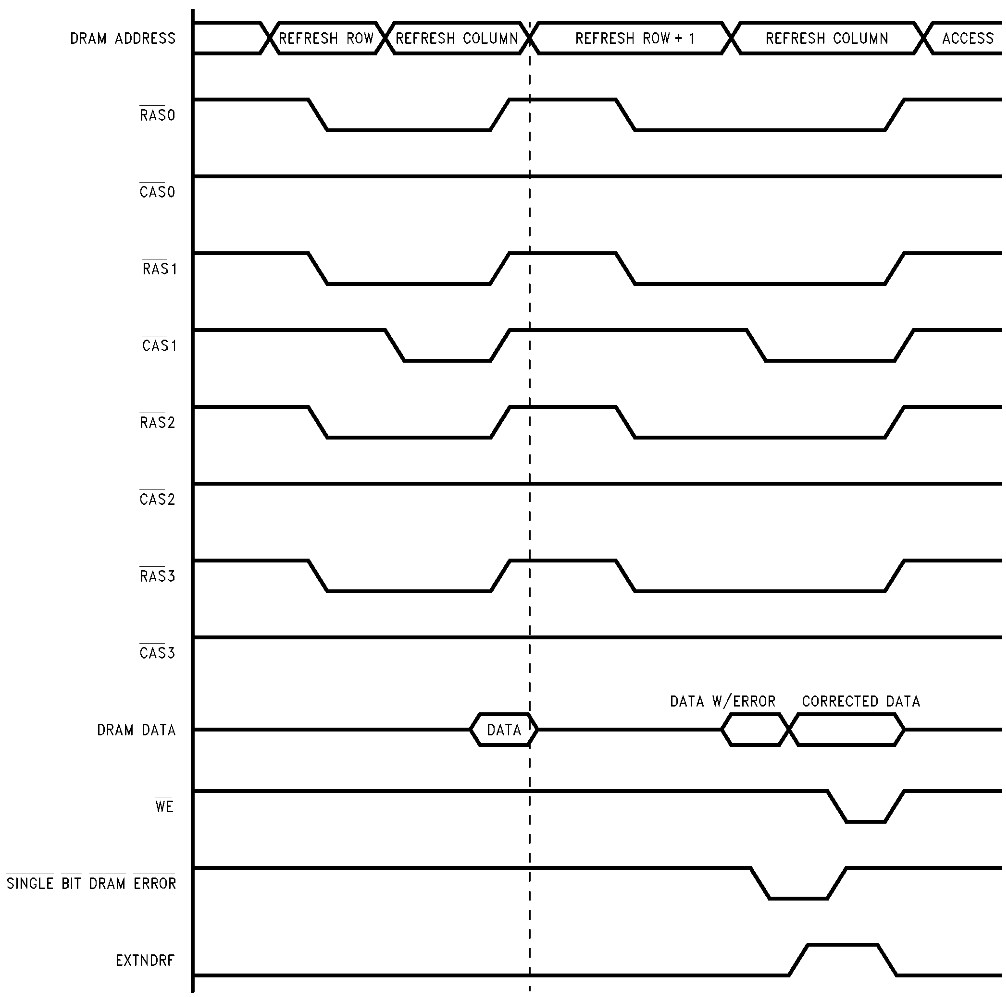

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FIGURE 16. Error Scrubbing during Refresh (Two Refresh Cycles Shown)

6.0 Refresh Modes (Continued)

6.4 EXTENDING REFRESH

The programmed number of periods of CLK that refresh $\overline{\text{RAS}}$s are asserted can be extended by one or multiple periods of CLK. Only the all $\overline{\text{RAS}}$ (with or without error scrubbing) type of refresh can be extended. To extend a refresh cycle, the input extend refresh, EXTNDRF, must be asserted before the positive edge of CLK that would have negated all the $\overline{\text{RAS}}$ outputs during the re fresh cycle and after the positive edge of CLK which starts all $\overline{\text{RAS}}$ outputs during the refresh as shown in *Figure 17*. This will extend the refresh to the next positive edge of CLK and EXTNDRF will be sampled again. The refresh cycle will continue until EXTNDRF is sampled low on a positive edge of CLK.

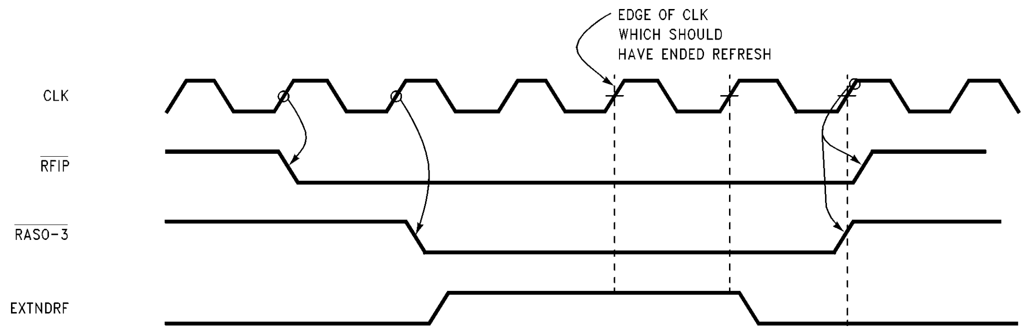

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FIGURE 17. Extending Refresh with the Extend Refresh (EXTNDRF) Input

6.5 REFRESH TYPES

The DP8440/41 support $\overline{RAS}$ Only refresh and $\overline{CAS}$-before-$\overline{RAS}$ refresh. $\overline{RAS}$ only refresh can be programmed to be staggered or non-staggered. Staggered refresh reduces peak current requirements and system noise.

The DP8440/41 have a large enough refresh address counter for error scrubbing during refresh. If error scrubbing is desired, the user must select the All $\overline{RAS}$ refresh option.

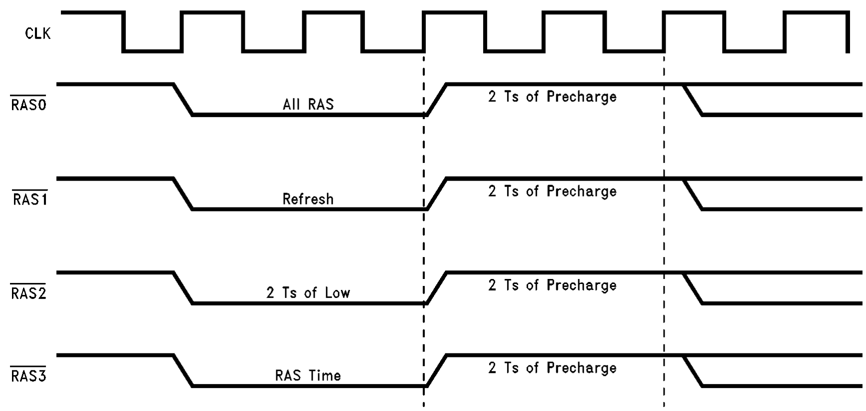

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FIGURE 18. All $\overline{RAS}$ Refresh with 2Ts of $\overline{RAS}$ Low and Precharge. All $\overline{RAS}$ refresh must be programmed when doing Error Scrubbing.

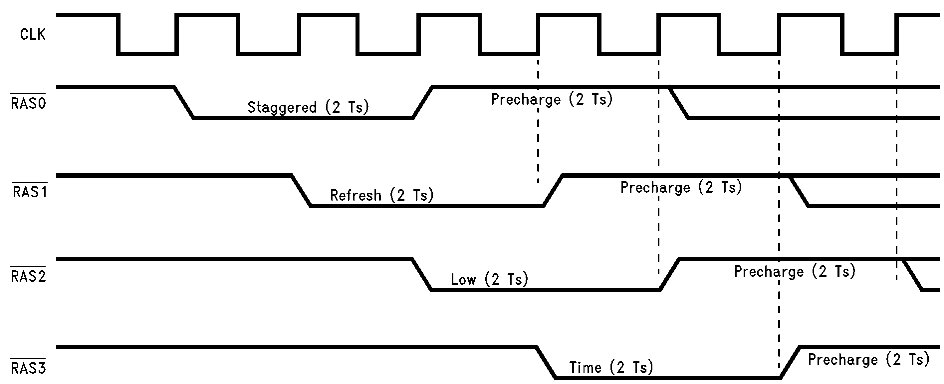

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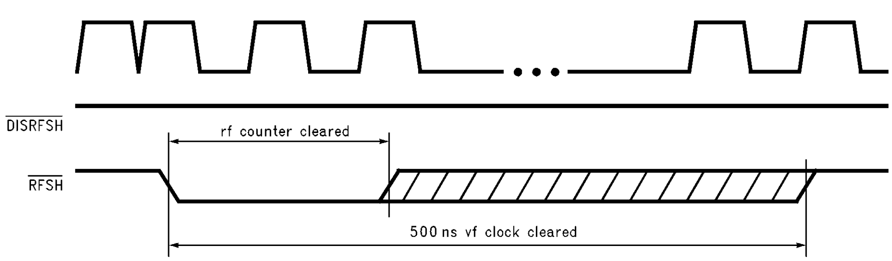
FIGURE 19. Staggered Refresh with 2Ts $\overline{RAS}$ low and Precharge. Staggered refresh is good for noise sensitive systems.

Clearing the Refresh Counter and Refresh Clock: The user can clear the refresh counter by pulsing $\overline{RFSH}$ low for two clocks while $\overline{DISRFSH}$ is negated. If $\overline{RFSH}$ is kept asserted for 500 ns, the refresh clock will also be cleared.



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7.0 Wait Support

The DP8440/41 provide full wait support for all types of accesses. Through the $\overline{DTACK}$ output, the user can insert wait states to provide the necessary time for completing a memory access. The user needs to program how $\overline{DTACK}$ will assert during Opening, Page or Burst accesses. The user can program $\overline{DTACK}$ to assert from the rising edge of clock or from the falling edge of clock.

7.1 OPENING ACCESS

Figures 20 and *21* show $\overline{DTACK}$ during opening accesses. $\overline{DTACK}$ asserts for only one clock cycle. $\overline{CAS}$ negates from the same clock edge $\overline{DTACK}$ negates. When programmed in Normal Mode, $\overline{RAS}$ will negate after the programmed $\overline{RAS}$ low time. When programmed in Page Mode, $\overline{RAS}$ will stay asserted until there is a page miss.

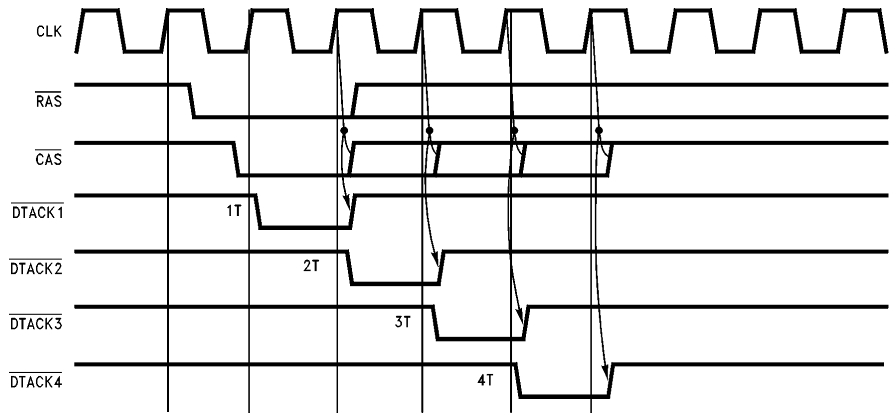

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FIGURE 20. $\overline{DTACK}$ Programmed to Assert from a Positive Edge of Clock

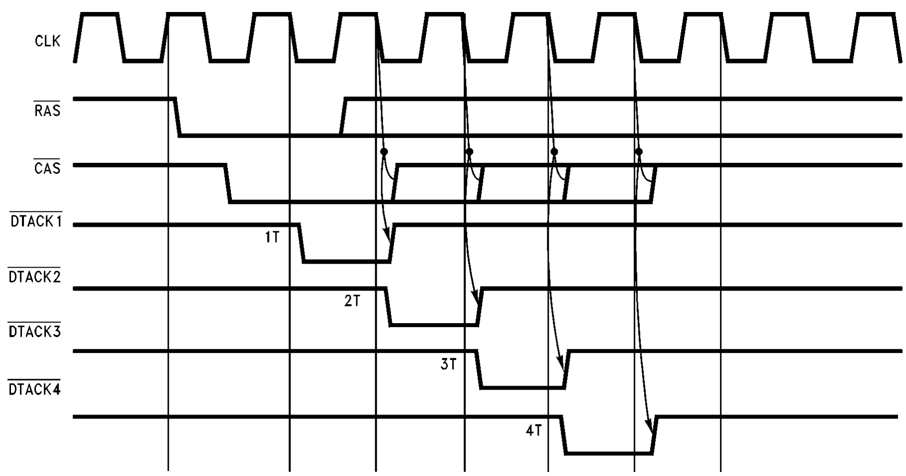

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FIGURE 21. $\overline{DTACK}$ Programmed to Assert from a Negative Edge of Clock

7.0 Wait Support (Continued)

7.2 PAGE ACCESSES

During page accesses, $\overline{\text{DTACK}}$ (and $\overline{\text{CAS}}$) will assert from either clock edge according to programming bit $\overline{\text{ECAS2}}$.

Figure 22 shows different $\overline{\text{DTACK}}$ assertions during page accesses, they follow an opening access with 1 wait state. $\overline{\text{DTACK}}$ and $\overline{\text{CAS}}$ assert on the rising edge of clock.

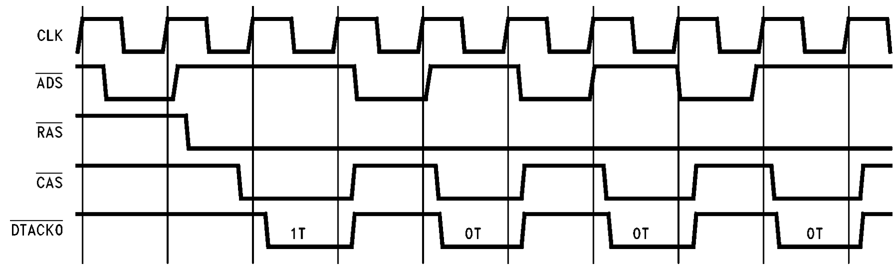

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FIGURE 22a. $\overline{\text{DTACK}}$ is Programmed 1T for Openings and 0T during Page

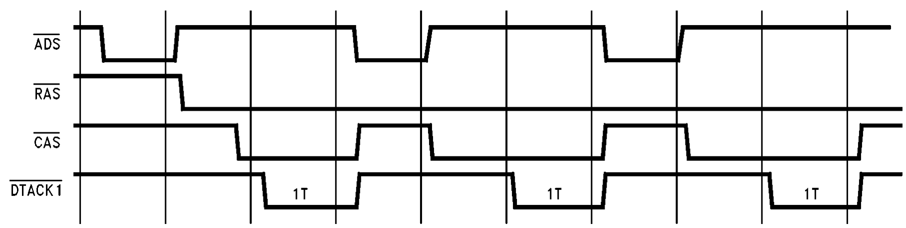

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FIGURE 22b. $\overline{\text{DTACK}}$ is Programmed 1T for Openings and 1T during Page

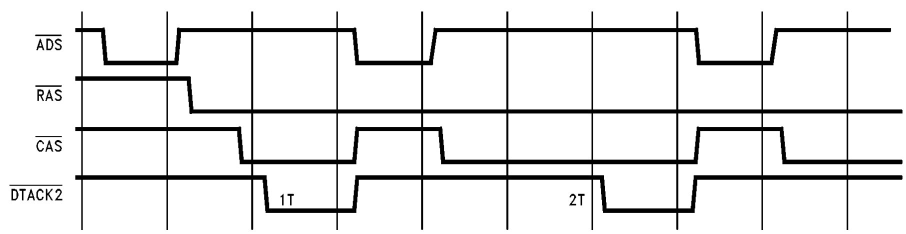

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FIGURE 22c. $\overline{\text{DTACK}}$ is Programmed 1T for Openings and 2T during Page

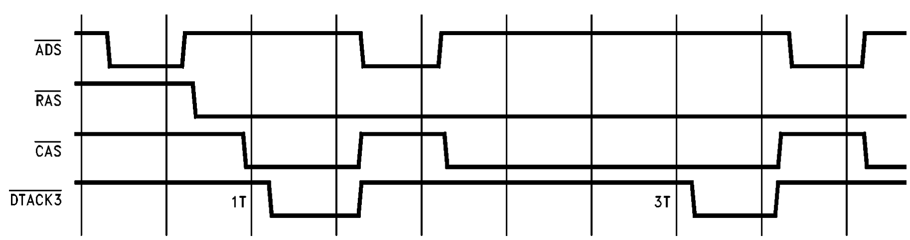

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FIGURE 22d. $\overline{\text{DTACK}}$ is Programmed 1T for Openings and 3T during Page

Note: $\overline{\text{DTACK}}$ is programmed to assert from a positive clock edge.

7.0 Wait Support (Continued)

7.3 BURST ACCESSES

During burst accesses, $\overline{\text{DTACK}}$ will assert from the clock edge chosen through programming bit $\overline{\text{ECAS2}}$. $\overline{\text{CAS}}$ automatically negates and the controller guarantees the minimum $\overline{\text{CAS}}$ precharge time according to programming bit C9. $\overline{\text{CAS}}$ and $\overline{\text{DTACK}}$ can be programmed to assert from either clock edge.

During burst accesses, the input BSTARQ must be asserted for $\overline{\text{CAS}}$ to toggle. *Figure 23* shows how $\overline{\text{DTACK}}$ asserts during burst accesses, following an opening access with one wait state. In *Figure 23a*, when the number of wait states in a burst is programmed to zero, $\overline{\text{DTACK}}$ remains asserted throughout the burst. The address is not incremented by the DRAM controller. It is the responsibility of the user to provide incrementing addresses.

For the controller to increment the column address $\overline{\text{DTACK}}$ must toggle.

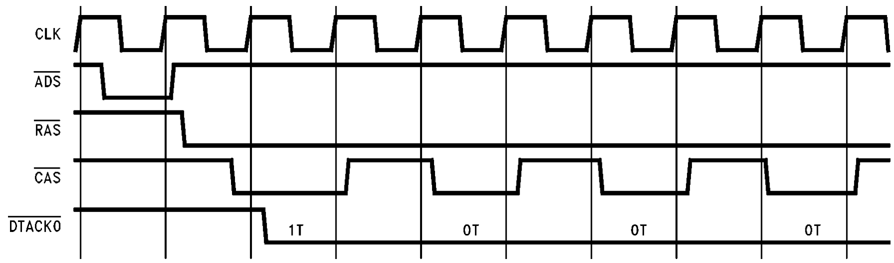

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FIGURE 23a. 1T during Opening and 0T during Burst. $\overline{\text{DTACK}}$ stays asserted during the burst.

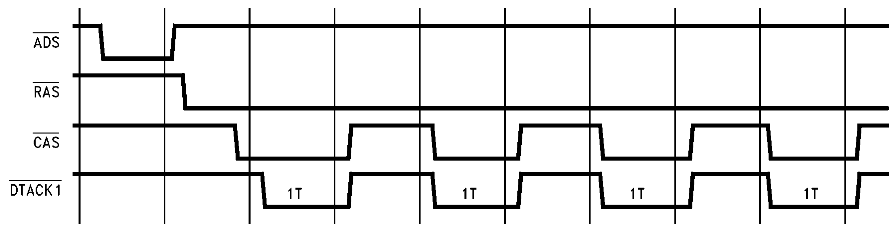

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FIGURE 23b. 1T during Opening, 1T during Burst

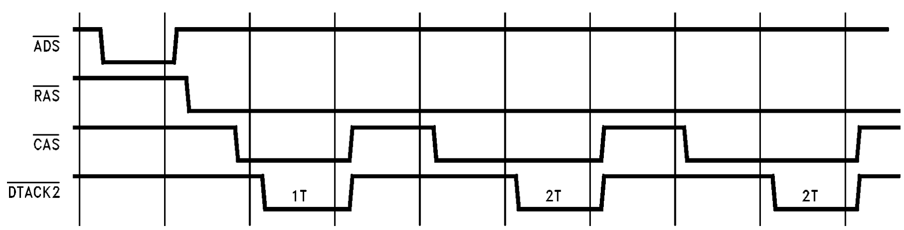

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FIGURE 23c. 1T during Opening, 2T during Burst

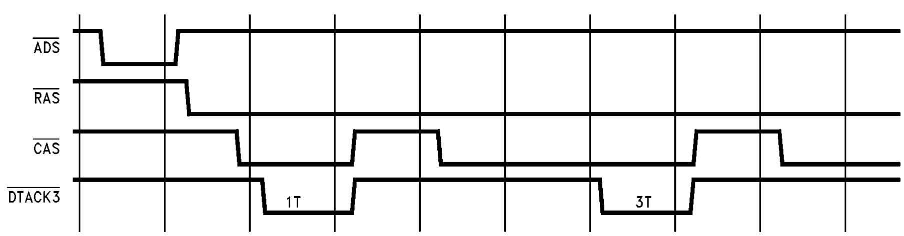

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FIGURE 23d. 1T during Opening, 3T during Burst

7.0 Wait Support (Continued)

7.4 $\overline{\text{NADTACK}}$

During any accesses, this output asserts one clock period before $\overline{\text{DTACK}}$ asserts, except when $\overline{\text{DTACK}}$ is programmed for 1T in normal accesses or 0T during page or burst accesses.

The user can use this output to request the next address in a sort of pipelining fashion. This output can also be used to generate a more accurate $\overline{\text{DTACK}}$ for special applications. The next figures show how $\overline{\text{NADTACK}}$ asserts in different cases.

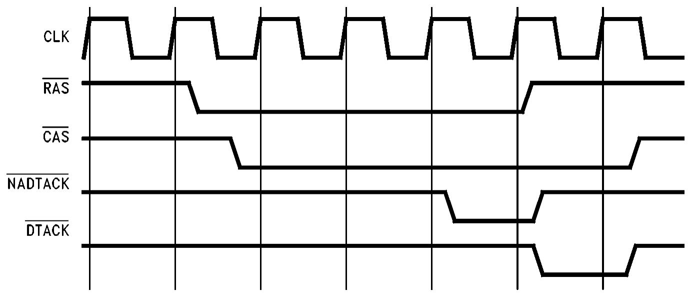

FIGURE 24a. $\overline{\text{DTACK}}$ is Programmed for 4Ts and to Assert from the Rising CLK Edge

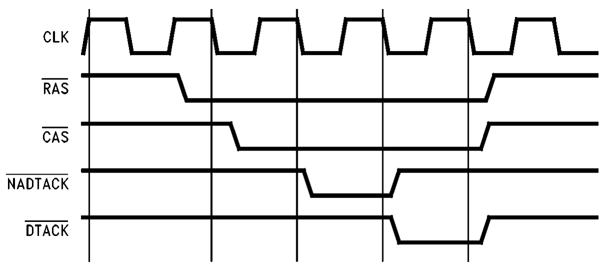

FIGURE 24b. $\overline{\text{DTACK}}$ is Programmed for 2Ts and to Assert from the Falling CLK Edge

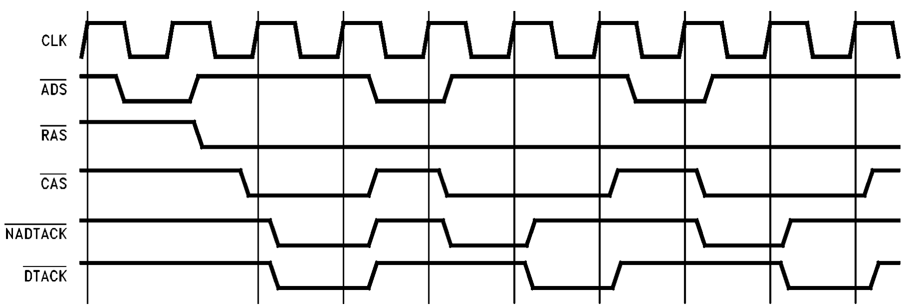

FIGURE 24c. $\overline{\text{DTACK}}$ and $\overline{\text{CAS}}$ assert from the rising edge of CLK. $\overline{\text{DTACK}}$ is programmed for 1T. $\overline{\text{NADTACK}}$ asserts with $\overline{\text{DTACK}}$ during the opening access. During Page Accesses, $\overline{\text{NADTACK}}$ asserts one clock before $\overline{\text{DTACK}}$.

8.0 Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input and Output Voltage with Respect to GND	−0.5V to +7V
ESD Rating	2000V

Recommended Operating Conditions

Supply Voltage, V_{CC}	4.75V to 5.25V
Operating Free Air Temperature	0°C to +70°C

9.0 DC Electrical Characteristics T_A = 0°C to +70°C, V_{CC} = 5V ±5%, GND = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logical 1 Input Voltage	Tested with a Limited Functional Pattern	2.00		V_{CC} + 0.5	V
V_{IL}	Logical 0 Input Voltage	Tested with a Limited Functional Pattern	−0.5		0.8	V
V_{OH1}	Q and $\overline{WE}$ Outputs	I_{OH} = −10 mA	V_{CC} − 1.0			V
V_{OL1}	Q and $\overline{WE}$ Outputs	I_{OL} = 10 mA			0.5	V
V_{OH2}	All Outputs Except Qs, $\overline{WE}$	I_{OH} = −5 mA	V_{CC} −1.0			V
V_{OL2}	All Outputs Except Qs, $\overline{WE}$	I_{OL} = 5 mA			0.5	V
I_{IN}	Input Leakage Current	V_{IN} = V_{CC} or GND	−10		10	μA
I_{CC2}	Supply Current	CLK at 40 MHz (I/Os Active)			260	mA
C_{IN}	Input Capacitance	f_{IN} at 1 MHz		5	10	pF

10.0 Load Capacitance

Q0–11	C_L = 50 pF
$\overline{WE}$	C_L = 50 pF
$\overline{RAS}$0–3	C_L = 50 pF
$\overline{CAS}$0–3	C_L = 50 pF (DP8440)
$\overline{CAS}$0–7	C_L = 50 pF (DP8441)
Other outputs	C_L = 50 pF

Adder Table for Higher Capacitive Loads

Output	ns/10 pF	Linear up to Maximum Load
Q0–11	0.350	360 pF max
$\overline{WE}$	0.548	500 pF max
$\overline{RAS}$0–3	0.282	125 pF max
$\overline{CAS}$0–3	0.282	125 pF max (DP8440)
$\overline{CAS}$0–7	0.334	67 pF max (DP8441)

11.0 AC Timing Parameters

Two speed selections are given, the DP8440/41-40 and the DP8440/41-25. The differences between the two parts are the maximum operating frequencies of the input CLKs and the maximum delay specifications. Low frequency applications may use the ‘‘-40’’ part to gain improved timing.

The AC timing parameters are grouped into sectional numbers as shown below. These numbers also refer to the timing diagrams.

1–6	Clock Parameters
50–53	TRI-STATE Parameters
100–109	Refresh Parameters
200–203	Programming Parameters
300–325	Common Parameters
400–423	Fast access parameters used in burst and Page Mode accesses

11.0 AC Timing Parameters (Continued)

#	Symbol	Description	DP8440/41-40 40 MHz Devices		DP8440/41-25 25 MHz Devices	
			Min	Max	Min	Max
CLOCK PARAMETER						
1	t_{CLKP}	Clock Period	25		40	
2, 3	t_{WCLK}	Clock Pulse Width	10		15	
4	t_{DCLKP}	DELCLK Period	25		25	
5, 6	t_{WDCLK}	DELCLK Pulse Width	10		10	
TRI-STATE PARAMETER						
50	t_{PZL}	TRI-STATE to Low Voltage Level		20		25
51	t_{PZH}	TRI-STATE to High Voltage Level		20		25
52	t_{PLZ}	Low Voltage Level to TRI-STATE		25		30
53	t_{PHZ}	High Voltage Level to TRI-STATE		25		30
REFRESH PARAMETER						
100	t_{SRFCK}	$\overline{RFSH}$ Asserted Set up to CLK High	6		8	
101	t_{HRFCK}	$\overline{RFSH}$ Asserted Hold Time	3		4	
102	t_{SDRFCK}	$\overline{DISRFSH}$ Asserted Setup to CLK High	6		8	
103	t_{HDRFCK}	$\overline{DISRFSH}$ Asserted Hold Time	3		4	
104	t_{PCKRFL}	CLK High to $\overline{RFIP}$ Asserted		17		20
105	t_{PCKRFH}	CLK High to $\overline{RFIP}$ Negated		34		36
106	t_{PCKRQL}	CLK High to $\overline{RFRQ}$ Asserted		13		15
107	t_{PCKRQH}	CLK High to $\overline{RFRQ}$ Negated		12		14
108	$t_{PCKRFRASL}$	CLK High to $\overline{RAS}$ Asserted During Refresh		23		25
109	$t_{PCKRFRASH}$	CLK High to $\overline{RAS}$ Negated During Refresh		19		21
PROGRAMMING PARAMETER						
200	t_{WML}	$\overline{ML}$ Pulse Width	15		15	
201	t_{SPBML}	Programming Bits Setup to $\overline{ML}$ High	18		18	
202	t_{HPBML}	Programming Bits Hold Time	6		6	
203	t_{PMLRFL}	$\overline{ML}$ High to $\overline{RFIP}$ Asserted		18		18

11.0 AC Timing Parameters (Continued)

#	Symbol	Description	DP8440/41-40 40 MHz Devices		DP8440/41-25 25 MHz Devices	
			Min	Max	Min	Max
COMMON PARAMETER						
300	t_{SADSCK}	$\overline{ADS}$ Asserted Setup to CLK High	10		12	
301	t_{SCSCK}	$\overline{CS}$ Asserted Setup to CLK High	10		12	
302a	t_{SADDCK}	Row, Column and Bank Address Valid Setup to CLK High	0		0	
302b	$t_{SADDCKP}$	Row and Bank Address Setup to CLK High in Page Mode Access	18		18	
303	t_{SCSADS}	$\overline{CS}$ Asserted Setup to $\overline{ADS}$ Negated	6		7	
304	t_{WADS}	$\overline{ADS}$ Pulse Width (Asserted)	6		6	
305	$t_{PCKRASL}$	CLK High to $\overline{RAS}$ Asserted		17		19
306	$t_{PCKRASH}$	CLK High to $\overline{RAS}$ Negated		18		20
307a	$t_{PRASCAS0}$	$\overline{RAS}$ Asserted to $\overline{CAS}$ Asserted (t_{RAH} = 10 ns)	20		20	
307b	$t_{PRASCAS1}$	$\overline{RAS}$ Asserted to $\overline{CAS}$ Asserted (t_{RAH} = 15 ns)	25		25	
308a	$t_{PCKCAS0}$	CLK High to Delay $\overline{CAS}$ Asserted (t_{RAH} = 10 ns)		60		60
308b	$t_{PCKCAS1}$	CLK High to Delay $\overline{CAS}$ Asserted (t_{RAH} = 15 ns)		65		65
309a	t_{RAH0}	Row Address Hold Time (t_{RAH} = 10 ns)	10		10	
309b	t_{RAH1}	Row Address Hold Time (t_{RAH} = 15 ns)	15		15	
310a	t_{PCKCV0}	CLK High to Column Address Valid (t_{RAH} = 10 ns)		52		52
310b	t_{PCKCV1}	CLK High to Column Address Valid (t_{RAH} = 15 ns)		57		57
311	t_{ASC}	Column Address Setup Time (t_{ASC} = 0 ns)	0		0	
312	$t_{PECSCASL}$	$\overline{ECAS}$ Asserted to $\overline{CAS}$ Asserted		14		16
313	$t_{PECSCASH}$	$\overline{ECAS}$ Negated to $\overline{CAS}$ Negated		14		16
314	t_{PAQ}	Row, Column and Bank Address to Q Valid		17		18
315	t_{PWINWE}	$\overline{WIN}$ to $\overline{WE}$ Out		14		16
316	t_{PCKDTL}	CLK High to $\overline{DATCK}$ Asserted		15		17
317	t_{PCKDTH}	CLK High to $\overline{DTACK}$ Negated		15		17
318	$t_{PCKLDTL}$	CLK Low to $\overline{DATCK}$ Asserted		16		18
319	$t_{PCKLDTH}$	CLK Low to $\overline{DTACK}$ Negated		16		18
320	$t_{PCKNADL}$	CLK High to $\overline{NADTACK}$ Asserted		15		17
321	$t_{PCKNADH}$	CLK High to $\overline{NADTACK}$ Negated		15		17
322	$t_{PCKLNADL}$	CLK Low to $\overline{NADTACK}$ Asserted		15		17
323	$t_{PCKLNADH}$	CLK Low to $\overline{NADTACK}$ Negated		15		17
324a	$t_{PRASCV0}$	$\overline{RAS}$ Asserted to Column Address Valid (t_{RAH} = 10 ns)		38		38
324b	$t_{PRASCV1}$	$\overline{RAS}$ Asserted to Column Address Valid (t_{RAH} = 15 ns)		43		43
325	t_{HCSCK}	$\overline{CS}$ Asserted Hold from CLK High	3		4	

11.0 AC Timing Parameters (Continued)

#	Symbol	Description	DP8440/41-40 40 MHz Devices		DP8440/41-25 25 MHz Devices	
			Min	Max	Min	Max
FAST ACCESS PARAMETER						
400	$t_{PCKCASL}$	CLK High to $\overline{CAS}$ Asserted		15.5		16
401	$t_{PCKCASH}$	CLK High to $\overline{CAS}$ Negated		17.5		18
402	$t_{PCKLCASL}$	CLK Low to $\overline{CAS}$ Asserted		18.5		19
403	$t_{PCKLCASH}$	CLK Low to $\overline{CAS}$ Negated		18.5		19
404	t_{WCASPC}	$\overline{CAS}$ Precharge when Programmed as ½T during Burst	10		10	
405	$t_{PCKCASB}$	CLK to $\overline{CAS}$ Asserted when Programmed as ½T during Burst	17	35	17	36
406	t_{PCKCVB}	CLK to Column Address Valid when B0 = 1 during Programming		27		27
407	$t_{PCKCVLB}$	CLK to Column Address Valid when B0 = 0 during Programming		32		32
408	t_{PCKPMH}	CLK to PAGMISS Asserted During Burst and NoWRAP		14		14
409	t_{SBARCK}	BSTARQ Asserted Setup to CLK	10		10	
410	$t_{HBARNCK}$	BSTARQ Asserted Hold from CLK (CLK following $\overline{DTACK}$ Negation)	16		17	
411	t_{SNWCK}	NoWRAP Asserted Setup to CLK ($\overline{NADTACK}$)	5		6	
412	t_{HNWCK}	NoWRAP Asserted Hold from CLK ($\overline{DTACK}$)	5		6	
413	t_{SNLADS}	$\overline{NoLATCH}$ Asserted Setup to $\overline{ADS}$	5		6	
414	t_{HNLCK}	$\overline{NoLATCH}$ Asserted Hold from CLK	5		6	
415	t_{SPMCK}	PAGMISS Input Asserted Setup to CLK	16		16	
416	t_{HPMCK}	PAGMISS Input Asserted Hold from CLK	5		6	
417	$t_{PADDPMH}$	Row and Bank Address Valid to PAGMISS Asserted		13		13
418	t_{PCKPML}	CLK High to PAGMISS Negated		17		17
419	t_{SWICLK}	$\overline{WAITIN}$ Asserted Setup to CLK ($\overline{NADTACK}$)	5		6	
420	t_{HWICLK}	$\overline{WAITIN}$ Asserted Hold from CLK ($\overline{NADTACK}$)	5		6	
421	$t_{SADSCKP}$	$\overline{ADS}$ Setup to CLK in Page Mode	22		22	
422	$t_{PADSPMH}$	$\overline{ADS}$ to PAGMISS High in Page Mode		16		16
423	$t_{HADSCKP}$	$\overline{ADS}$ Hold from CLK before Assertion in Page Mode	4		4	
424	t_{SCSKP}	$\overline{CS}$ Setup to CLK in Page Mode	22		22	

12.0 AC Timing Waveforms: DP8440/41

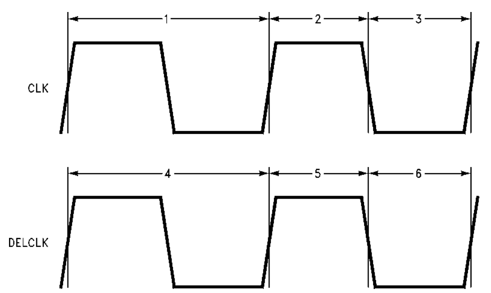

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FIGURE 25. CLK and DELCLK Timing

Number	DP8440/41-40		DP8440/41-25	
	Min	Max	Min	Max
1	25		40	
2	10		15	
3	10		15	
4	25		25	
5	10		10	
6	10		10	

12.0 AC Timing Waveforms: DP8440/41 (Continued)

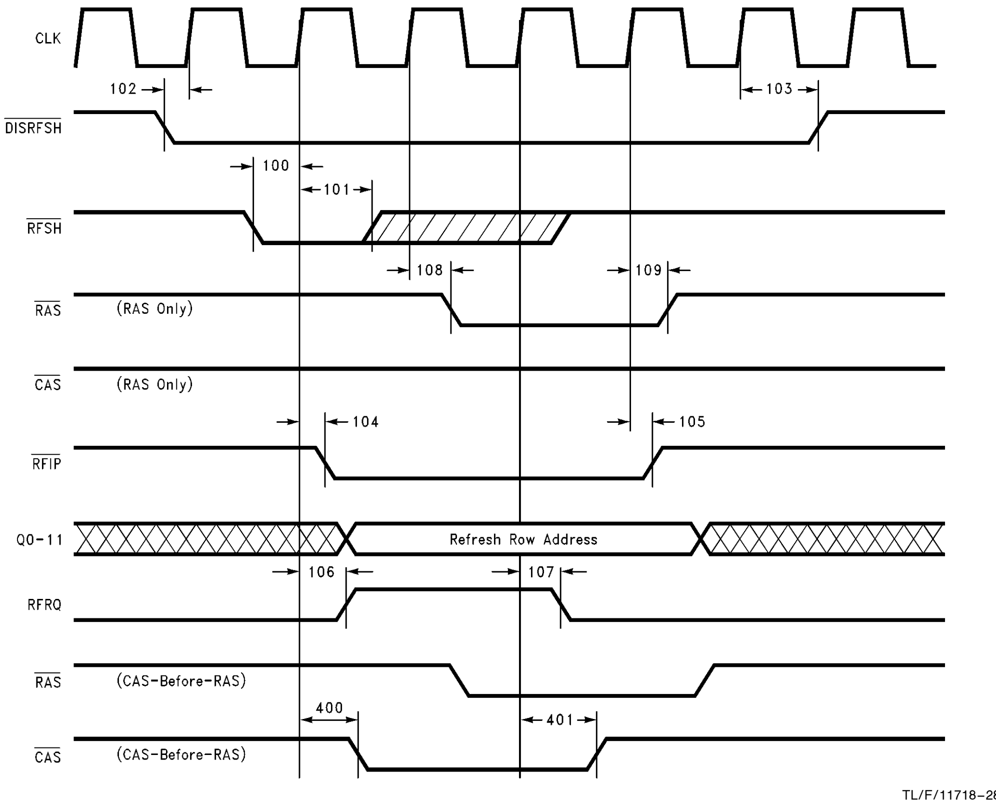

FIGURE 26. Refresh Timing

DP8440/41-40

Number	Min	Max
100	6	
101	3	
102	6	
103	3	
104		17
105		34
106		13
107		12
305		17
306		18
400		15.5
401		17.5

DP8440/41-25

Number	Min	Max
100	8	
101	4	
102	8	
103	4	
104		20
105		36
106		15
107		14
305		19
306		19
400		16
401		18

12.0 AC Timing Waveforms: DP8440/41 (Continued)

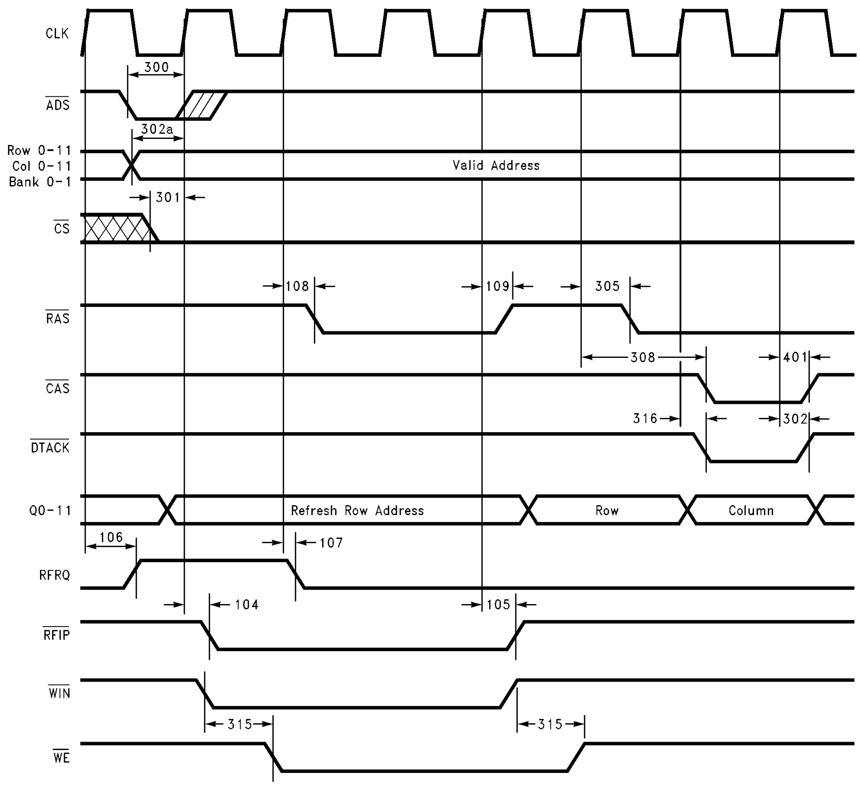

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FIGURE 27. Refresh and Access Timing

Number	DP8440/41-40		DP8440/41-25	
	Min	Max	Min	Max
104		17		20
105		34		36
106		13		15
107		12		14
300	10		12	
301	10		12	
302a	0		0	
302b	18		18	
305		17		19
306		18		19
308a		60		60
308b		65		65
315		14		16
316		15		17
401		17.5		18

12.0 AC Timing Waveforms: DP8440/41 (Continued)

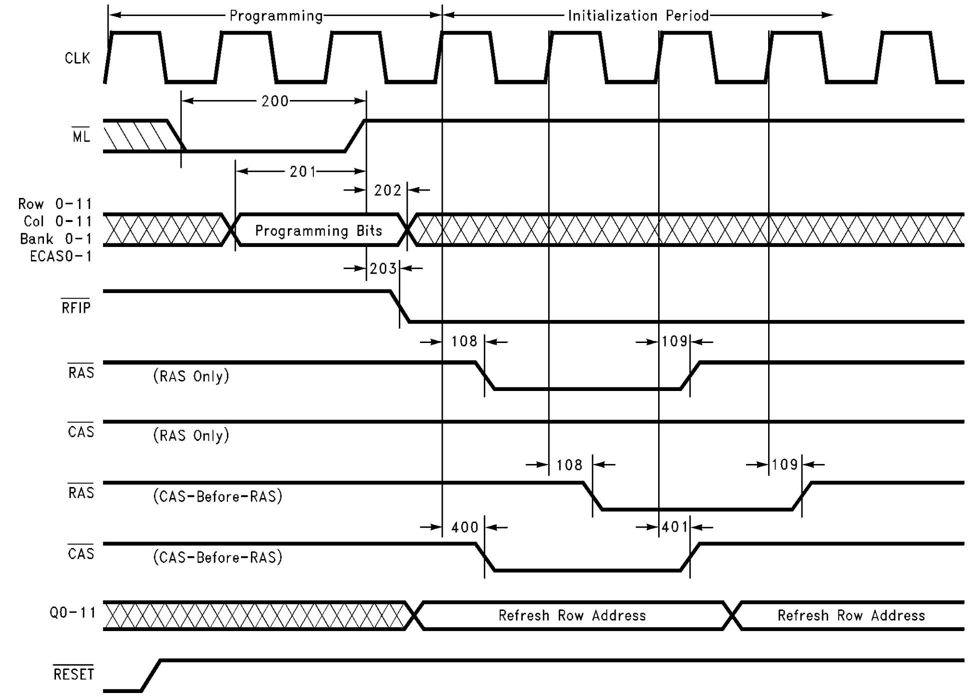

FIGURE 28. Programming and Initialization Period Timing

Number	Min	Max
200	15	
201	18	
202	6	
203		18

12.0 AC Timing Waveforms: DP8440/41 (Continued)

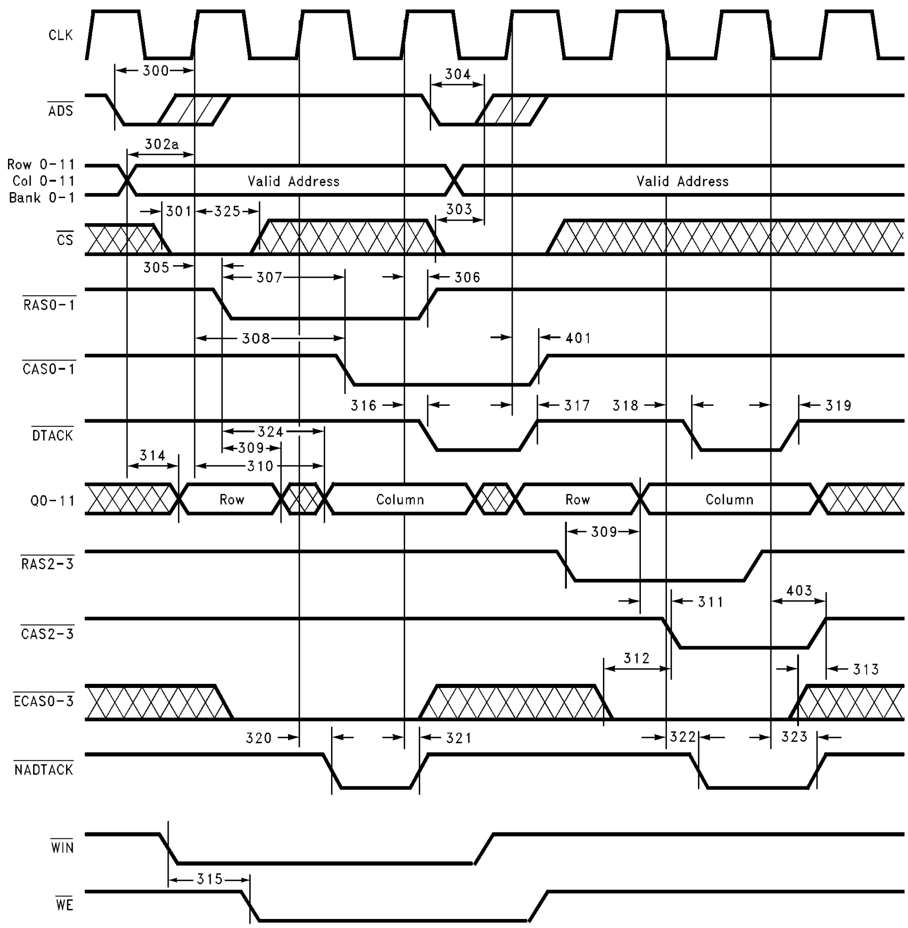

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FIGURE 29a. Normal Mode Access Timing—DP8440/41-40

Number	DP8440/41-40	
	Min	Max
300	10	
301	10	
302a	0	
303	6	
304	6	
305		17
306		18
307a	20	
307b	25	
308a		60

Number	DP8440/41-40	
	Min	Max
308b		65
309a	10	
309b	15	
310a		52
310b		57
311	0	
312		14
313		14
314		17
315		14

Number	DP8440/41-40	
	Min	Max
316		15
317		15
318		16
319		16
320		15
325	3	
400		15.5
401		17.5
402		18.5
403		18.5

12.0 AC Timing Waveforms: DP8440/41 (Continued)

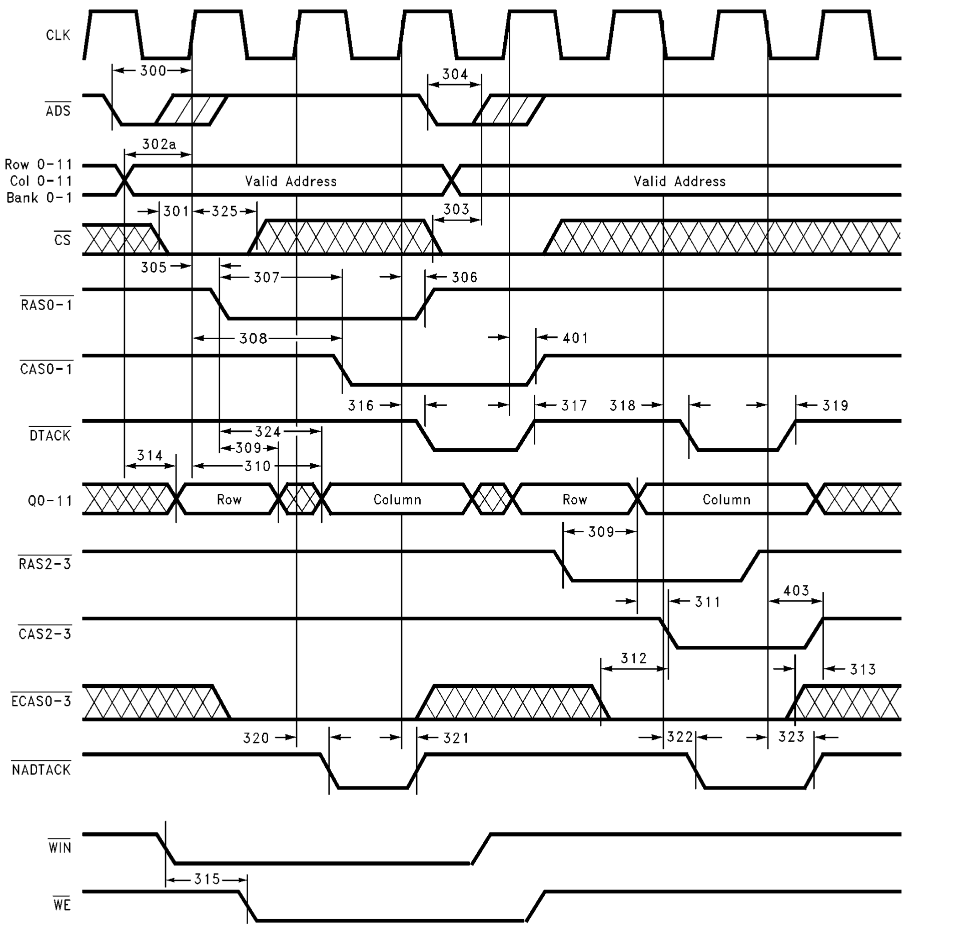

FIGURE 29b. Normal Mode Access Timing—DP8440/41-25

Number	DP8440/41-25 Min	DP8440/41-25 Max
300	12	
301	12	
302a	0	
303	7	
304	6	
305		19
306		19
307a	20	
307b	25	
308a		60

Number	DP8440/41-25 Min	DP8440/41-25 Max
308b		65
309a	10	
309b	15	
310a		52
310b		57
311	0	
312		16
313		16
314		18
315		16

Number	DP8440/41-25 Min	DP8440/41-25 Max
316		17
317		17
318		18
319		18
320		17
325	4	
400		16
401		18
402		19
403		19

12.0 AC Timing Waveforms: DP8440/41 (Continued)

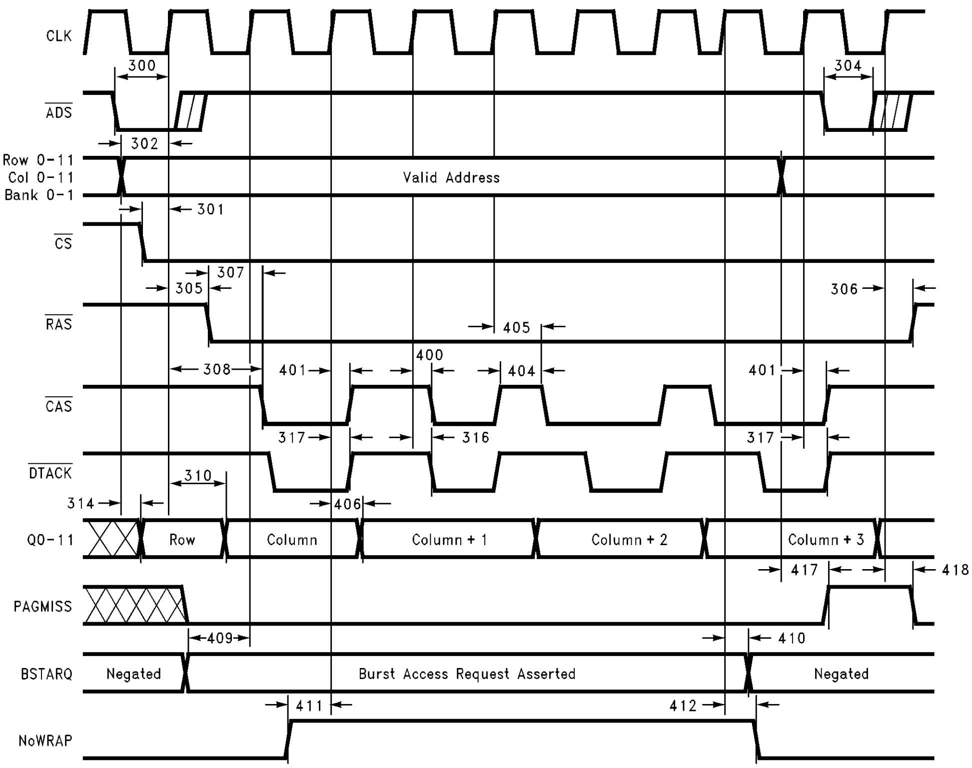

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FIGURE 30. Burst Mode Access Timing When Using Rising CLK Edge

Number	DP8440/41-40		DP8440/41-25	
	Min	Max	Min	Max
300	10		12	
301	10		12	
302a	0		0	
304	6		6	
305		17		19
306		18		19
307a	20		20	
307b	25		25	
308a		60		60
308b		65		65
310a		52		52
310b		57		57
314		17		18
316		15		17
317		15		17

Number	DP8440/41-40		DP8440/41-25	
	Min	Max	Min	Max
318		16		18
400		15.5		16
401		17.5		18
402		18.5		19
403		18.5		19
404	10		10	
405	17	35	17	36
406		27		27
409	10		10	
410	16		17	
411	5		6	
412	5		6	
417		13		13
418		17		17

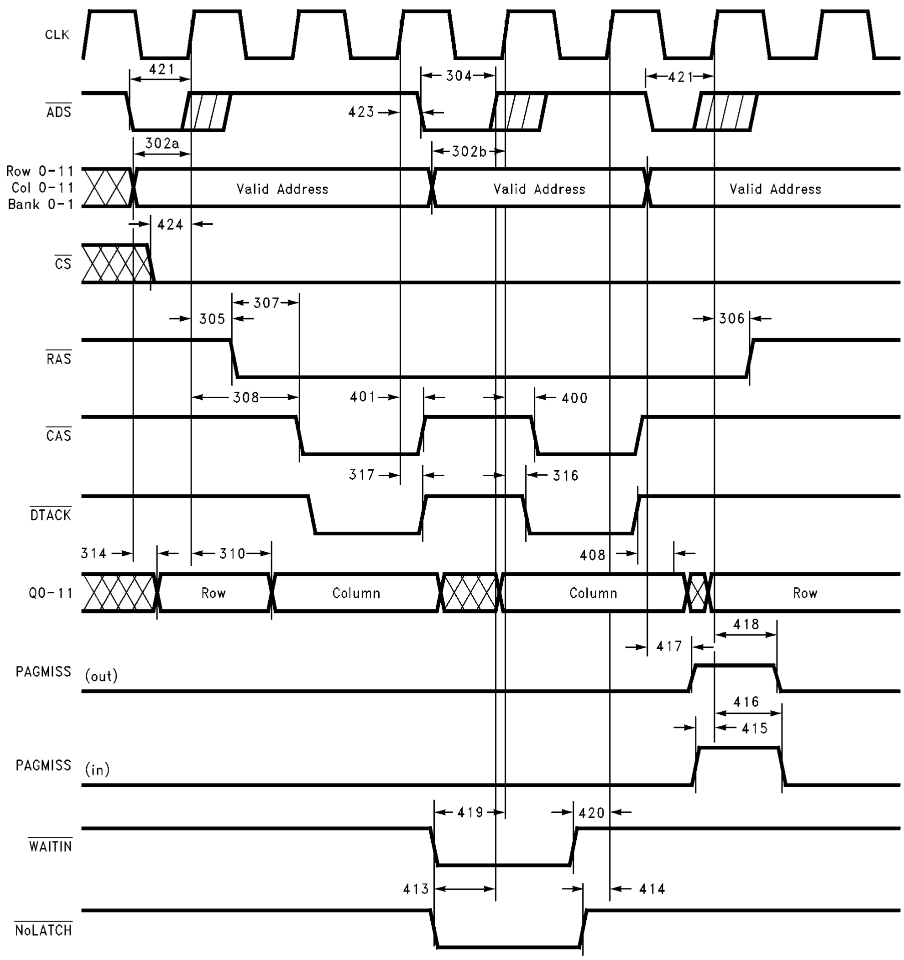

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FIGURE 31a. Page Mode Access Timing—DP8440/41-40

Number	DP8440/41-40	
	Min	**Max**
302b	21	
303	6	
304	6	
305		17
306		18
307a	20	
307b	25	
308a		60
308b		65

Number	DP8440/41-40	
	Min	**Max**
310a		52
310b		57
314		17
316		15
317		15
400		15.5
401		17.5
407		32
408		14
413	5	

Number	DP8440/41-40	
	Min	**Max**
414	5	
415	16	
416	5	
417		13
418		17
419	5	
420	5	
421	22	
423	4	
424	22	

12.0 AC Timing Waveforms: DP8440/41 (Continued)

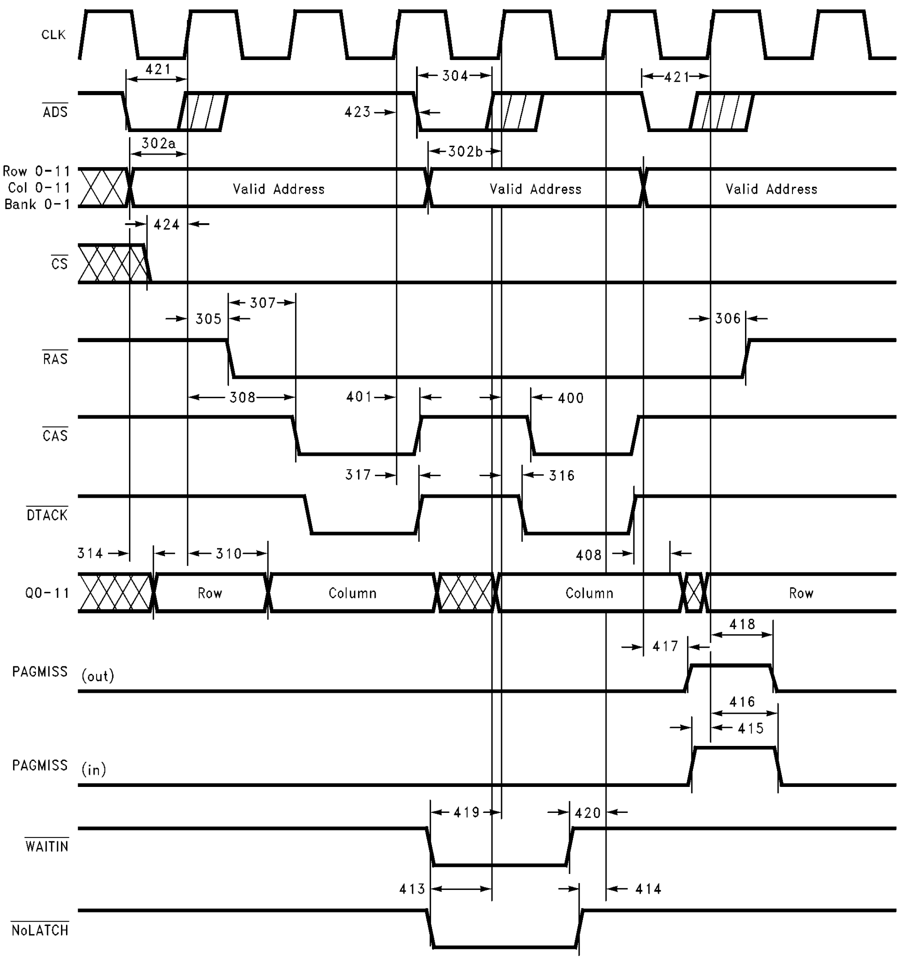

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FIGURE 31b. Page Mode Access Timing—DP8440/41-25

Number	DP8440/41-25	
	Min	Max
302b	18	
303	7	
304	6	
305		19
306		19
307a	20	
307b	25	
308a		60
308b		65

Number	DP8440/41-25	
	Min	Max
310a		52
310b		57
314		18
316		17
317		17
400		16
401		18
407		32
408		14
413	6	

Number	DP8440/41-25	
	Min	Max
414	6	
415	16	
416	5	
417		13
418		17
419	5	
420	5	
421	22	
423	4	
424	22	

12.0 AC Timing Waveforms: DP8440/41 (Continued)

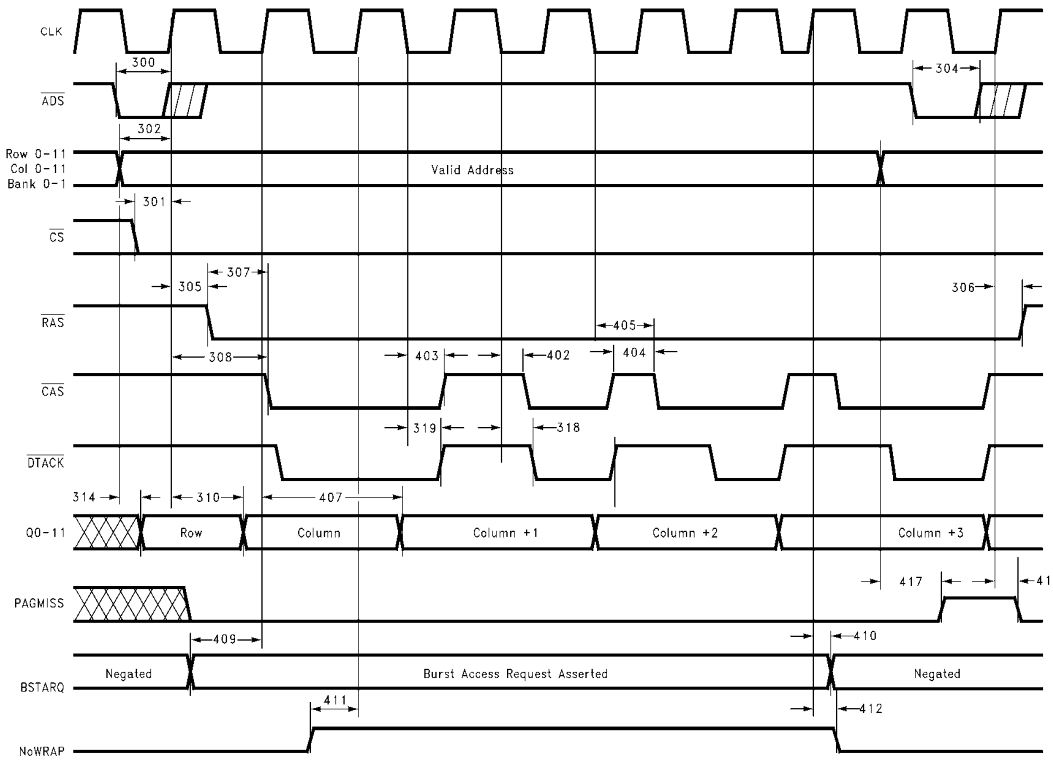

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FIGURE 32. Burst Mode Access Timing When Using Falling CLK Edge ($\overline{ECAS2}$ = 1)

Number	DP8440/41-40		DP8440/41-25	
	Min	Max	Min	Max
300	10		12	
301	10		12	
302b	21		18	
304	6		6	
305		17		19
306		18		19
307a	20		20	
307b	25		25	
308a		60		60
308b		65		65
310a		52		52
310b		57		57
314		17		18
316		15		17
317		15		17

Number	DP8440/41-40		DP8440/41-25	
	Min	Max	Min	Max
318		16		18
400		15.5		16
401		17.5		18
402		18.5		19
403		18.5		19
404	10		10	
405	17	35	17	36
407		32		32
409	10		10	
410	16		17	
411	5		6	
412	5		6	
417		13		13
418		17		17
419	5		6	

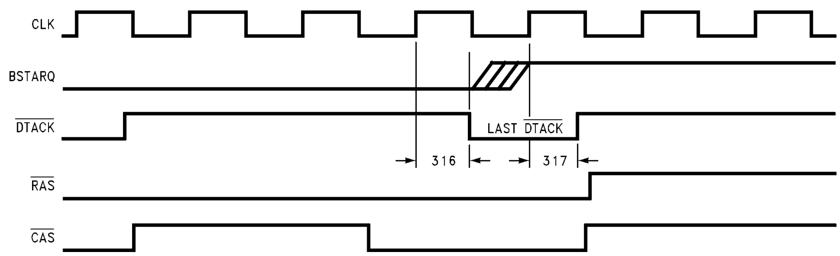
13.0 Errata for DP8440/41

ERRATUM #1

While programmed in Normal Mode, the $\overline{\text{RAS}}$ signals may negate ½ clock before the $\overline{\text{CAS}}$ signals for the last burst access. This can be a problem for write accesses, in which the $\overline{\text{RAS}}$ hold time may not be met for some DRAM arrays.

Recommended Fix

The $\overline{\text{RAS}}$ assertion time can be extended ½ clock by holding off the negation of the BSTARQ signal (Burst Access Request) until after the falling edge of the last $\overline{\text{DTACK}}$. If this approach is taken, then BSTARQ must then be negated before the clock edge which negates the last $\overline{\text{DTACK}}$ to guarantee no other accesses take place.



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ERRATUM #2

The NoWrap signal and EXTNDRF signal are multiplexed on the same pin. NoWrap is asserted when doing sequential burst acceses that don't wrap around. EXTNDRF (Extend Refresh) is used to extend a refresh while it is occurring.

A problem arises when a NoWrap burst access occurs slightly before or during a refresh cycle. The DP8440/41 goes into a refresh cycle, however, because the NoWrap/EXTNDRF signal is asserted, the refresh cycle may last indefinitely and the access will never complete.

Recommended Fix

The designer must be reminded that NoWrap/EXTNDRF are multiplexed and if NoWrap acceses are used in the design, it is recommended that the NoWrap be gated with the $\overline{\text{RFIP}}$ signal as outlined below.

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ERRATUM #3

The NoWrap signal and BSTARQ (Burst Request) signal should not be asserted on the same clock edge. This is only a problem when doing NoWrap burst accesses.

Recommended Fix

The NoWrap signal should be asserted from ONE clock after the BSTARQ signal is asserted. This will have no effect on the operation of the burst access and will prevent any problems from occurring.

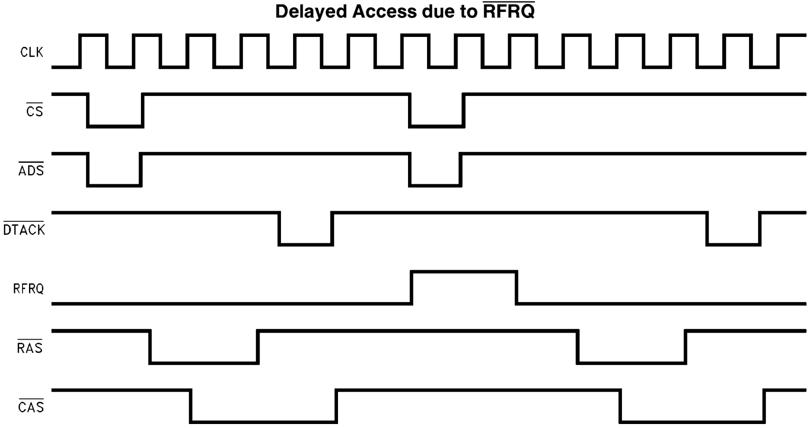
ERRATUM #4

When using external refreshes, the start of an access may be delayed slightly if the access occurs near the assertion of the RFRQ (Refresh Request) signal.

Recommended Fix

There is no guarantee the access will begin immediately after the assertion of $\overline{\text{ADS}}$, therefore, the internal timing signals, $\overline{\text{DTACK}}$ or $\overline{\text{NADTACK}}$, should always be used as a reference to generate the acknowledge signal to the CPU.

Delayed Access due to $\overline{\text{RFRQ}}$



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13.0 Errata for DP8440/41 (Continued)

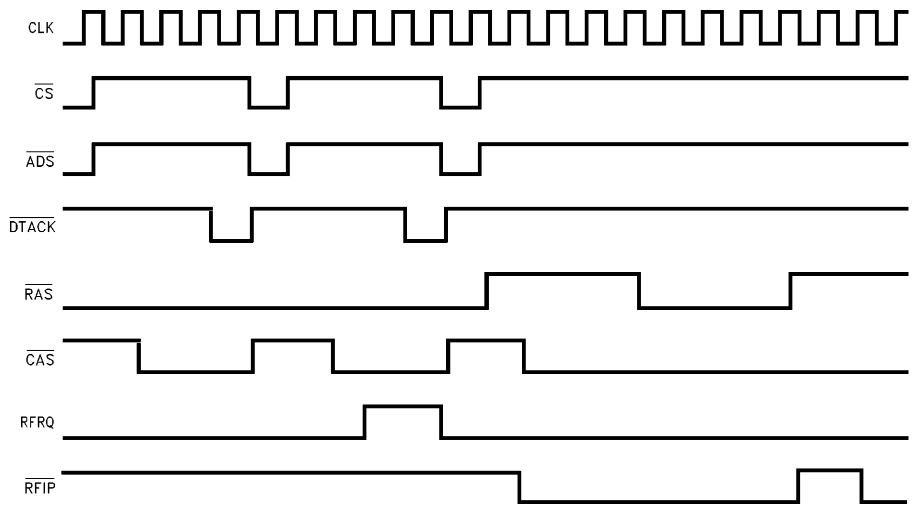
ERRATUM #5

When operating in Page Mode, an access cannot start on the clock edge immediately following the negation of $\overline{DTACK}$. If back-to-back accesses are done in this way, the $\overline{CAS}$ signals will remain low during a refresh as shown in the timing diagram.

Recommended Fix

There should be at least one idle clock between the negation of $\overline{DTACK}$ and the start of a new access.

Illegal Back-to-Back Accesses in Page Mode



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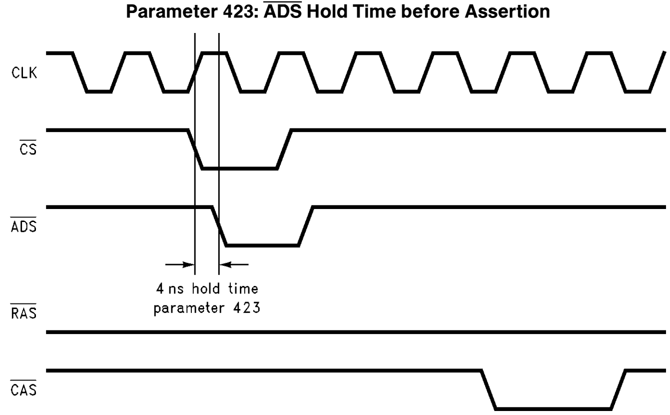
ERRATUM #6

When starting a page access, there is a hold time from the rising edge of the clock when $\overline{ADS}$ cannot assert. This hold time (parameter 423 in the datasheet) is 4 ns and only applies when operating in Page Mode.

Recommended Fix

$\overline{ADS}$ assertion should be delayed at least 4 ns from the rising edge of the clock when in Page Mode operation.

Parameter 423: $\overline{ADS}$ Hold Time before Assertion



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13.0 Errata for DP8440/41 (Continued)

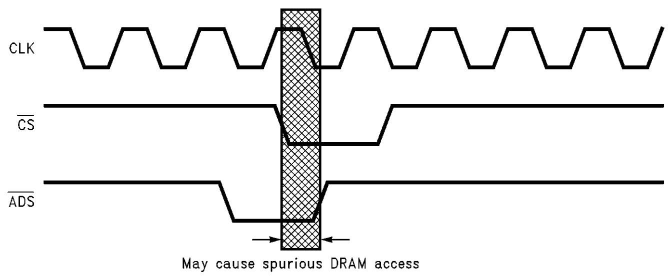
ERRATUM #7

Both $\overline{CS}$ and $\overline{ADS}$ are sampled asynchronously to the clock, consequently there should be no overlap in their assertion unless an access is being attempted.

Recommended Fix

Avoid asserting $\overline{CS}$ and $\overline{ADS}$ simultaneously unless attempting a DRAM access.

Illegal Overlap of $\overline{CS}$ and $\overline{ADS}$



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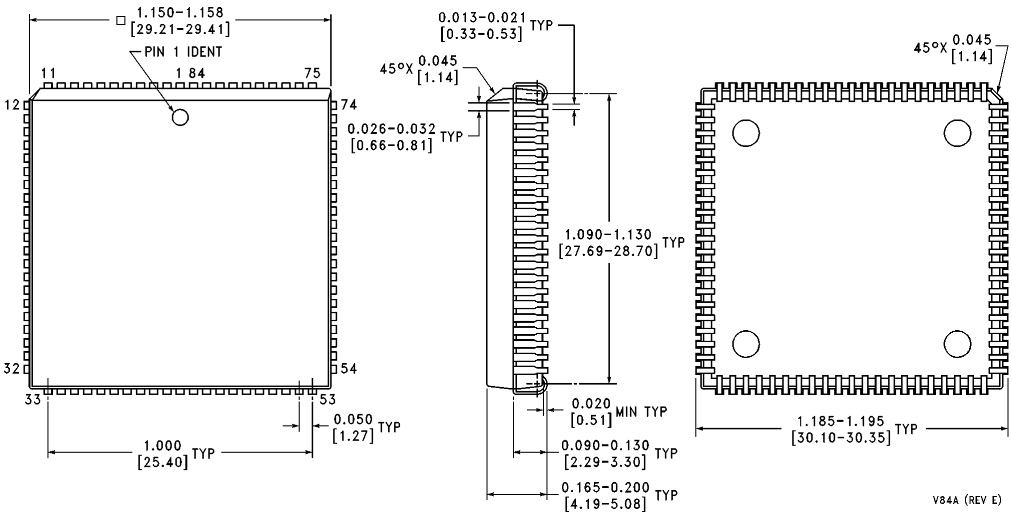
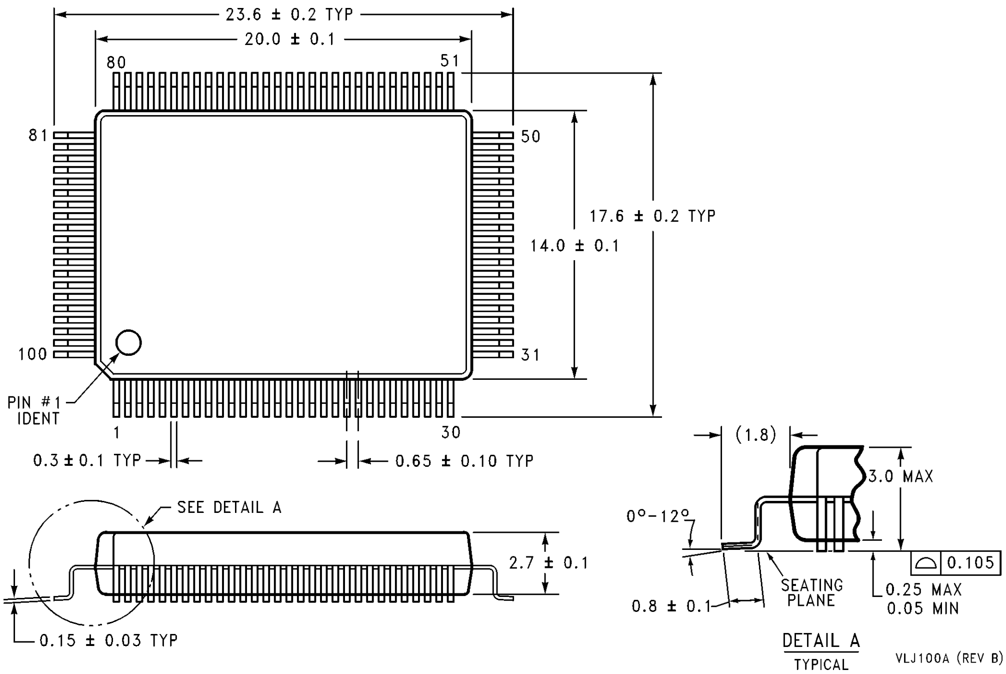
14.0 Physical Dimensions inches (millimeters)



Plastic Chip Carrier (PLCC)
Order Number DP8440V-40
NS Package Number V84A

14.0 Physical Dimensions inches (millimeters) (Continued)



100-Lead Plastic Quad Flatpak (PQFP)
Order Number DP8440VLJ-40, DP8440VLJ-25, DP8441VLJ-40 or DP8441VLJ-25
NS Package Number VLJ100A

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