Subject:	Additional Information
Data Sheet Concerned:	DMA 2275, DMA 2286 6251-330-1E, 06/92
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The DMA 2386 is hardware and software compatible to the DMA 2286.

Software and hardware changes have been implemented in a fully compatible way, allowing the new DMA 2386 to replace the DMA 2286 in existing applications. Of course, only adapted software can benefit from the new features.

Software control is achieved by using already existing registers of the DMA 2286. The new defined bits are unused in the existing DMA 2286 specification and ‘0’ is the compatible state.

Changes between the DMA 2286 and the DMA 2386:

1. Digital E7 De-emphasis Filter

E7 is a nonlinear pre/de-emphasis which has been developed at the IBA to provide noise reduction for MAC satellite transmission. Until now, all MAC receivers using the ITT chip set have an analog E7 de-emphasis implemented. Analog E7 de-emphasis does not have linear phase characteristic and is not really complementary to the E7 pre-emphasis.

The DMA 2386 contains a digital E7 de-emphasis filter as specified by the IBA. The SCRAM_MODE register is used to control E7 de-emphasis. Bits 5 and 6 have been changed in the DMA 2386.

Mode Register

Name	Address	Function
mode_register	**0000**	**6*8 bit**
scram_mode	0010	8 bit bit 0: video descrambling (0 = on) bit 1: video rotation (0 = double / 1 = single) bit 2: aspect ratio (0 = 4:3 / 1 = 16:9) bit 3: vbi descrambling (1 = on) bit 4: coeff clock (1 = on) **bit 5: video E7 (1 = on)** **bit 6: baseband E7 (1 = on)** bit 7: user panning (1 = on)

Video E7 is only active during the chroma and luma components of the incoming baseband signal, baseband E7 is active all the time. Baseband E7 overwrites video E7.

The E7 de-emphasis filter is designed for 9-bit binary input. For real 9-bit A/D converters, pin 34 of the DMA 2386 is chosen as an additional LSB input. In this case, the gray decoder must be switched off and the A/D converter should deliver binary output.

2. Synchronization of Audio Descrambling (BC1/BC2)

Audio descrambling can be synchronized with the BC1/BC2 transition of the related sound packets. After a change of audio scrambling has been indicated in the BI packets, the decoder switches to the new configuration at the beginning of the third packet after the BC1/BC2 transition.

Audio descrambling is controlled by the SPS register. Bit 5 has been changed in the DMA 2386.

Pac1 Register

Name	Address	Function
pac1_register	**0100**	**12*8 bit**
spa_reg	0100	4*2*8 bit bit 9–0: packet address
sps_reg	0140	4*8 bit bit 0: packet descrambling (1 = on) bit 2,1: packet location (01 = 1st subframe) (10 = 2nd subframe) (00 = both subframes) (11 = both subframes) bit 3: packet remove (1 = on) bit 4: automode (1 = on) **bit5: update bit 0 (0 = always)** **(1 = BC synced)**

The packet descrambler of the DMA 2386 updates bit0 of the SPS register only after a BC1/BC2 transition has been detected. For compatibility reasons, the packet descrambler can be forced to update bit0, all the time, by holding the new bit5 of the SPS register at ‘0’.

The BI packet information “scrambling/no scrambling” can therefore be used for each of the four packet descramblers. To switch between free-access and controlled-access, two packet descramblers must be used in parallel. Both are programmed with the same packet address, but one is loaded with the fixed control word and one with the conditional access control word. Only one of them is enabled at a time, and the switch over is controlled by the BC1/BC2 transition.

3. Cut Point Noise Cleared

4. Video Timing Corrected

5. Corrected Golay Decoding of Linked Packets

6. New Output Stages of DRAM Interface