Subject:	Additional Information
Data Sheet Concerned:	DMA 2271, DMA 2280, DMA 2281 6251-331-1E, 08/91
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The DMA 2381 can replace the DMA 2281.

Software changes are only needed to achieve improved functionality.

Hardware changes are only needed to optimize improved functionality.

Changes between the DMA 2281 and the DMA 2381:

1. Luma and chroma interpolation filters (see attachment)
   - Luma interpolation filters have been improved in bandwidth and noise performance.
   - Chroma interpolation filters have been improved in noise performance.
2. Vertical blank circuit
   - Luma and chroma have been set to black from lines 1 to 23, lines 311 to 335, and lines 623 to 625.
   - If ‘VPSD’ is set to zero, the luma signal of line 16 is not blanked. This is required for VPS acquisition.
3. AGC circuit with PWM output, polarity, and tristate
   - The number of samples used to measure the amplitude of the digitized baseband signal has been increased from 8 to 128.
   - If ‘IAGC’ is set to 1, the AGC output (pin 49) supplies a 16 level PWM signal instead of a 3 level signal.
   - If ‘AGCP’ is set to 1, the polarity of the AGC output is inverted.
   - If ‘AGCT’ is set to 1, the AGC output signal (PWM) supplies three levels: high, low, and tristate.
4. Clamping circuit with PWM output, polarity, and tristate
   - The number of samples used to measure the DC level of the digitized baseband signal has been increased from 8 to 14.
   - If ‘DCLE’ is set to 1, all ‘zero cross points’ detected in the databurst are used to measure the DC level of the digitized baseband signal in addition to the 14 samples during the clamping period.
   - If ‘TZE’ is set to 1, only triple ‘zero cross points’ in the databurst are used to measure the DC level of the digitized baseband signal.
   - If ‘ICLE’ is set to 1, the integral clamp loop is activated.
   - If ‘CLMP’ ist set to 1, the polarity of the clamping output is inverted.
   - If ‘CLMT” is set to 1, the clamp output signal (PWM) supplies three levels: high, low, and tristate.

5. Slave mode for S_BUS interface

   – If ‘SBS’ is set to 1, the S_BUS interface is set to slave mode for applications with MSP 3410/MSP 3400. In this mode
     – S_IDENT signal becomes an input signal
     – Audio clock output signal (pin 65) supplies an 18 kHz reference signal for MSP 3410/MSP 3400
     – pin XTAL2 (pin 17) is used as an 18.432 MHz input signal supplied from MSP 3410/MSP 3400 (internal load capacitor = 0 pF)

   – In S_BUS slave mode operation, “DCOF” should be set to 1 to achieve minimum input capacitance at clock input XTAL2 (pin 17).

6. Soft reset for sound processing part

   – If ‘SR’ is set to 1, the sound processing part of the DMA 2381 is reset.

The following IM Bus bits have been added in Table 4–1 and Table 4–3.

VPSD	VPS Disable	0 = line 16 is not blanked 1 = line 16 is blanked
SR	Sound Reset	0 = normal operation 1 = sound part of DMA 2381 is reset
IAGC	Improved AGC	0 = AGC compatible to DMA 2281 1 = improved AGC enabled
DCLE	Digital Clamp Enable	0 = clamping compatible to DMA 2281 1 = digital clamp enabled
TZE	Triple Zero Enable	0 = all ‘zero crossing points’ are used 1 = triple ‘zero crossing points’ are used only
ICLE	Integral Clamp Enable	0 = clamping compatible to DMA 2281 1 = integral clamp enabled
TPE	Tristate Polarity Enable	0 = CLMP, CLMT, AGCP and AGCT don’t care compatible to DMA 2281 1 = CLMP, CLMT, AGCP and AGCT enabled
CLMP	Clamping Polarity	0 = compatible to DMA 2281 1 = polarity of clamping output is inverted
CLMT	Clamping Tristate	0 = compatible to DMA 2281 1 = tristate of clamping output is enabled
AGCP	AGC Polarity	0 = compatible to DMA 2281 1 = polarity of clamping output is inverted
AGCT	AGC Tristate	0 = compatible to DMA 2281 1 = tristate of AGC output is enabled
SBS	S_BUS Slave	0 = compatible to DMA 2281 1 = S_BUS slave mode enabled
DCOF	DCO_Forced	0 = audio clock DCO normal operation 1 = audio clock DCO forced to minimum input capacitance (XTAL2)

Attachments:
– IM_Bus register list of the DMA 2381
– Frequency response of the DMA 2381 luma and chroma filters

4.3.1. Control and Status Registers

Note: unused bits must be set to zero for control (receive) registers and are don't care for status (transmit) registers.

Table 4–1: 16-bit DMA control registers, instructions from CCU to DMA

Address	Label	Bit No.	Default Setting	Typical Value	Function
14	VCOA	0–7	0	0	VCO adjustment (range –128...+127) alignment of the 20.25 MHz VCO
14	VCOS	8–10	4	4	VCO select 1 = VCO3 selected 2 = VCO2 selected 4 = VCO1 selected
14	DI1 DI2 DI3	11 14 15	0	0	disable PLL output (pin 25, 26) if (DI1 . or . DI2 . or DI3) then PLL output = high impedance
23	SAV	2–7	32	25	saturation V adjust 0: gain = 0 63: gain = 2
23	SAU	10–15	32	18	saturation U adjust 0: gain = 0 63: gain = 2
200	LD	3–7	4	6	luma delay adjust (range 0...30) resolution: 20.25 MHz clock
200	CTS	8	0	1	luma contrast switch
200	CT	10–15	32	16	luma contrast adjust 0: gain = 0 63: gain = 1 if CTS = 1 63: gain = 2 if CTS = 0
201	DSY	0	1	0	disable sync outputs (pins 50–53, 58–60) 0 = enabled 1 = high impedance
201	DCL	1	0	0	disable clamping output (pin 48) 0 = enabled 1 = high impedance
201	DLC	2	0	0	disable luma/chroma output (pin 21–24, 27–38) 0 = enabled 1 = high impedance
201	NIN	3	0	0	non interlace 0 = interlace on 1 = interlace off
201	PLLO	4	0	0	PLL open 0 = PLL closed 1 = PLL opened
201	STA	5	0	0	stand alone operation 0 = digital insertion 1 = stand alone
201	CMP	6	0	0	chroma output multiplex 0 = 4 x 4 multiplex 1 = 2 x 8 multiplex

Table 4–1, continued

Address	Label	Bit No.	Default Setting	Typical Value	Function
201	DGC	7	0	0	disable gray code converter input signal (pin 39–45) 0 = gray coded 1 = binary coded
201	L525	8	0	0	525 lines standard select 0 = 625 lines standard selected 1 = 252 lines standard selected
201	LF	10–11	0	0	luma filter selection
201	CF	13–15	0	0	chroma filter selection
202	BD	1–7	64	64	horizontal blank delay adjust (pin 50–52) resolution: 10.125 MHz clock
202	VPSD	8	0	0	VPS disable 0 = line 16 is not blanked 1 = line 16 is blanked
202	SD	9–15	64	64	comp. sync delay adjust (pin 53) resolution: 10.125 MHz clock
203	C1A	0–9	0	128	channel 1 packet address
203	C1E	10	0	1	channel 1 enable
203	C1U	11	0	0	channel 1 mode update
203	C1M	12–15	0	12	channel 1 mode × × × × linear/nicam hamming/parity protection high/medium quality stereo/mono
194	see register 203				channel 2
195	see register 203				channel 3
196	see register 203				channel 4
197	SFS	0–10	7	7	subframe select SFS = sample number of the first bit in the selected subframe examples: DRS = 1, first subframe SFS = 7 DRS = 1, second subframe SFS = 106 DRS = 0, first subframe SFS = 14
197	SR	12	0	0	sound reset 0 = normal operation 1 = sound part of DMA 2381 is reset
197	CD	13	0	0	chip definition 0 = DMA 2280 1 = DMA 2285
197	AUM	14	0	0	auto mode 0 = auto mode off 1 = sound coding in packet header
197	DRS	15	0	1	data rate select 0 = 10.125 Mbits/s D2-MAC 1 = 20.25 Mbits/s C/D-MAC

Table 4–1, continued

Address	Label	Bit No.	Default Setting	Typical Value	Function
198	AGCT	0	0	0	AGC tristate 0 = compatible to DMA 2281 1 = tristate of AGC output is enabled
198	AGCP	1	0	0	AGC polarity 0 = compatible to DMA 2281 1 = polarity of clamping output is inverted
198	CLMT	2	0	0	clamping tristate 0 = compatible to DMA 2281 1 = tristate of clamping output is enabled
198	CLMP	3	0	0	clamping polarity 0 = compatible to DMA 2281 1 = polarity of clamping output is inverted
198	CLG	4–5	0	2	clamping loop gain
198	TPE	9	0	0	tristate polarity enable 0 = CLMP, CLMT, AGCP and AGCT don’t care compatible to DMA 2281 1 = CLMP, CLMT, AGCP and AGCT enabled
198	ICLE	10	0	0	integral clamp enable 0 = clamping compatible to DMA 2281 1 = integral clamp enabled
198	TZE	11	0	0	triple zero enable 0 = all ‘zero crossing points’ are used 1 = triple ‘zero crossing points’ are used only
198	DCLE	12	0	0	digital clamp enable 0 = clamping compatible to DMA 2281 1 = digital clamp enabled
198	IAGC	13	0	0	integral clamp enable 0 = AGC compatible to DMA 2281 1 = improved AGC enabled
198	CS	14–15	0	0	chip select 0 = IM bus of DMA 2280 active 1 = IM bus of DMA 2285 active

Table 4–1, continued

Address	Label	Bit No.	Default Setting	Typical Value	Function
199	PLLS	0	0	0	PLL select 0 = D/D2 MAC PLL 1 = CMAC PLL
199	ENF2	1	0	0	enable filter 2 0 for C/D MAC 1 for D2 MAC
199	SLS	2–3	0	1	slicer select 0 for D2-MAC 1 for D-MAC 2 for C-MAC
199	PLLG	4–5	0	2	PLL gain 0 = maximal gain 3 = minimal gain
199	FCD	6	0	0	full channel data 0: DBW is gated (pin 52) 1: DBW is active all the time
199	BPH	7	0	0	burst phase 0 = with DMA 2285 1 = only DMA 2280
199	SLL	8–15	0	40 0	slice level (range –128...+127) for D/D2-MAC for C-MAC
204	SBE	0–3	0	15	S bus enable × × × × channel 1 enable channel 2 enable channel 3 enable channel 4 enable
204	DGT	4–7	0	0	data group type selection
204	POR	8	0	0	packet 0 reset 1: select first byte in packet 0 buffer (first byte = data group type DGT)
204	POC	9	0	0	packet 0 clear 1: enable packet 0 buffer to store next packet 0
204	DSB	10	1	0	disable S bus outputs (pins 64, 66, 67) 0 = enabled 1 = high impedance
204	ACS	11	1	1	audio clock switch (pin 65) 0: audio clock = main clock 1: audio clock = 18.432 MHz
204	ACF	12	1	0	audio clock free running 0 = audio clock locked to main clock 1 = audio clock free running
204	SBS	13	0	0	S bus slave 0 = compatible with DMA 2281 1 = S bus slave mode enabled
204	DCOF	14	0	0	0 = audio clock DCO normal operation 1 = audio clock DCO forced to minimum input capacitance (XTAL2)

Table 4–1, continued

Address	Label	Bit No.	Default Setting	Typical Value	Function
205	T0	0	0	0	for test only
205	T1	1	0	0	for test only
205	T2	2	0	0	for test only
205	T3	3	0	0	for test only
205	T4	4	0	0	for test only
205	T5	5	0	0	for test only
205	T6	6	0	0	enable PDAT input
205	T7	7	0	0	for test only
205	T8	8	0	0	disable error concealment
205	T9	9	0	0	for test only
205	T10	10	0	0	enable BDAT input
205	T11	11	0	0	for test only
205	T12	12	0	0	for test only
205	T13	13	0	0	disable luma/chroma interpolation filters
205	T14	14	0	0	for test only
205	T15	15	0	0	for test only

Table 4–2: 16-bit DMA status registers, information from DMA to CCU

Address	Label	Bit No.	Function
206	BER	0–7	bit error rate number of erroneous bits detected by the golay decoder within the 82 packet headers of one frame
206	VER	8–9	version 0: C/D/D2-MAC Decoder 1: D2-MAC Decoder 2: D-MAC Decoder 3: C/D2-MAC Decoder
206	C1S	10	status of sound signal selected by C1A 0: sound signal is inactive or interrupted 1: sound signal is present
206	C2S	11	status of sound signal selected by C2A 0: sound signal is inactive or interrupted 1: sound signal is present
206	C3S	12	status of sound signal selected by C3A 0: sound signal is inactive or interrupted 1: sound signal is present
206	C4S	13	status of sound signal selected by C4A 0: sound signal is inactive or interrupted 1: sound signal is present
206	P0S	14	status of packet 0 buffer 0: packet 0 selected by DGT not received 1: packet 0 received
206	SYNC	15	status of frame sync word detector 0: frame sync word not detected within 8 frames 1: frame sync word detected
207	WL	0–7	white level measured in line 624 (typical value = 240)
207	BL	8–15	black level measured in line 624 (typical value = 16)
208	C1L	0–3	coding law of sound signal selected by C1A
208	C2L	4–7	coding law of sound signal selected by C2A
208	C3L	8–11	coding law of sound signal selected by C3A
208	C4L	12–15	coding law of sound signal selected by C4A L = 0: companded law 1: linear law H = 0: first level protection 1: second level protection HQ = 0: medium quality sound 1: high quality sound S = 0: monophonic sound 1: stereophonic sound
209	PSL	0–7	packet 0 syndrom low byte
209	PSH	8–15	packet 0 syndrom high byte PSL + PSH = 0: packet 0 received without error PSL + PSH > 0: packet 0 received with error
210	PDL	0–7	packet 0 data low byte
210	PDH	8–15	packet 0 data high byte

Table 4–3: DMA control and status registers, graphical overview

Addr. No.	Bit No. / Direct.	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
14	W	DI3	DI2	⟋	⟋	DI1	VCOS			VCOA VCO Adjustment							
		0	0	0	0	0	1	0	0	0							
23	W	SAU Saturation U						☒	☒	SAV Saturation V						☒	☒
		28						0	0	40						0	0
200	W	CT Luma Contrast						CSE	CTS	LD Luma Delay					☒	☒	☒
		32						0	0	6					0	0	0
201	W	CFI Chroma Filter			CSP	LFI Luma Filter		CSP	L525 525 lines	DGC Disable Gray	CMP Chroma Mult.	STA Stand alone	PLLO PLL open	NIN Non Interl.	DLC Disable L/C	DCL Clamp. off	DSY Disable Sync.
		0			0	0		0	0	0	0	0	0	0	0	0	0
202	W	SD Composite Sync. Delay							VPSD VPS Disable	BD Blank Delay							☒
		64							0	64							0
203	W	C1M Channel Mode				C1U Mode Update	C1E Channel Enable			C1A Channel Packet Address							
		S	HQ	H	L	0	1			100							
194	W	C2M Channel Mode				C2U Mode Update	C2E Channel Enable			C2A Channel Packet Address							
		S	HQ	H	L	0	1			100							
195	W	C3M Channel Mode				C3U Mode Update	C3E Channel Enable			C3A Channel Packet Address							
		S	HQ	H	L	0	0			100							
196	W	C4M Channel Mode				C4U Mode Update	C4E Channel Enable			C4A Channel Packet Address							
		S	HQ	H	L	0	0			100							
197	W	DRS Data Rate Select	AUM Auto Mode	CD Chip Defin.	SR Sound Reset	☒				SFS Subframe Select							
		1	0	0	0	0				7							
198	W	CS Chip Select		IAGC Improved AGC	DCLE Digital Clamp Enable	TZE Triple Zero **Enable**	ICLE Integral Clamp Enable	TPE Tristate Polarity Enable	☒	☒	☒	CLG Clamping Loop Gain		CLMP Clamping Polarity	CLMT Clamping Tristate	AGCP AGC Polarity	AGCT AGC Tristate
		0		0	0	0	0	0	0	0	0	2		2	2	2	2
199	W	SLL Slice Level								BPH Burst Phase	FCD Full Chanel Data	PLLG PLL Gain		SLS Slicer Select		ENF2 Enable Filter 2	PLLT PLL Test
		0								0	0	2		1		0	0
204	W	⟋	DCOF DCO Forced	SBS S Bus Slave	ACF Audio Free	ACS Clock Switch	DSB Disable S Bus	P0C P0 Clear	P0R P0 Reset	DGT Data Group Type				SBE S Bus Enable			
		0	0	0	0	1	0	0	0	0				3			
205	W	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
		0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
206	R	SYNC	P0S	C4S	C3S	C2S	C1S	VER Version		BER Bit Error Rate							
		Status															
207	R	BL Black Level								WL White Level							
208	R	C4L Coding Law CH4				C3L Coding Law CH3				C2L Coding Law CH2				C1L Coding Law CH1			
		S	HQ	H	L	S	HQ	H	L	S	HQ	H	L	S	HQ	H	L
209	R	PSH Packet 0 Syndrom High Byte								PSL Packet 0 Syndrom Low Byte							
210	R	PDH Packet 0 Data High Byte								PDL Packet 0 Data Low Byte							

☒ Bits must be set to zero for write registers (W) and are don't care for read registers (R)

⟋ Bits not used in DMA 2280 registers, but in other devices

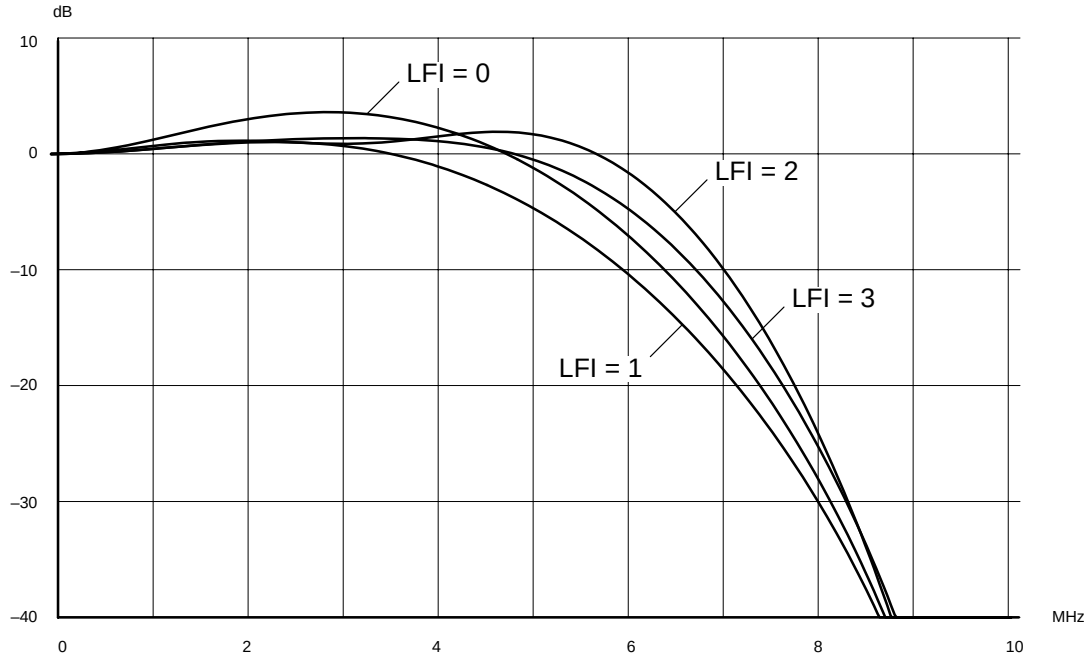
Table 4–4: VCU control and status registers, graphical overview

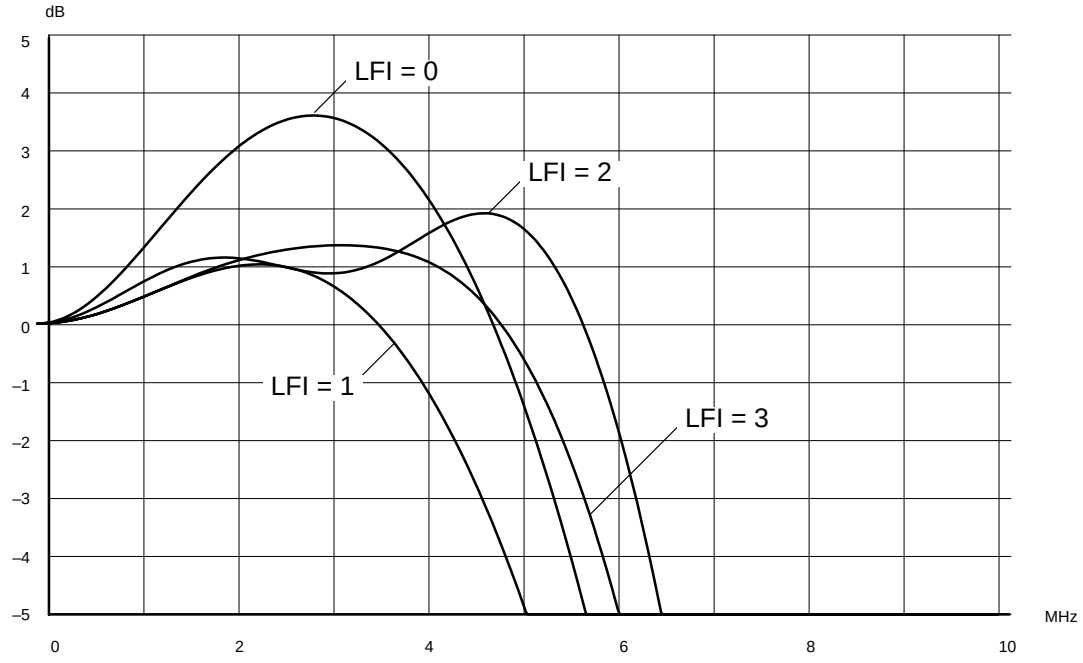
Addr. No.	Bit No. / Direct.	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
16	W	SCS SECAM Chroma Sync	NIE Noise Invert. Enable	VI2 Video Input 2	COB Code Bits			BCR Beam Current Reduction		BR Brightness							
		1	0	0	7			0		128							
17	W	CR Cutoff Voltage Red								DR White Drive Red							YDA Luma Adder
		127								127							1
18	W	CG Cutoff Voltage Green								DG White Drive Green							BLD Blank Disable
		127								127							1
19	W	CB Cutoff Voltage Blue								DB White Drive Blue							YDAS Luma Adder Shift
		127								127							0
27	W									RGBC Ext. RGB Contrast						DGD Double Gain Disable	BEN Bit Enlarg.
		0								32						1	1

☒ Bits must be set to zero for write registers (W) and are don't care for read registers (R)

Frequency Responses of the DMA 2381

a) Luminance frequency response





b) Chrominance frequency response