NS

TTL MSI

DM7590/DM8590 eight-bit parallel-in serial-out shift register

general description

The DM7590/DM8590 utilizes Series 54/74 compatible TTL circuitry to provide an eight-bit parallel-in serial-out shift register designed to operate at frequencies of 20 MHz. The device also features gating to inhibit clocking, parallel load control, and both Q and $\overline{Q}$ outputs from the last flip flop for added flexibility.

The following characteristics are applicable:

The Clock Inhibit input, when in the logical "1" state, will inhibit the Clock. It must be in the logical "0" state for clocking to occur.

There is no difference between the Clock input and the Clock Inhibit input. Their functions may be reversed if ease of layout results.

Clocking occurs on the positive-going transition of the Clock input.

Data on the D1 through D8 inputs will be entered on the negative-going transition of the Load input. This information is entered independent of the state of the Clock, Clock Inhibit, or Serial Input lines. Information on these parallel inputs may be changed while the Load line is enabled thus changing the information in the register.

The logic level applied to the Serial Input is entered into the first flip flop when the register is clocked.

logic and connection diagrams
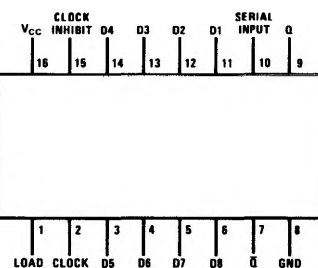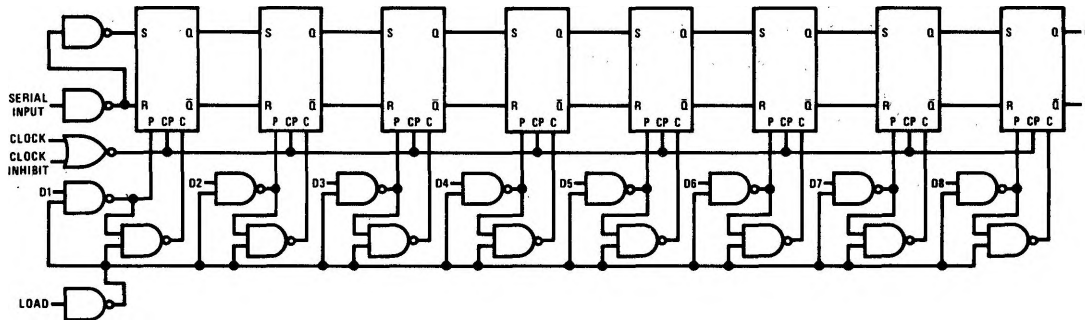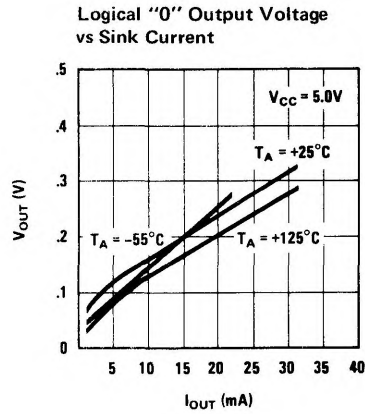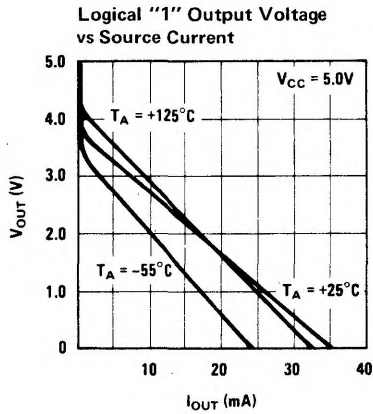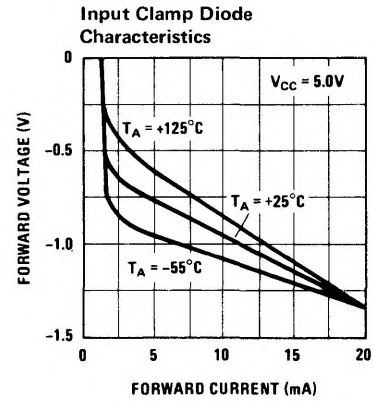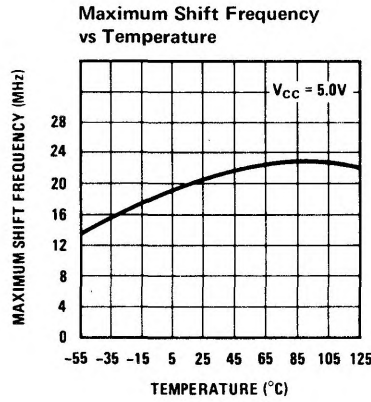
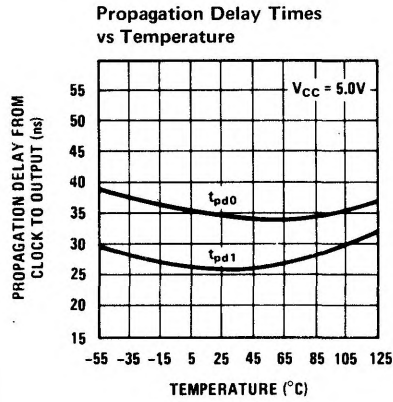# absolute maximum ratings

Supply Voltage   +7V
Input Voltage   +5.5V
Fan Out   10
Storage Temperature Range $-65^\circ C$ to $+150^\circ C$
Operating Temperature Range   DM7590 $-55^\circ C$ to $+125^\circ C$
                                DM8590 $0^\circ C$ to $+70^\circ C$

electrical characteristics (Note 1)

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		$V_{CC} = 5.0V$, $T_A = 25^\circ C$, $I_{IN} = -12\,mA$			-1.5	V
Logical "1" Input Voltage	DM7590	$V_{CC} = 4.5V$	2.0			V
	DM8590	$V_{CC} = 4.75V$				
Logical "0" Input Voltage	DM7590	$V_{CC} = 4.5V$			0.8	V
	DM8590	$V_{CC} = 4.75V$				
Logical "1" Output Voltage	DM7590	$V_{CC} = 4.5V$ $I_{OUT} = -400\,\mu A$	2.4			V
	DM8590	$V_{CC} = 4.75V$				
Logical "0" Output Voltage	DM7590	$V_{CC} = 4.5V$ $I_{OUT} = 16\,mA$			0.4	V
	DM8590	$V_{CC} = 4.75V$				
Logical "1" Input Current (All Inputs Except Load Input)	DM7590	$V_{CC} = 5.5V$ $V_{IN} = 2.4V$			40	μA
	DM8590	$V_{CC} = 5.25V$				
Logical "1" Input Current (Load Input)	DM7590	$V_{CC} = 5.5V$ $V_{IN} = 2.4V$			80	μA
	DM8590	$V_{CC} = 5.25V$				
Logical "1" Input Current	DM7590	$V_{CC} = 5.5V$ $V_{IN} = 5.5V$			1	mA
	DM8590	$V_{CC} = 5.25V$				
Logical "0" Input Current (All Inputs Except Load Input)	DM7590	$V_{CC} = 5.5V$ $V_{IN} = 0.4V$			-1.6	mA
	DM8590	$V_{CC} = 5.25V$				
Logical "0" Input Current (Load Input)	DM7590	$V_{CC} = 5.5V$ $V_{IN} = 0.4V$			-3.2	mA
	DM8590	$V_{CC} = 5.25V$				
Output Short Circuit Current	DM7590	$V_{CC} = 5.5V$ $V_{OUT} = 0V$	-20		-55	mA
	DM8590	$V_{CC} = 5.25V$	-18			
Power Supply Current	DM7590	$V_{CC} = 5.5V$		40	63	mA
	DM8590	$V_{CC} = 5.25V$				
Propagation Delay to a Logical "0" from Clock to Q or $\bar{Q}$, t_{pd0}		$V_{CC} = 5.0V$, $T_A = 25^\circ C$		35	50	ns
Propagation Delay to a Logical "1" from Clock to Q or $\bar{Q}$, t_{pd1}		$V_{CC} = 5.0V$, $T_A = 25^\circ C$		26	40	ns
Propagation Delay to a Logical "0" from D_8 to Q or $\bar{Q}$, $t_{pd0(D8)}$		$V_{CC} = 5.0V$, $T_A = 25^\circ C$		36	50	ns
Propagation Delay to a Logical "1" from D_8 to Q or $\bar{Q}$, $t_{pd1(D8)}$		$V_{CC} = 5.0V$, $T_A = 25^\circ C$		25	40	ns
Propagation Delay to a Logical "0" from Load to Q or $\bar{Q}$, $t_{pd0(load)}$		$V_{CC} = 5.0V$, $T_A = 25^\circ C$		42	60	ns
Propagation Delay to a Logical "1" from Load to Q or $\bar{Q}$, $t_{pd1(load)}$		$V_{CC} = 5.0V$, $T_A = 25^\circ C$		34	50	ns
Minimum Time That Serial Input Data Must Be Set Up Prior to Clock Pulse, $t_{set\,up\,(clock)}$		$V_{CC} = 5.0V$, $T_A = 25^\circ C$		23	40	ns
Minimum Time That Serial Input Data Must Be Held after Clock Pulse, $t_{hold\,(clock)}$		$V_{CC} = 5.0V$, $T_A = 25^\circ C$			0	ns
Minimum Time That $D_1 - D_8$ Input Data Must Be Set Up Prior to Load Pulse Termination, $t_{set\,up\,(load)}$		$V_{CC} = 5.0V$, $T_A = 25^\circ C$		10	25	ns
Minimum Time That $D_1 - D_8$ Input Data Must Be Held after Load Pulse Termination, $t_{hold\,(load)}$		$V_{CC} = 5.0V$, $T_A = 25^\circ C$			5	ns
Minimum Clock Pulse Width		$V_{CC} = 5.0V$, $T_A = 25^\circ C$		25	35	ns
Minimum Load Pulse Width		$V_{CC} = 5.0V$, $T_A = 25^\circ C$		24	35	ns
Maximum Shift Frequency		$V_{CC} = 5.0V$, $T_A = 25^\circ C$ Duty Cycle	14	20		MHz

Note 1: Unless otherwise specified, limits shown apply from $-55^\circ C$ to $+125^\circ C$ for the DM7590 and $0^\circ C$ to $+70^\circ C$ for the DM8590. Typical values apply to supply voltages of 5.0V.

DM7590/DM8590

typical performance characteristics

Propagation Delay Times vs Temperature

Maximum Shift Frequency vs Temperature

Input Clamp Diode Characteristics

Logical "1" Output Voltage vs Source Current

Logical "0" Output Voltage vs Sink Current

switching time waveforms