TTL MSI

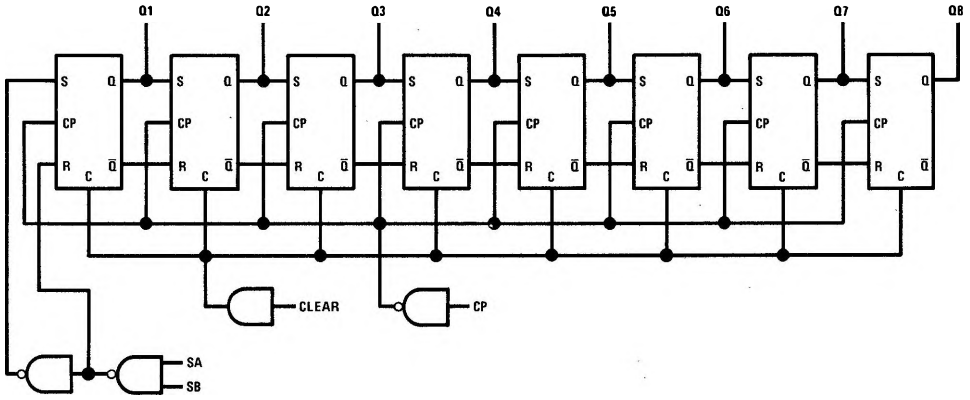
DM7570/DM8570 eight bit serial-in parallel-out shift register

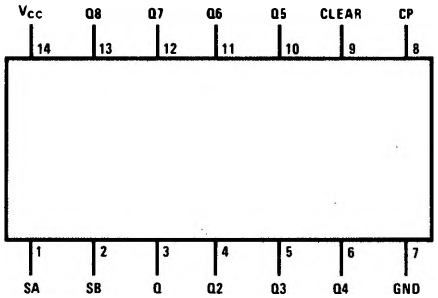
general description

The DM7570/DM8570 utilizes Series 54/74 compatible TTL circuitry to provide an eight-bit serial-in parallel-out shift register designed to operate at frequencies of 20 MHz. Other features include gated serial inputs for strobe capability and a clear input which, when taken to a logical 0, asynchronously sets all flip flops to the logical 0 state.

Because the flip flops are R-S instead of J-K, input information may be changed immediately prior to the triggering edge of the clock waveform. Logical 1 levels on SA and SB enter logical 1's into the shift register. Clocking occurs on the positive-going edge of the clock pulse.

logic and connection diagrams





absolute maximum ratings

Supply Voltage		7V
Input Voltage		5.5V
Fanout		5
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	DM7570	−55°C to +125°C
	DM8570	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)		300°C

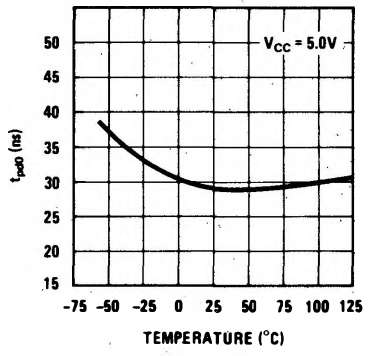
electrical characteristics (Note 1)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7570	V_{CC} = 4.5V		2.0			V
	DM8570	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM7570	V_{CC} = 4.5V				0.8	V
	DM8570	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM7570	V_{CC} = 4.5V	I_{OUT} = −200 μA	2.4			V
	DM8570	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM7570	V_{CC} = 4.5V	I_{OUT} = 8 mA			0.4	V
	DM8570	V_{CC} = 4.75V					
Logical "1" Input Current (Except Clear Input)	DM7570	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM8570	V_{CC} = 5.25V					
Logical "1" Input Current (Clear Input)	DM7570	V_{CC} = 5.5V	V_{IN} = 2.4V			80	μA
	DM8570	V_{CC} = 5.25V					
Logical "1" Input Current	DM7570	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM8570	V_{CC} = 5.25V					
Logical "0" Input Current (Except Clear Input)	DM7570	V_{CC} = 5.5V	V_{IN} = 0.4V			1.6	mA
	DM8570	V_{CC} = 5.25V					
Logical "0" Input Current (Clear Input)	DM7570	V_{CC} = 5.5V	V_{IN} = 0.4V			3.2	mA
	DM8570	V_{CC} = 5.25V					
Output Short Circuit Current (Note 2)	DM7570	V_{CC} = 5.5V	V_{OUT} = 0V	10		27.5	mA
	DM8570	V_{CC} = 5.25V		9			
Power Supply Current	DM7570	V_{CC} = 5.5V			36	54	mA
	DM8570	V_{CC} = 5.25V					
Maximum Clock Frequency		V_{CC} = 5.0V, 25°C, 50% Duty Cycle		14	20		mHz
Propagation Delay to a Logical "0" from Clock to Output, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF		10	28	40	ns
Propagation Delay to a Logical "1" from Clock to Output, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF		10	28	40	ns
Propagation Delay to a Logical "0" from Clear to Output		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF			34	50	ns
Minimum Clock Pulse Width		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF			25	45	ns
Minimum Clear Pulse Width		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF			30	45	ns
Minimum Time that $S_A \cdot S_B$ Data Must be Set-up Prior to Clock Pulse, $t_{set\text{-}up}$		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF, Clock Pulse Width = 50 ns			15	30	ns
Minimum Time that $S_A \cdot S_B$ Data Must be Held After Clock Pulse, t_{hold}		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF, Clock Pulse Width = 50 ns			−15	0	ns

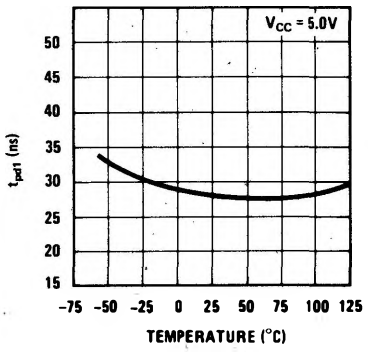
Note 1: Unless otherwise specified, limits shown apply from −55°C to +125°C for the DM7570 and 0°C to +70°C for the DM8570. Typical values apply to supply voltages of 5.0V and 25°C.
Note 2: Only one output should be shorted at a time.

typical performance characteristics

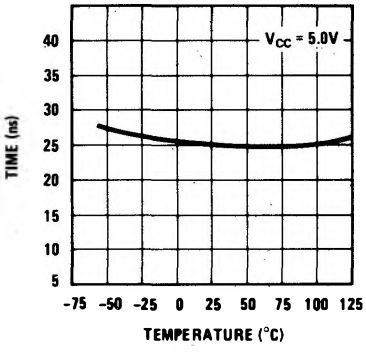
Transition Time to a Logical "0" (t_{pd0}) from Clock to Output vs Temperature



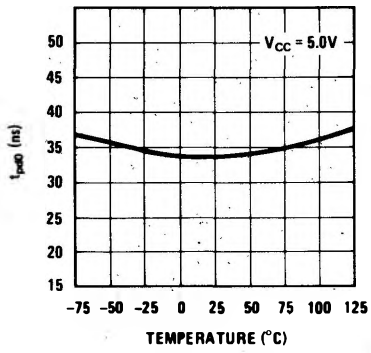
Transition Time to a Logical "1" (t_{pd1}) from Clock to Output vs Temperature



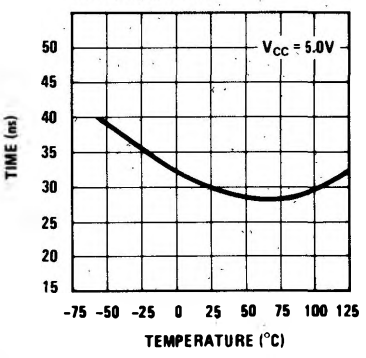
Minimum Clock Pulse Width vs Temperature



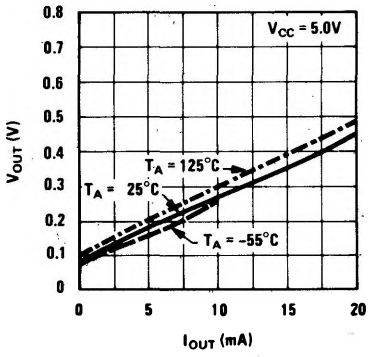
Transition Time to a Logical "0" (t_{pd0}) from Clear to Output vs Temperature



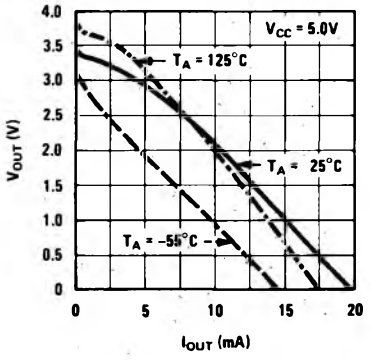
Minimum Clear Pulse Width vs Temperature



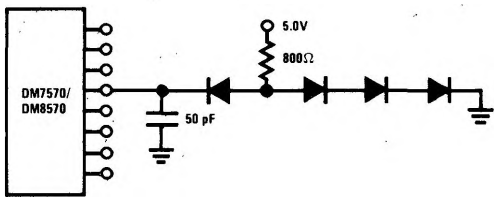
Logical "0" Output Voltage vs Sink Current



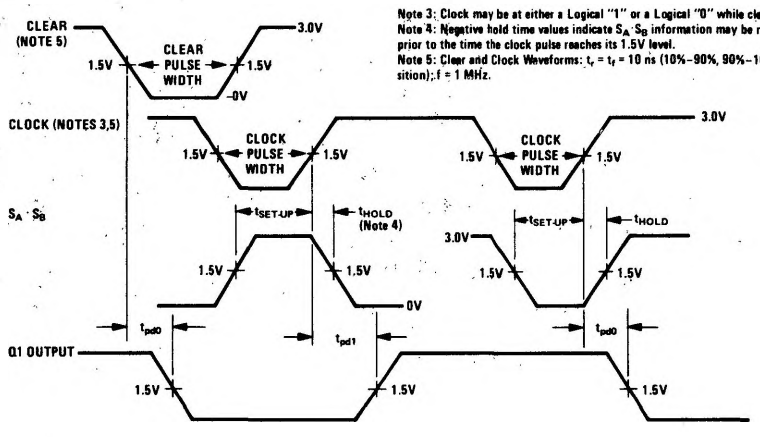
Logical "1" Output Voltage vs Source Current



ac test circuit



switching time waveforms



Note 3: Clock may be at either a Logical "1" or a Logical "0" while clearing.
Note 4: Negative hold time values indicate $S_A \cdot S_B$ information may be released prior to the time the clock pulse reaches its 1.5V level.
Note 5: Clear and Clock Waveforms: $t_r = t_f = 10$ ns (10%–90%, 90%–10% transition); f = 1 MHz.