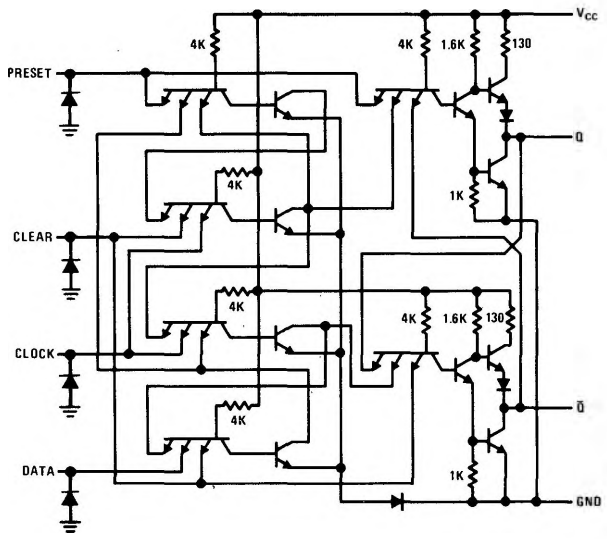
Flip Flops, Series 54/74

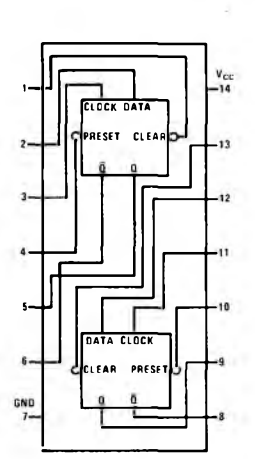
DM5474/DM7474 (SN5474/SN7474) dual D flip flops

general description

The DM5474/DM7474 dual D flip flops are designed for use where the flexibility of two inputs, such as on a JK or an RS flip flop, are not required. If only a single input (two logic combinations) can be utilized, then an extra input is superfluous. The DM5474/DM7474 have only a single DATA input. The logical level applied to this DATA input is transferred to the Q output when the clock pulse voltage rises to a logical 1. It is only necessary to set-up information on the DATA input several nanoseconds before the clock pulse voltage rises; likewise it is only necessary to hold that information several nanoseconds after the clock pulse voltage reaches the logical 1 level. DATA information is then free to change in preparation for the next clock pulse. Since only one pin is used for data entry, fully asynchronous (both PRESET and CLEAR) capability can be provided in a 14 pin dual-in-line package.

schematic and connection diagrams

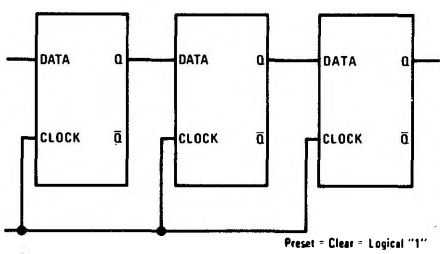




Note: A logical 0 on CLEAR sets Q to a logical 0.
A logical 0 on PRESET sets Q to a logical 1.

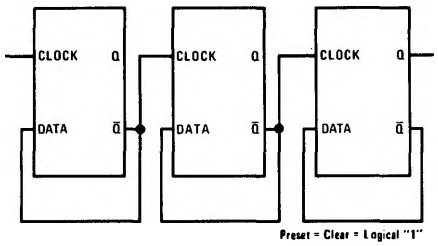
typical applications

shift register



Preset = Clear = Logical "1"

ripple counter (divide-by-2^n)



Preset = Clear = Logical "1"

absolute maximum ratings

Supply Voltage		+7V
Input Voltage		5.5V
Fan Out		10
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	DM5474	−55°C to +125°C
	DM7474	0°C to +70°C
Lead Temperature (soldering, 10 sec)		300°C

electrical characteristics (Note 1)

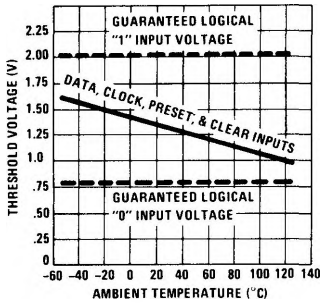
PARAMETER		CONDITION			MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5.0V, I_{OUT} = −12 mA, T_A = 25°C					−1.5	V
Logical "1" Input Voltage	DM5474	V_{CC} = 4.5V			2.0			V
	DM7474	V_{CC} = 4.75V						
Logical "0" Input Voltage	DM5474	V_{CC} = 4.5V					0.80	V
	DM7474	V_{CC} = 4.75V						
Logical "1" Output Voltage	DM5474	V_{CC} = 4.5V	I_{OUT} = −400 μA		2.4	3.3		V
	DM7474	V_{CC} = 4.75V						
Logical "0" Output Voltage	DM5474	V_{CC} = 4.5V	I_{OUT} = 16.0 mA			0.15		V
	DM7474	V_{CC} = 4.75V						
Logical "0" Input Current	DM5474	V_{CC} = 5.5V	V_{IN} = 0.40V	Data or Preset		−1.0	−1.6	mA
	DM7474	V_{CC} = 5.25V		Clear or Clock		−2.0	−3.2	mA
Logical "1" Input Current	DM5474	V_{CC} = 5.5V	V_{IN} = 2.4V	Data or Preset			40.0	μV
	DM7474	V_{CC} = 5.25V		Clear or Clock			80.0	μV
Logical "1" Input Current	DM5474	V_{CC} = 5.5V	V_{IN} = 5.5V				1.0	mA
	DM7474	V_{CC} = 5.25V						
Output Short Current (Note 2)	DM5474	V_{CC} = 5.5V	V_{OUT} = 0V		−20.0		−55.0	mA
	DM7474	V_{CC} = 5.25V			−18.0			
Power Supply Current (each flip-flop)		V_{CC} = 5.0V, V_{IN} = 5.0V				8.2	13.0	mA
Maximum Clock Frequency		V_{CC} = 5.0V, T_A = 25°C	C = 50 pF		15.0	25.0		MHz
Propagation Delay Time to a Logical "0" from Clock — t_{pd0}		V_{CC} = 5.0V, T_A = 25°C	C = 50 pF		13.0	22.0	45.0	ns
Propagation Delay Time to a Logical "1" from Clock — t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	C = 50 pF		10.0	16.0	30.0	ns
Propagation Delay Time to a Logical "0" from Clear, or Preset — t_{pd0}		V_{CC} = 5.0V, T_A = 25°C					40.0	ns
Propagation Delay Time to a Logical "1" from Clear, or Preset — t_{pd1}		V_{CC} = 5.0V, T_A = 25°C					25.0	ns
Time Prior to Clock Pulse that Data Information Must be Present — $t_{set\ up}$		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF		Logical "1"		15.0	20.0	ns
				Logical "0"		15.0	20.0	ns
Time After Clock Pulse that Data Information Must be Held — t_{hold}		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF		Logical "1"		−5.0	0	ns
				Logical "0"		0.6	3.0	ns

Note 1: Min/max limits apply across the guaranteed operating temperature range of −55°C to +125°C for DM5474 and 0°C to 70°C for DM7474 unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

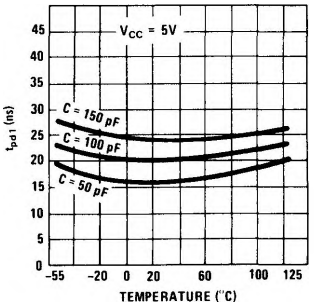
Note 2: Only one output may be shorted at a time.

typical performance characteristics

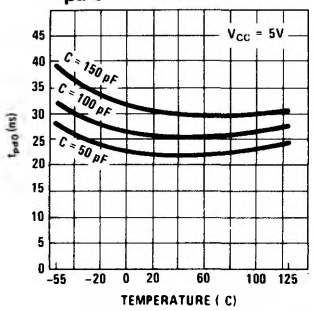
Threshold Voltage vs Temperature*



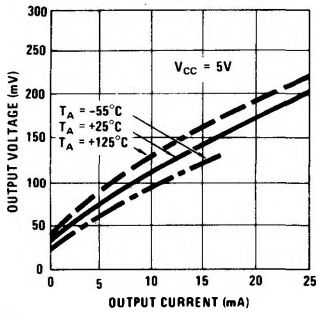
Transition Time to a Logical "1" ($t_{pd\ 1}$) vs Temperature*



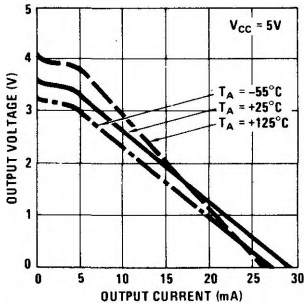
Transition Time to a Logical "0" ($t_{pd\ 0}$) vs Temperature*



Logical "0" Output Voltage vs Sink Current

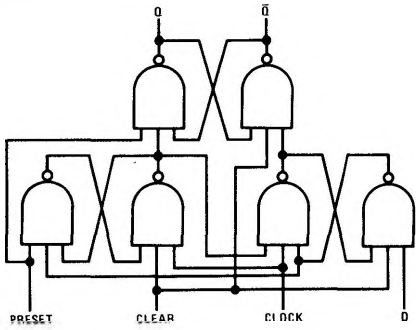


Logical "1" Output Voltage vs Source Current

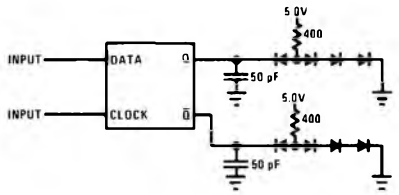


*Note: Curves apply to DM7474 across 0°C to +70°C range only.

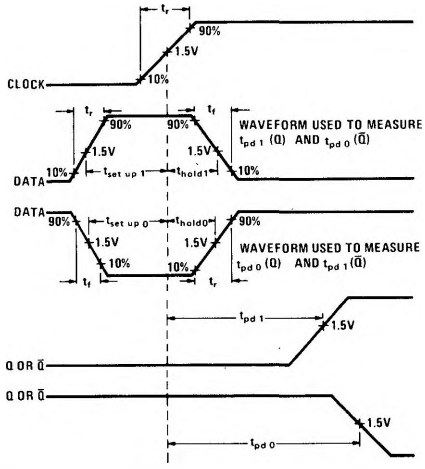
block diagram (each flip flop)



ac test circuit



switching time waveforms



Note: No maximum rise and fall times are imposed upon the clock voltage. However very slow transitions which allow an input to remain in the threshold region can cause noise problems.