

## Features

- ANSI TIA/EIA-644-1995-compliant
- Designed for data rates to $\geq 650 \mathrm{Mbps}=(325 \mathrm{MHz})$
- Single $2 \times 2$ with high-drive output drivers
—Low-voltage Differential Signaling with output
voltages of $\pm 350 \mathrm{mV}$ into 50 -ohm load version (Bus LVDS)
- Single 3.3V supply
- Accepts $\pm 350-\mathrm{mV}$ differential inputs
- Output drivers are high impedance when disabled or when VDD $\leq 1.5 \mathrm{~V}$
- 28-pin SSOP/TSSOP packages
- Industrial version available


## Description

The Cypress CY2LL8423 are differential line drivers and receivers that utilize low-voltage differential signaling (LVDS) to achieve signaling rates of 650 Mbps . The receiver outputs can be switched to either or both drivers through the multiplexer control signals S2/S3. This provides flexibility in application for either a splitter or router configuration with a single device.

The Cypress CY2LL8423 are configured as a dual 2-channel repeater/Mux. The LVDS standard provides a minimum differential output voltage of 247 mV into a 50 -ohm load and receipt of as little as $100-\mathrm{mV}$ signals with up to 1V of DC offset between transmitter and receiver.
A doubly-terminated Bus LVDS line enables multipoint configurations.
Designed for both point-to-point based-B and multipoint data transmission over controlled impedance lines.

## Block Diagram



## Pin Configuration



## Pin Description

| Pin Number | Pin Name | Description |
| :---: | :---: | :--- |
| 15,22 | GND | Ground |
| 2,1 | $1 \mathrm{~A}, 1 \mathrm{~B}$ | Differential Input Channel 1 |
| 3 | S0 | Function Select Channel 1\&2 |
| 4 | 1 DE | Data Enable Channel 1 |
| 5 | S1 | Function Select Channel 1\& 2 |
| 6,7 | $2 \mathrm{~A}, 2 \mathrm{~B}$ | Differential Input Channel 2 |
| 21,28 | VDD | Power Supply |
| 8,9 | $3 \mathrm{~A}, 3 \mathrm{~B}$ | Differential Input Channel 3 |
| 10 | S 2 | Function Select Channel 3 \& 4 |
| 11 | 3 DE | Data Enable Channel 3 |
| 12 | $\mathrm{S3}$ | Function Select Channel 3 \& 4 |
| 13,14 | $4 \mathrm{~A}, 4 \mathrm{~B}$ | Differential Input Channel 4 |
| 17,16 | $4 \mathrm{Y}, 4 \mathrm{Z}$ | Differential Output Channel 4 |
| 18 | 4 DE | Data Enable Channel 4 |
| 20,19 | $3 \mathrm{Y}, 3 \mathrm{Z}$ | Differential Output Channel 3 |
| 23,24 | $2 \mathrm{Y}, 2 \mathrm{Z}$ | Differential Output Channel 2 |
| 25 | 2 DE | Data Enable Channel 2 |
| 27,26 | $1 \mathrm{Y}, 1 \mathrm{Z}$ | Differential Output Channel 1 |

Table 1. Mux Function Table

| Input |  | Output |  | Function |
| :---: | :---: | :---: | :---: | :---: |
| $\mathbf{S 0}$ | $\mathbf{S 1}$ | $\mathbf{1 Y / 1 Z}$ | $\mathbf{2 Y / 2 Z}$ |  |
| 0 | 0 | $1 \mathrm{~A} / 1 \mathrm{~B}$ | $1 \mathrm{~A} / 1 \mathrm{~B}$ | Splitter A |
| 1 | 0 | $2 \mathrm{~A} / 2 \mathrm{~B}$ | $2 \mathrm{~A} / 2 \mathrm{~B}$ | Splitter B |
| 0 | 1 | $1 \mathrm{~A} / 1 \mathrm{~B}$ | $2 \mathrm{~A} / 2 \mathrm{~B}$ | Pass Thru Router |
| 1 | 1 | $2 \mathrm{~A} / 2 \mathrm{~B}$ | $\mathbf{1 A} / 1 \mathrm{~B}$ | Cross Point Router |
| $\mathbf{S 2}$ | $\mathbf{S 3}$ | $\mathbf{3 Y / 3 Z}$ | $\mathbf{4 Y / 4 Z}$ |  |
| 0 | 0 | $3 \mathrm{~A} / 3 \mathrm{~B}$ | $3 \mathrm{~A} / 3 \mathrm{~B}$ | Splitter A |
| 1 | 0 | $4 \mathrm{~A} / 4 \mathrm{~B}$ | $4 \mathrm{~A} / 4 \mathrm{~B}$ | Splitter B |
| 0 | 1 | $3 \mathrm{~A} / 3 \mathrm{~B}$ | $4 \mathrm{~A} / 4 \mathrm{~B}$ | Pass Thru Router |
| 1 | 1 | $4 \mathrm{~A} / 4 \mathrm{~B}$ | $3 \mathrm{~A} / 3 \mathrm{~B}$ | Cross Point Router |

Table 2. Absolute Maximum Rating Over Operating Free-Air Temperature ${ }^{[1]}$

| Supply Voltage Range, $\mathrm{V}_{\mathrm{DD}}(1)$ | -0.5 V to 4 V |
| :--- | :--- |
| Voltage Range (DE,S0,S1) | -0.5 V to 6.0 V |
| Input Voltage Range, VIN (A or B) | -0.5 V to $\mathrm{V}_{\mathrm{DD}}+0.5 \mathrm{~V}$ |
| ESD (All pins) | Class $3, \mathrm{~A}: 2 \mathrm{KV}, \mathrm{B}: 500 \mathrm{~V}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $150^{\circ} \mathrm{C}$ |

## Note:

1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 3. Recommended Operating Conditions ${ }^{[2]}$

| Parameter | Description |  | Min. | Typ. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| V ${ }^{\text {DD }}$ | Supply Voltage |  | 3 | 3.3 | 3.6 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage | (S0,S1,1DE,2DE) (S2,S3,3DE,4DE) | 2 |  |  |  |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage | $\begin{aligned} & \text { (S0,S1,1DE,2DE) } \\ & \text { (S2,S3,3DE,4DE) } \end{aligned}$ |  |  | 0.8 |  |
| $\mathrm{V}_{\text {ID }}$ | Magnitude of Differential Input Voltage |  | 0.1 |  | 0.6 |  |
| $\mathrm{V}_{\text {IC }}$ | Common Mode Input Voltage |  | $\mathrm{V}_{\mathrm{ID}} / 2$ |  | $2.4-\left(\mathrm{V}_{\mathrm{ID}} / 2\right)$ |  |
| $\mathrm{T}_{\mathrm{A}}$ | Operating Free Air Temperature | Industrial | -40 |  | 85 | ${ }^{\circ} \mathrm{C}$ |
|  |  | Commercial | 0 |  | 70 |  |

Table 4. Receiver Electrical Characteristics Over Recommended Operating Conditions

| Parameter | Description | Condition | Min. | Typ. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {ITH }+}$ | Positive-going Differential Input Voltage Threshold | $\mathrm{V}_{\mathrm{CM}}=1.2 \mathrm{~V}$ |  |  | 100 | mV |
| $\mathrm{V}_{\text {ITH- }}$ | Negative-going Differential Input Voltage Threshold | $\mathrm{V}_{\mathrm{CM}}=1.2 \mathrm{~V}$ | -100 |  |  | mV |
| 1 | Input Current (A Inputs) [FAIL SAFE] | $\mathrm{V}_{1}=0 \mathrm{~V}$ | -0.5 |  | -10 | $\mu \mathrm{A}$ |
|  |  | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  | -10 | $\mu \mathrm{A}$ |
| 1 | Input Current (B Inputs) [FAIL SAFE] | $\mathrm{V}_{1}=0.8 \mathrm{~V}$ | 0.5 |  | 10 | $\mu \mathrm{A}$ |
|  |  | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  | 10 | $\mu \mathrm{A}$ |
| 1 (Off) | Power Off Current (A or B Inputs) | $\mathrm{V}_{\mathrm{DD}}=0 \mathrm{~V}$ |  | 0.1 | 10 | $\mu \mathrm{A}$ |

Table 5. Receiver Electrical Characteristics Over Recommended Operating Conditions

| Parameter | Description | Condition |  | Min. | Typ. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{O D}$ | Differential Output Voltage Swing | $\mathrm{RL}=50 \mathrm{Ohm}$ | See Figure 3 | 247 | 340 | 454 | mV |
| $\sim \mathrm{V}_{\text {OD }}$ | Change in Differential Output Voltage Swing between Logic States |  |  | -50 |  | 50 | mV |
| $\mathrm{V}_{\mathrm{OC}}$ (SS) | Steady State Common-mode Output Voltage |  | See Figure 4 | 1.125 |  | 1.375 | V |
| $\sim \mathrm{V}_{\text {OC }}(\mathrm{SS})$ | Change in Steady State Common-mode Output between Logic States |  |  | -50 | 3 | 50 | mV |
| $\mathrm{V}_{\mathrm{OC}}(\mathrm{PP})$ | Peak-to-Peak Common-mode Output Voltage |  |  |  |  | 150 | mV |
| $\mathrm{I}_{\mathrm{CC}}$ | Supply Current | No load |  |  | 20 | 28 | mA |
|  |  | RL = 50 ohm@3.3V Fin $=75 \mathrm{MHz}$ |  |  | 42 | 54 | mA |
|  |  | Both channels disabled |  |  | 16 | 24 | mA |
| $\mathrm{I}_{\mathrm{IH}}$ | High-Level Input Current | $\begin{aligned} & \text { (S0,S1,1DE,2DE) } \\ & \text { (S2,S3,3DE,4DE) } \end{aligned}$ | $\mathrm{V}_{\mathrm{IH}}=5 \mathrm{~V}$ |  | 15 |  | $\mu \mathrm{A}$ |
| IL | Low-Level Input Current | $\begin{aligned} & \text { (S0,S1,1DE,2DE) } \\ & \text { (S2,S3,3DE,4DE) } \end{aligned}$ | $\mathrm{V}_{\mathrm{IL}}=0.8 \mathrm{~V}$ |  | 5 |  | $\mu \mathrm{A}$ |
| los | Short Circuit Current |  | $\mathrm{V}_{\mathrm{OY}}$ or $\mathrm{V}_{0 \mathrm{O}}=0 \mathrm{~V}$ |  |  | 20 | mA |
|  |  |  | $\mathrm{V}_{\mathrm{OD}}=0 \mathrm{~V}$ |  |  | 20 |  |
| $\mathrm{I}_{\mathrm{OZ}}$ | High Impedance Output Current |  | $\mathrm{V}_{\mathrm{OD}}=600 \mathrm{mV}$ |  | 0.1 | 1 | $\mu \mathrm{A}$ |
|  |  |  | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ or $\mathrm{V}_{\mathrm{DD}}$ |  | 0.1 | 1 |  |
| IO(OFF) | Power-Off Output Current |  | $\mathrm{V}_{\mathrm{DD}}=0 \mathrm{~V}, \mathrm{~V} 0=3.6 \mathrm{~V}$ |  | 0.1 | 10 | $\mu \mathrm{A}$ |
| $\mathrm{C}_{\text {in }}$ | Input Capacitance |  | $\begin{aligned} & 1 \mathrm{~A}, 1 \mathrm{~B}, 2 \mathrm{~A}, 2 \mathrm{~B}, 3 \mathrm{~A}, \\ & 3 \mathrm{~B}, 4 \mathrm{~A}, 4 \mathrm{~B} \end{aligned}$ |  | 3 |  | pF |
|  | Control Input Capacitance |  | $\begin{aligned} & \text { (S0,S1,1DE,2DE) } \\ & \text { (S2,S3,3DE,4DE) } \end{aligned}$ |  | 6 |  | pF |

Note:
2. Multiple supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

Table 6. Differential Receiver to Driver Switching Characteristics Over Recommended Operating Conditions ${ }^{[3,4]}$

| Parameter | Description | Test Conditions | Min. | Typ. ${ }^{[3]}$ | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{T}_{\text {PLH }}$ | Differential Propagation delay, low to high | $\mathrm{CL}=10 \mathrm{pF}$ (see Figure 5 and Figure 6) |  | 4 | 6 | ns |
| $\mathrm{T}_{\text {PHL }}$ | Differential Propagation delay, high to low |  |  | 4 | 6 | ns |
| $\mathrm{T}_{\text {sk(p) }}$ | Pulse Skew ( $\mathrm{T}_{\mathrm{PHL}}-\mathrm{T}_{\mathrm{PLH}}$ ) |  |  | 0.2 |  | ns |
| $\mathrm{T}_{\mathrm{r}}$ | Transition Low to High |  |  |  | 700 | ps |
| $\mathrm{T}_{\mathrm{f}}$ | Transition High to Low |  |  |  | 700 | ps |
| $\mathrm{T}_{\mathrm{PHZ}}$ | Propagation delay, high level to high impedance output | (see <br> Figure 6) |  | 4 | 10 | ns |
| $\mathrm{T}_{\text {PLZ }}$ | Propagation delay, low level to high impedance output |  |  | 4.3 | 10 | ns |
| $\mathrm{T}_{\text {PZH }}$ | Propagation delay, high impedance to high level output |  |  | 3 | 10 | ns |
| $\mathrm{T}_{\text {PZL }}$ | Propagation delay, high impedance to low level output |  |  | 2 | 10 | ns |
| TPHL_skR1_Dx | Channel to Channel skew-receiver 1 to Any mux related drivers |  |  | 95 |  | ps |
| TPLH_skR1_Dx | Channel to Channel skew-receiver 1 to Any mux related drivers |  |  | 95 |  | ps |
| TPPHL_skR2_Dx | Channel to Channel skew-receiver 2 to Any mux related drivers |  |  | 95 |  | ps |
| TPLH_skR2_Dx | Channel to Channel skew-receiver 2 to Any mux related drivers |  |  | 95 |  | ps |
| TPHL_skR3_Dx | Channel to Channel skew-receiver 3 to Any mux related drivers |  |  | 95 |  | ps |
| TPLH_skR3_Dx | Channel to Channel skew-receiver 3 to Any mux related drivers |  |  | 95 |  | ps |
| TPHL_skR4_Dx | Channel to Channel skew-receiver 4 to Any mux related drivers |  |  | 95 |  | ps |
| TPLH_skR4_Dx | Channel to Channel skew-receiver 4 to Any mux related drivers |  |  | 95 |  | ps |



Figure 1. Dual-2 Channel Cross Point Switch/Mux

## Notes:

3. All typical values are measured at $25^{\circ} \mathrm{C}$ with a 3.3 V supply.
4. These parameters are measured over supply voltage and temperature ranges recommended for the device.




Figure 2. Dynamic IDD Diagrams


Figure 3. Test Circuit \& Voltage Definitions for the Differential Output Signal ${ }^{[5,6,7]}$


Figure 4. Test Circuit \& Voltage Definitions for the Driver Common-Mode Output Voltage ${ }^{[5,6,7,8]}$

Notes:
5. All input pulses are supplied by a frequency generator with the following characteristics: $\mathrm{t}_{\mathrm{R}}$ and $\mathrm{t}_{\mathrm{F}} \leq 1 \mathrm{~ns}$; Pulse rep rate $=50 \mathrm{Mpps} ; \mathrm{Pulse}$ width $=10 \pm 0.2 \mathrm{~ns}$.
6. $R L=100$ Ohm.
7. CL includes instrumentation and fixture capacitance within 6 mm of the DUT.
8. VOC measurement requires equipment with a $3-\mathrm{dB}$ bandwith of at least 300 MHz


Figure 5. Differential Receiver to Driver Propagation Delay and Driver Transition Time ${ }^{[5,9,10]}$


Figure 6. Test Circuit and Voltage Definitions for the Driver Common-Mode Output Voltage ${ }^{[5,9]}$

## Application Engineering



Figure 7. Termination Scheme for $\mathbf{1 0 0}-\mathrm{Ohm}$ External Termination


Figure 8. Termination Scheme for 100-Ohm Self Termination Interface Chip

Typical Characteristics @ $\mathrm{V}_{\mathrm{DD}}=3.3 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$


Figure 9. VOH vs 10 H


Figure 10. VOL vs IOL

## Notes:

9. $\mathrm{RL}=100 \mathrm{Ohm} \pm 1 \%$,
10. Point to Point: RL $=100$ Ohm $\pm 1 \% \mathrm{CL} 3 \mathrm{pF}$.

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Table 7. Technical Notes on STD Drive (LL842, A, and D) vs. High Drive (LL8423, B, and C

|  | A | B | C | D | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| VOX | 1.2 | 1.2 | 1.2 | 1.2 | V |
| DC Offset | 1.0 | 1.0 | 1.0 | 1.0 | V |
| VOD Min | 0.25 | 0.5 | 0.25 | 0.125 | V |
| VOD Max | 0.45 | 0.9 | 0.45 | 0.225 | V |
| T/Rise | 1.4 | 1.4 | 0.6 | 0.6 | ns |
| T/Fall | 1.4 | 1.4 | 0.6 | 0.6 | ns |

## Standard Drive

 Current drive of $\mathbf{1 i}$

Hi Drive
Current drive of 2i


Figure 11.

## Ordering Information

| Part Number | Package Type | Product Flow |
| :--- | :--- | :--- |
| CY2LL8423ZI | 28-pin TSSOP | Industrial, $-40^{\circ}$ to $85^{\circ} \mathrm{C}$ |
| CY2LL8423ZIT | 28-pin TSSOP - Tape and Reel | Industrial, $-40^{\circ}$ to $85^{\circ} \mathrm{C}$ |
| CY2LL8423ZC | 28-pin TSSOP | Commercial, $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ |
| CY2LL8423ZCT | 28-pin TSSOP - Tape and Reel | Commercial, $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ |
| CY2LL8423OI | 28 -pin SSOP | Industrial, $-40^{\circ}$ to $85^{\circ} \mathrm{C}$ |
| CY2LL8423OIT | 28-pin SSOP - Tape and Reel | Industrial, $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ |
| CY2LL8423OC | 28 -pin SSOP | Commercial, $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ |
| CY2LL8423OCT | 28 -pin SSOP - Tape and Reel | Commercial, $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ |

Note:
11. See Figure 11.

## Package Drawings and Dimensions

28-lead ( 5.3 mm) Shrunk Small Outline Packaqe 028


## 28-lead Thin Shrunk Small Outline Package (4.40-mm Body) Z29


dIMENSIGNS IN MILLIMETERS. $\frac{\text { MIN. }}{\text { MAX }}$


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ComLink ${ }^{\text {TM }}$ Series CY2LL8423

## Document History Page

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| :---: | :---: | :---: | :---: | :---: |
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 116744 | 07/08/02 | HWT | New Data Sheet |
| *A | 122750 | 12/15/02 | RBI | Added power-up requirements to operating conditions information |
| *B | 124088 | 02/06/03 | RGL | Changed the package drawing and dimension from Z28 to Z29 |

