## CD4066BM/CD4066BC Quad Bilateral Switch

## General Description

The CD4066BM/CD4066BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4016BM/CD4016BC, but has a much lower "ON" resistance, and "ON" resistance is relatively constant over the input-signal range.

## Features

- Wide supply voltage range
- High noise immunity
- Wide range of digital and analog switching
■ "ON" resistance for 15 V operation
$80 \Omega$
- Matched "ON" resistance

3 V to 15 V
$0.45 \mathrm{~V}_{\mathrm{DD}}$ (typ.)
$\pm 7.5$ VPEAK over 15 V signal input

- "ON" resistance flat over peak-to-peak signal range
- High "ON" ${ }^{\prime \prime}$ "OFF' output voltage ratio
- High degree linearity

65 dB (typ.)
@ $\mathrm{f}_{\mathrm{is}}=10 \mathrm{kHz}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$
$0.1 \%$ distortion (typ.) $@ \mathfrak{f}_{\text {is }}=1 \mathrm{kHz}, \mathrm{V}_{\text {is }}=5 \mathrm{~V}_{\mathrm{p} . \mathrm{p}}$, $V_{D D}-V_{S S}=10 \mathrm{~V}, R_{L}=10 \mathrm{k} \Omega$

## Schematic and Connection Diagrams



TOP VIEW

Absolute Maximum Ratings
(Notes 1 and 2)
$V_{D D}$ Supply Voltage
VIN Input Voltage
$T_{S}$ Storage Temperature Range
$P_{D}$ Package Dissipation
$T_{L}$ Lead Temperature (Soldering, 10 seconds)
-0.5 V to +18 V
-0.5 V to $\mathrm{V}_{\mathrm{DD}}+0.5 \mathrm{~V}$ $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ 500 mW $300^{\circ} \mathrm{C}$
(Note 2)
$V_{\text {DD }}$ Supply Voltage
3 V to 15 V $O V$ to $V_{D D}$
$-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$

DC Electrical Characteristics CD4066BM (Note 2)

| Parameter |  | Conditions | $-55^{\circ} \mathrm{C}$ |  | $25^{\circ} \mathrm{C}$ |  |  | $125{ }^{\circ} \mathrm{C}$ |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max | Min | Typ | Max | Min | Max |  |
|  | Quiescent Device Current |  | $V_{D D}=5 \mathrm{~V}$ |  | 0.25 |  | 0.01 | 0.25 |  | 7.5 | $\mu \mathrm{A}$ |
|  |  | $V_{D D}=10 \mathrm{~V}$ |  | 0.5 |  | 0.01 | 0.5 |  | 15 | $\mu \mathrm{A}$ |
|  |  | $V_{D D}=15 \mathrm{~V}$ |  | 1.0 |  | 0.01 | 1.0 |  | 30 | $\mu \mathrm{A}$ |

Signal Inputs and Outputs


DC Electrical Characteristics CD4066BC (Note 2)


DC Electrical Characteristics (Cont'd.) CD4066BC (Note 2)

| Parameter | Conditions | $-40^{\circ} \mathrm{C}$ |  | $25^{\circ} \mathrm{C}$ |  |  | $85^{\circ} \mathrm{C}$ |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max | Min | Typ | Max | Min | Max |  |
| Signal Inputs and Outputs |  |  |  |  |  |  |  |  |  |
| RON "ON" Resistance | $\begin{aligned} & R_{L}=10 \mathrm{k} \Omega \text { to } \frac{V_{D D}-V_{S S}}{2} \\ & V_{C}=V_{D D}, V_{S S} \text { to } V_{D D} \end{aligned}$ |  |  |  |  |  |  |  |  |
|  | $V_{D D}=5 \mathrm{~V}$ |  | 2000 |  | 270 | 2500 |  | 3200 | $\Omega$ |
|  | $V_{D D}=10 \mathrm{~V}$ |  | 450 |  | 120 | 500 |  | 520 | $\Omega$ |
|  | $V_{D D}=15 \mathrm{~V}$ |  | 250 |  | 80 | 280 |  | 300 | $\Omega$ |
| $\triangle R_{O N} \quad \triangle$ "ON" Resistance Between Any 2 of 4 Switches | $R_{L}=10 \mathrm{k} \Omega \text { to } \frac{V_{D D}-V_{S S}}{2}$ |  |  |  |  |  |  |  |  |
|  | $V_{C C}=V_{D D}, V_{I S}=V_{S S} \text { to } V_{D D}$ |  |  |  |  |  |  |  |  |
|  | $V_{D D}=10 \mathrm{~V}$ |  |  |  | 10 |  |  |  | $\Omega$ |
|  | $V_{D D}=15 \mathrm{~V}$ |  |  |  | 5 |  |  |  | $\Omega$ |
| IIS Input or Output Leakage Switch "OFF" | $V_{C}=0$ |  | $\pm 50$ |  | $\pm 0.1$ | $\pm 50$ |  | $\pm 200$ | nA |

Control Inputs

| VILC Low Level Input Voltage | $\begin{aligned} & V_{I S}=V_{S S} \text { and } V_{D D} \\ & V_{O S}=V_{D D} \text { and } V_{S S} \\ & I_{I S}= \pm 10 \mu \mathrm{~A} \\ & V_{D D}=5 \mathrm{~V} \\ & V_{D D}=10 \mathrm{~V} \\ & V_{D D}=15 \mathrm{~V} \end{aligned}$ | 1.5 3.0 4.0 |  | $\begin{aligned} & 2.25 \\ & 4.5 \\ & 6.75 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 3.0 \\ & 4.0 \end{aligned}$ | 1.5 3.0 4.0 | $V$ $v$ $v$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| VIHC High Level Input Voltage | $\begin{aligned} & V_{D D}=5 \mathrm{~V} \\ & V_{D D}=10 \mathrm{~V} \text { (See note 6) } \\ & V_{D D}=15 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 7.0 \\ & 11.0 \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 7.0 \\ & 11.0 \end{aligned}$ | $\begin{aligned} & 2.75 \\ & 5.5 \\ & 8.25 \end{aligned}$ |  | $\begin{aligned} & 3.5 \\ & 7.0 \\ & 11.0 \end{aligned}$ | $\begin{aligned} & v \\ & v \\ & v \end{aligned}$ |
| IIN Input Current | $\begin{aligned} & V_{D D}-V_{S S}=15 \mathrm{~V} \\ & \mathrm{~V}_{D D} \geqslant \mathrm{~V}_{I S} \geqslant V_{S S} \\ & \mathrm{~V}_{\mathrm{DD}} \geqslant \mathrm{~V}_{\mathrm{C}} \geqslant \mathrm{~V}_{S S} \end{aligned}$ | $\pm 0.3$ |  | $\pm 10^{-5}$ | $\pm 0.3$ | $\pm 1.0$ | $\mu \mathrm{A}$ |

AC Electrical Characteristics $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{t}_{\mathrm{r}}=\mathrm{t}_{\mathrm{t}}=20$ ns and $\mathrm{V}_{S S}=\mathrm{OV}$ unless otherwise specified

| Parameter |  | Conditions | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| tPHL, tPLH | Propagation Delay Time Signal Input to Signal Output | $\begin{aligned} & V_{C}=V_{D D}, C_{L}=50 \mathrm{pF}, \text { (Figure 1) } \\ & R_{\mathrm{L}}=200 \mathrm{k} \\ & V_{D D}=5 \mathrm{~V} \\ & V_{D D}=10 \mathrm{~V} \\ & V_{D D}=15 \mathrm{~V} \end{aligned}$ |  | $\begin{aligned} & 25 \\ & 15 \\ & 10 \end{aligned}$ | $\begin{aligned} & 55 \\ & 35 \\ & 25 \end{aligned}$ | ns <br> ns <br> ns |
| tPZH, tPZL | Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level | $\begin{aligned} & R_{\mathrm{L}}=1.0 \mathrm{k} \Omega, C_{\mathrm{L}}=50 \mathrm{pF}, \text { (Figures } 2 \\ & \text { and } 3 \text { ) } \\ & \mathrm{V}_{\mathrm{DD}}=5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{DD}}=10 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{DD}}=15 \mathrm{~V} \end{aligned}$ |  |  | $\begin{aligned} & 125 \\ & 60 \\ & 50 \end{aligned}$ | ns <br> ns <br> ns |
| tPHZ, tPLZ | Propagation Delay Time Control Input to Signal Output Logical Level to High Impedance | $R_{L}=1.0 \mathrm{k} \Omega, C_{L}=50 \mathrm{pF} \text {, (Figures } 2$ <br> and 3) $\begin{aligned} & V_{D D}=5 \mathrm{~V} \\ & V_{D D}=10 \mathrm{~V} \\ & V_{D D}=15 \mathrm{~V} \end{aligned}$ |  |  | $\begin{aligned} & 125 \\ & 60 \\ & 50 \end{aligned}$ | ns <br> ns <br> ns |
|  | Sine Wave Distortion | $\begin{aligned} & V_{C}=V_{D D}=5 \mathrm{~V}, V_{S S}=-5 \mathrm{~V} \\ & R_{L}=10 \mathrm{k} \Omega, V_{I S}=5 V_{p-p}, f=1 \mathrm{kHz}, \\ & \text { (Figure 4) } \end{aligned}$ |  | 0.1 |  | \% |
|  | Frequency Response-Switch "ON" (Frequency at -3 dB) | $\begin{aligned} & V_{C}=V_{D D}=5 \mathrm{~V}, V_{S S}=-5 \mathrm{~V}, \\ & R_{L}=1 \mathrm{k} \Omega, V_{I S}=5 V_{P-p} . \end{aligned}$ <br> 20 Log 10 VOS $/ \operatorname{VOS}_{\text {O }}(1 \mathrm{kHz})-\mathrm{dB}$, (Figure 4) |  | 40 |  | MHz |

## AC Electrical Characteristics (Continued)

$T_{A}=25^{\circ} \mathrm{C}, \mathrm{t}_{\mathrm{r}}=\mathrm{t}_{\mathrm{t}}=20 \mathrm{~ns}$ and $\mathrm{V}_{\mathrm{SS}}=0 \mathrm{~V}$ unless otherwise noted


Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.
Note 2: $V_{S S}=0 \mathrm{~V}$ unless otherwise specified.
Note 3: These devices should not be connected to circuits with the power "ON".
Note 4: In all cases, there is approximately 5 pF of probe and jig capacitance in the output; however, this capacitance is included in $C_{L}$ wherever it is specified.
Note 5: $V_{I S}$ is the voltage at the in/out pin and $V_{O S}$ is the voltage at the out/in pin. $V_{C}$ is the voltage at the control input.
Note 6: Conditions for $V_{I H C}$ :
$\begin{array}{ll}\text { a) } V_{I S}=V_{D D}, I_{O S}=s t a n d a r d ~ & \text { series } I_{O H} \\ V_{I S}=0 V & I_{O L}=s t a n d a r d B \text { series } I_{O L} \text {. }\end{array}$

## AC Test Circuits and Switching Time Waveforms



FIGURE 1. tPHL, tplH Propagation Delay Time Signal Input to Signal Output


FIGURE 2. tPZH. tPHZ Propagation Delay Time Control to Signal Output


FIGURE 3. tpZL. iplz Propagation Delay Time Control to Signal Output

## AC Test Circuits and Switching Time Waveforms (Cont'd.)



$V_{C}=V_{D D}$ for distortion and frequency response tests $V_{C}=V_{S S}$ for feedthrough test

FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough


FIGURE 5. Crosstalk Between Any Two Switches


FIGURE 6. Crosstalk: Control Input to Signal Output

$v_{0 s}$


FIGURE 7. Maximum Control Input Frequency

Typical Performance Characteristics

"ON" Resistance as a Function
of Temperature for $V_{D D}-V_{S S}=10 \mathrm{~V}$


SIGNAL VOLTAGE (VIS) (V)

## Special Considerations

In applications where separate power sources are used to drive $V_{D D}$ and the signal input, the $V_{D D}$ current capability should exceed $V_{D D} / R_{L} / R_{L}=$ effective external load of the 4 CD4066BM/CD4066BC bilateral switches). This provision avoids any permanent current flow or clamp action on the $V_{D D}$ supply when power is applied or removed from CD4066BM/CD4066BC.

In certain applications, the external load-resistor current may include both VDD and signal-line components. To
"ON" Resistance as a Function of Temperature for
$V_{D D}-V_{S S}=15 V$

"ON" Resistance as a Function of Temperature for $\mathbf{V}_{D D}-\mathbf{V}_{\mathbf{S S}}=\mathbf{5 V}$

avoid drawing VDD current when switch current flows into terminals $1,4,8$ or 11 , the voltage drop across the bidirectional switch must not exceed 0.6 V at $\mathrm{T}_{\mathrm{A}} \leq 25^{\circ} \mathrm{C}$, or 0.4 V at $\mathrm{T}_{\mathrm{A}}>25^{\circ} \mathrm{C}$ (calculated from $\mathrm{R}_{\mathrm{ON}}$ values shown).

No $V_{D D}$ current will flow through $R_{L}$ if the switch current flows into terminals $2,3,9$ or 10.

