On-screen display for camcorders BU2848FS/BU2870FS/BU2873FS

The BU2848FS, BU2870FS and BU2873FS series ICs are fabricated using a CMOS process, and are designed for displaying character data on camcorder and television screens. The ICs are controlled by serial data from a microcontroller, and display patterns and data such as the date on the camcorder viewfinder. The characters are displayed in a 12×18 bit matrix, so Chinese characters can also be displayed. The display format is 12 lines ×24 characters. There is no space between characters, so two or more characters can be joined to form icons.

The ICs are available in small SSOP packages and are suitable for high-density mounting in camcorders.

Series

Part No.	No. of Characters
BU2873FS	64
BU2848FS	128
BU2870FS	256

Applications

Camcorders and televisions

Features

1)12 line×24 character display.

2)64, 128, or 256 character types depending on the model.

3)Three-system monochrome output.

4)Character size can be selected as 1H/dot or 2H/dot.5)Background can be selected on a per screen basis: none, border, knockout or solid.

6)12×18 dot matrix, with no space between characters.
7)Character blinking ratio can be selected as 1:1, 3:1, or 1: 3.

8)8-bit serial microcontroller interface.

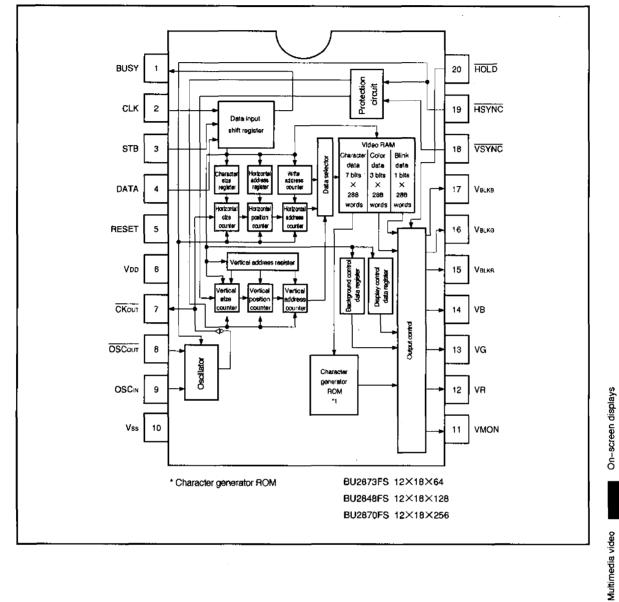
9)5V power supply.

10)CMOS for low power consumption.

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BU2848FS/BU2870FS/BU2873FS



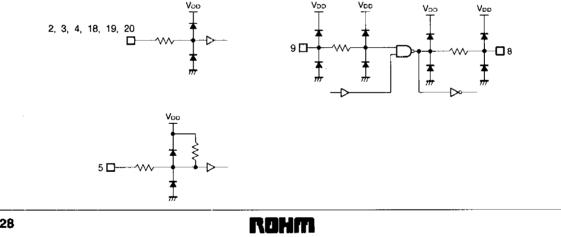
Block diagram

BU2848FS/BU2870FS/BU2873FS

Pin descriptions

Pin No.	Input/output	Symbol	Function
1	Output	BUSY	Informs the microcontroller when strobe input is possible after serial data input. Strobe input can be input when this is low.
2	Input	CLK	Clock input for reading in data. Data on the DATA pin is read in on the rising edge of the clock.
3	Input	STB	Input pin for the strobe signal after serial-data input. The eight bits of data are read in on the rising edge of the pulse applied to the STB pin. When the bit-data is character data, the data address is incremented on the falling edge of the pulse.
4	Input	DATA	Control data input pin. Data on this pin is read synchronously with the rising edge of the clock signal.
5	Input	RESET	Resets all internal registers. Clears the internal RAM in the case of the BU2870FS. (Pullup resister connected)
6	-	VDD	Power supply (+5V)
7	Output	CKOUT	OSC OUT inverting output. Use to check the oscillator frequency.
8 9	Input Output	OSCOUT OSCIN	For connection to oscillator capacitor and coil.
10	_	Vss	Connect to system GND.
11	Output	VMON	High level is output when one of the VR, VG, or VB character signal outputs is high.
12 13 14	Output	VR VG VB	Character data output pin. Three-system output can be selected on a character basis. Active high output.
15 16 17	Output	Vəlkr Velkg Velke	Blanking signal output for cutting the video signal. Active high output.
18	Input	VSYNC	Vertical sync input. Active low input.
19	Input	HSYNC	Horizontal sync input. Active low input.
20	Input	HOLD	Low level input stops the oscillator. At this time, VR, VG, VB, and VBLK outputs all go low. (This input is normally high.)

Input/output circuits



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rising edge of the STB signal. In the case of formatted

data, the BUSY signal falls after the internal state has

stabilized completely. When the data is written to VRAM,

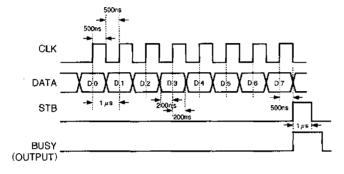
the BUSY signal falls when the data write operation is

complete.

Serial data timing

The control commands are in 8-bit serial input format. After the eight bits of command data have been input, a STB pulse is input to execute the command.

The data is read into a shift register on the rising edge of the CLK signal, and copied to the other registers on the



●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit		
Power supply voltage	VDD	-0.3~7.0	V		
Power dissipation	P⊳	750 *	mW		
Operating temperature	Tstg		ĉ		
Storage temperature	Topr	-20~75	Ĵ		
Pin voltages			v		

* Reduced by 6.0mW for each increase in Ta of 1°C over 25°C.

●Electrical characteristics (Unless otherwise specified: Ta=25℃ and Vob=5V)

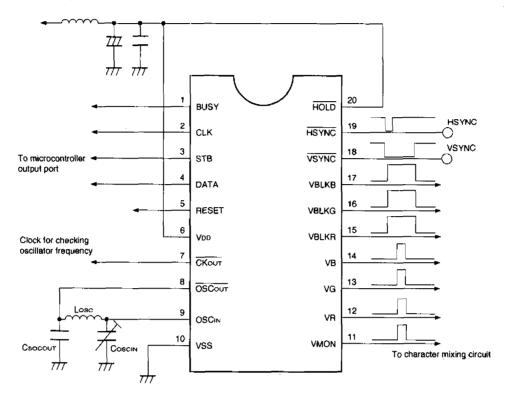
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Operating voltage	Vod		5	-	V	
"L" input voltage	Vi∟2	0	_	0.3Voo	V	For CMOS input
"H" input voltage	V(H2	0.7Vpp		Voo	V	For CMOS input
"L" output voltage	Vol.1		_	0.4	v	For OSC
"H" output voltage	Vон1	4.6	_	-	٧	For OSC
"L" output voltage	Vol2	0	_	0.4	V	la∟≦2mA
"H" output voltage	VOH2	4.6		-	V	lon≦1mA
Input leakage current	ĺu	-	_	1	μA	
Output leakage current	ILO	_	_	10	μA	
Input pullup resistance	lın	_	28	70	kΩ	Pullup input
Operating current	lop	—	_	10	mA	

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On-screen displays

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Application example



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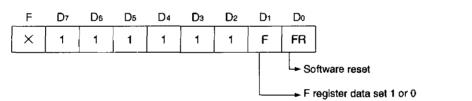
Command format

The control command format is 8-bit serial data. After the eight bits of data for the command have been input, a STB pulse is input to execute the command.

Content	F	D7	D6	D5	D4	Da	D2	Dı	D٥
Display character data	0	0	C6	C5	C₄	C3	C2	C1	Co
Character unit, blink data	0	1	0	0	0	Blink	R	G	В
Character display line address	0	1	0	0	1	ARı	AR2	ARı	AR ₀
Character display column address	0	1	0	1	AC4	AC3	AC ₂	AC1	ACo
Background specification	0	1	1	0	BS4	BS₃	RB	GB	BB
Blinking, dot oscillation control and display ON/OFF	0	1	1	1	0	D٥	BL2	BL1	OSC
Character code, bank switch *1	0	1	1	1	1	0	1	0	Α
Frame control	0	1	1	1	1	0	0	Egi	0
Format specification	×	1	1	1	1	1	1	F	FR
Display position vertical address	1	0	1	0	V4	V۹	V۶	V1	Vo
Display position horizontal address	1	1	1	0	H₄	Hs	H2	Hı	Ho
Character size specification	1	1	0	M	S₄	AR₃	AR ₂	AR1	ARo
Test mode setting	1	1	1	1	0	Тз	T2	τ1	Τo

*1 Only used for the BU2870FS.

Format set



Software reset (BU2848FS and BU2873FS)

Reset when a "1" is input. The software reset data is not latched. After this command is executed, the following registers are reset.

Character size register

test mode set register

format specification F→0

Data in the other registers is preserved. In the case of the BU2870FS, zeros are written to the RAM.

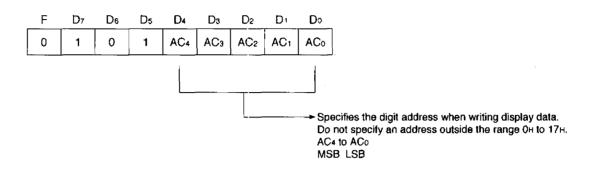
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On-screen displays

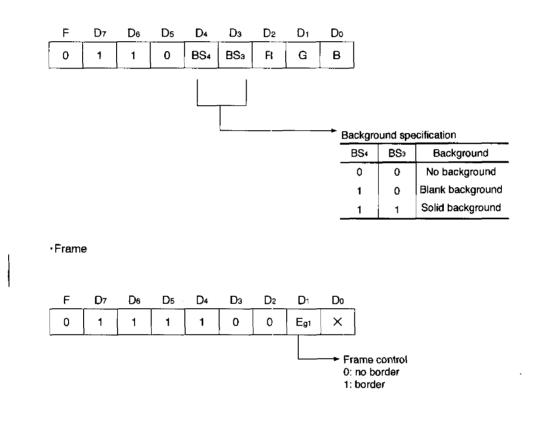
Multimedia video

BU2848FS/BU2870FS/BU2873FS

·Character display column address



·Background specification



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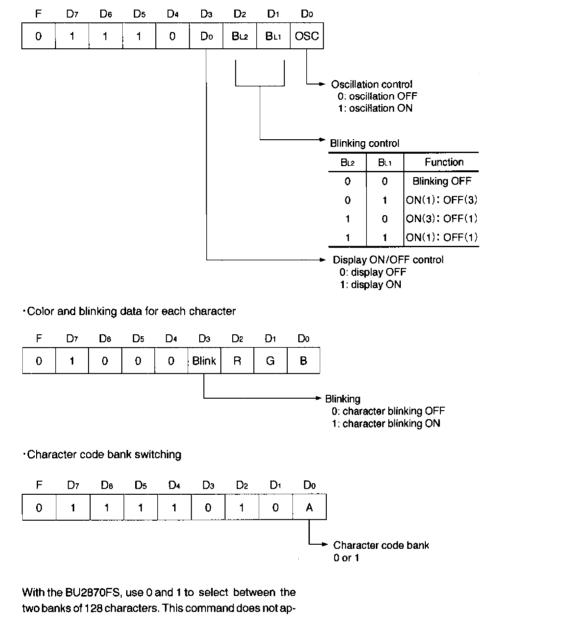
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Command format

Blinking, dot oscillation control, and display ON/OFF



ply to the BU2848FS and BU2873FS.

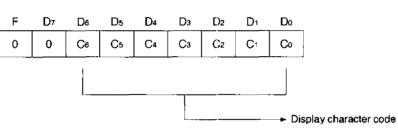
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On-screen displays

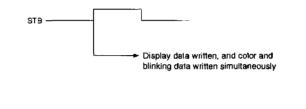
Multimedia video

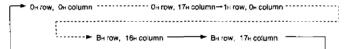
BU2848FS/BU2870FS/BU2873FS

Writing display data



The address counter is incremented after the display data writing is complete.

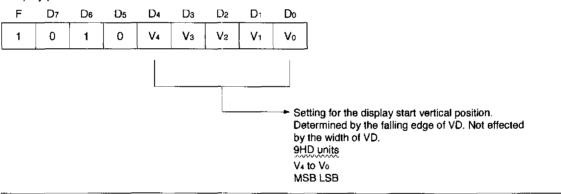




- * 1)The address counter is incremented after the RAM data is written. It is not effected by the STB pulse width.
- * 2)The BUSY flag is high while the data is being written, but all other commands can be processed simultaneously.

It is possible to change the display position horizontal address and display position vertical address as described below.

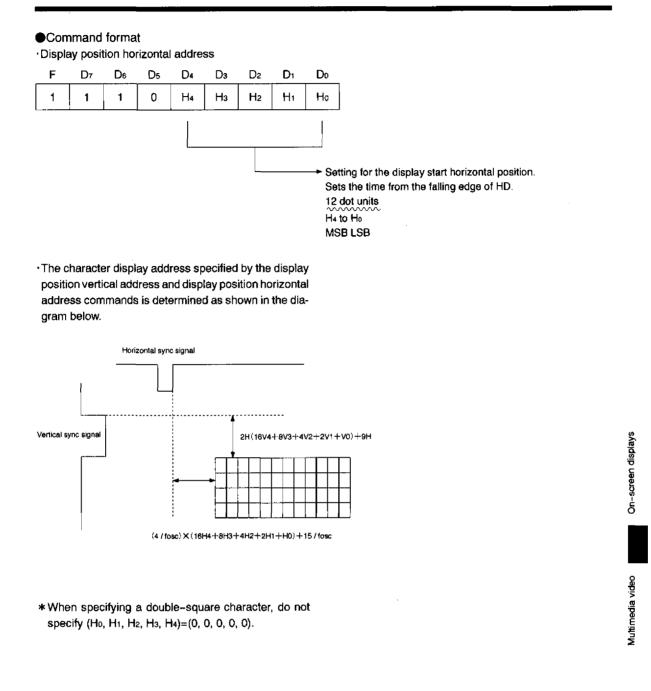
·Display position vertical address



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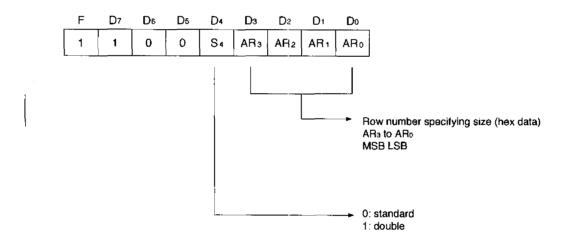
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Character display

The number of characters that can be displayed is 288 (12 lines \times 24 characters).

AC0~	AC4	00	01	02	03	04	05	06	07	08	09	0A	0 8	0C	0D	0E	0F	10	11	12	13	14	15	16	1
	00																								Γ
	01	i																							
	02				[ļ											Γ
	03															_									ſ
	04																								ſ
AR3	05															-					1				Γ
~AR0	06					[Ī
	07																								Γ
	08																								Γ
	09											_													Γ
	OA																								t
	0B	-																							T

·Character size specification



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EPROM address and character data

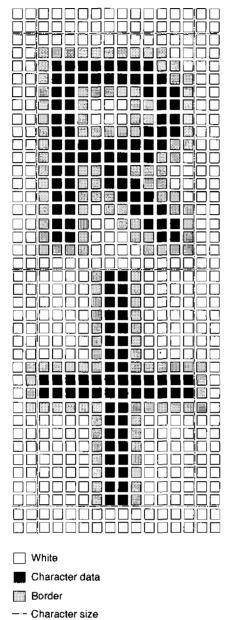
[RC	DM1]							[ROM2]	
EPROM	Character	data (Bll	N)	Character	Cł	haract	er data	a (BIN)	Character
Address A	0 A1 A2 A	3 A4 A5	A6 A7	data (HEX)	A0 A	1 A2	A3 A4	A5 A6 A7	data (HEX)
0000 0	000	0 0 0	0 0	00	0 0	0 0	0 0	0 0 0	00
00010	0 0 0	0 0	0 0	00	0 0	0 0	0 0	0 0 0	00
00020	000	0	0	60	0 0	0 0	0 0	000	00
00030	000) ia ti	n /	F 0	0 0	0 0	0 0	0 0 0	00
0004 0	00	- XX - 1	1.1	F 8	0 (0 0	0	0 0 0	01
0005 0	0	1 1 0	0 0	80	0 0	0 0	0	0 0	03
0006 0	111	0 0	0 0	0 E	0 (0 0	0	0	07
00070		0 0 0	0 0	06	0 (0 0	0 0	1 1 0	06
00080		0 0 0	00	06	0 (0 0	0 0	f , 100 0	06
00090	111 0	0 0 0	00	06	0 (0 0	0 0	1/2 11 0	06
0 0 0 A 0	1 3 1	1. 1 . 15	121	FE	0 (0 0	0	1 1 0	07
000B 0	1 1 1	1 1 1	1 44	FE	0 (0 0	0 1	* 1 0	07
000000	• 1.*1 C	0 0 0	0 0	06	0 0	0 0	0 0	1 1.0	06
000D 0	1 1 0	0 0 0	0 0	06	0 (0 0	0 0	1 0	06
000E 0	1 2017 C	0 0	0 0	06	0 (0 0	0 0	1 0	06
000F 0	ាំ។ ប	0 0 0	0 0	06	0 (0 0	0 0	1 1 0	06
0010 0	000	0 0 0	0 0	00	0 (0 0	0 0	0 0 0	00
0011 0	000	0 0	0 0	00	0 0	0 0	0 0	0 0 0	00
00120	000	0 0	0 0	00	0 (0 0	0 0	0 '0 0	00
•		•					•		
•		•					•		
•		•					•		
001F 0	000	0 0 0	00	00	0 (0 0	0 0	0 0 0	0 0



Multimedia video

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Frame data



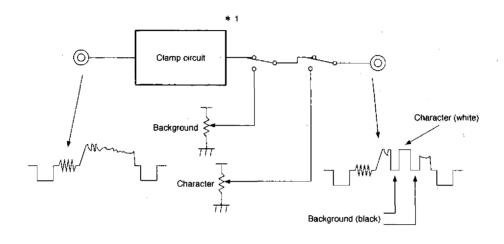
BU2848FS/BU2870FS/BU2873FS

The conditions for display of border data are no character data above the cell, and character data in one of the cells above, below, left, right, or diagonally removed from the cell. However, border data is not displayed above character data in the first row, below character data in the 18th row, or when there is character data in the first column. When there is character data in the 12th column, border data is displayed on the right, but when the next character is in the off state, the border is not displayed.

In the case of the 24th character, the border data for character data in the 12th column is not displayed. Character blinking is set individually for each character. When there is a border to the left or right in another character's area, blinking does not occur.

BU2848FS/BU2870FS/BU2873FS

•Character superimposition (black and white) To superimpose characters on a VCR, either a composite or color difference (component) signal is used. In the case of a composite signal, sync and color signals are included, so caution is required to ensure that the timing does not overlap.



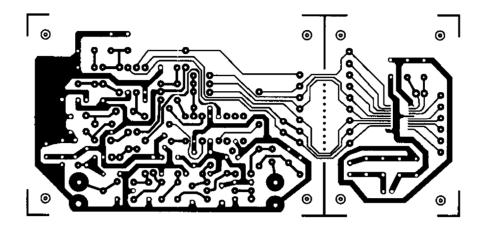
* 1) Composite signals have their level fixed at 1 VP-P, and the DC level is fixed. However, in many cases, the signal used has had its frequency components removed by a capacitor. To superimpose white, gray, and black levels the DC level of the signal to be superimposed must be fixed with reference to the pedestal-level voltage. This is done using a clamp circuit.



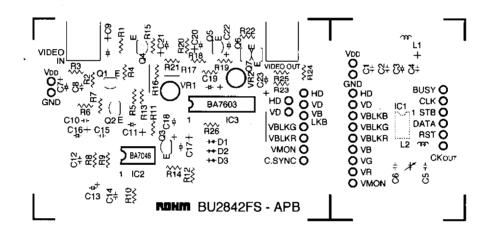
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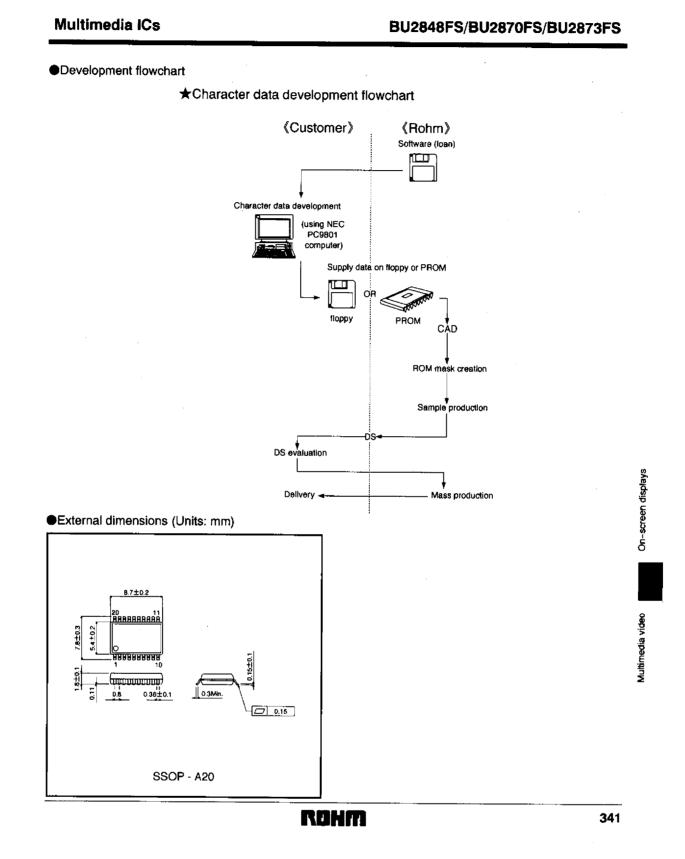
●PCB for application example circuit (solder side)



PCB for application example circuit (component side)



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