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Microchip 93 Series Serial EEPROM Compatibility

INTRODUCTION

With Microchip Technology's introduction of the 93XX46, 93XX56, and 93XX66 devices in the 'A' and 'B' versions, a certain number of compatibility questions have arisen. This application note is intended to discuss, in detail, the differences between each of the variations of the 93XX series of devices offered and address all of the technical considerations related to the conversion from one device to another.

There are several key areas in which compatibility, particularly with respect to conversion from the 'original' 93XX46/56/66 and 93XX46B/56B/66B to the new 93XX46A/B, 93XX56A/B, and 93XX66A/B, must be specifically addressed. These areas include the following:

- Operating Voltage Range
- Write Cycle Initiation
- CS Functionality
- Ready/$\overline{\text{Busy}}$ Polling
- Tying DI and DO together
- Noise Immunity

Each of these points is addressed individually in this app note under a section heading of the same name.

PRODUCT FAMILY OVERVIEW

The current 93 series product offering from Microchip Technology totals 31 devices when including both the original and the new devices. In addition, each device is offered in one or more temperature grades. This fairly large number of individual products is mitigated, from a compatibility standpoint, by the fact that for many of the devices a single die is used for multiple 'part numbers'. For example, the original 93AA46, 93AA46B, 93LC46, and 93LC46B are all 'made' from the exact same die. The 'AA' and 'LC' versions are separated by testing to different V_{DD} limits and the 'B' version is a bonding option. In other cases multiple parts are created from a single die through the use of metal level options during fabrication. The significance of this is in the fact that in any case where a single die makes multiple parts (as in the example of the 93XX46/46B above) the functionality is identical for all variations. This effectively reduces the number of different devices that have to be addressed in this application note by allowing several devices to be grouped together for the purpose of functional discussions. Further reduction is possible by grouping devices of different array sizes together when their functionality is otherwise identical. Finally, devices can also be grouped together regardless of whether they utilize X8 or X16 communication.

Table 1 provides a list of devices that have been grouped together such that the members of each group are functionally identical with the exceptions of voltage range, array size, and/or X8/X16 communication (which are irrelevant for the purposes of this application note)

TABLE 1: FUNCTIONAL GROUPING

Group	Devices
1	93C06, 93C46
2 (Original)	93AA46/46B, 93LC46/46B, 93AA56/56B, 93LC56/56B, 93C56/56B, 93AA66/66B, 93LC66/66B, 93C66/66B
3	93AA76, 93LC76, 93C76 93AA86, 93LC86, 93C86
4 (New)	93LC46A/46B, 93LC56A/56B, 93LC66A/66B
5	93C46B, 93C56A/56B, 93C66A/66B

For the remainder of this document reference will only be made to the functional group number listed above rather than to specific devices. In all cases any device from within the group will function as described.

OPERATING VOLTAGE RANGE

One key difference between Group 2 'LC' devices and Group 4 'LC' devices is the range of V_{DD} over which the devices operate. Group 2 devices are specified to operate from 2.0V to 6.0V and Group 4 devices are specified from 2.5V to 6.0V. Group 4 devices have a V_{DD} threshold detect that is set at ~2.2V (nominal) which prevents operation when V_{DD} drops below that level. In any application where a Group 2 'LC' device is being used at a V_{DD} level below 2.5V, the equivalent 'AA' Group 2 device should be used. Because this conversion does not require using a device from a new functional group (see Table 1) there are no other compatibility issues. The second compatibility issue arises from converting from Group 2 'C' devices to Group 5 'C' devices. Group 2 devices, while specified as 'C' which indicates a V_{DD} operating range of 4.5V to 5.5V, will actually operate down to ~1.8V due to the fact that the V_{CC} threshold detection circuit has a ~1.5V trip point. Group 5 'C' devices, however, have a V_{CC} threshold detect trip point of ~3.8V. Because of this difference in trip point settings, applications that previously used Group 2 'C' devices, and have a requirement to operate below 4.5V, should be converted to Group 4 'LC' devices, which will operate down to 2.5V.

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WRITE CYCLE INITIATION

For the 93 Series EEPROM's, the internal write cycle is initiated by one of two events depending upon the functional group. For Groups 1, 3, and 5 the write cycle is initiated by the rising edge of CLK for the last data bit (D_0). For Groups 2 and 4, the write cycle is not initiated until CS is lowered.

The devices in Groups 1 and 5 are targeted specifically at 5V, extended temperature applications. Group 5 devices were intentionally designed to have the same write cycle CS functionality as Group 1 devices in order to serve as drop in replacements. Group 3 devices are unique in that they span the entire voltage range but also initiate the write cycle on the rising edge of CLK.

A potential compatibility issue regarding write cycle CS functionality only occurs if converting from Group 1, 3 or 5 devices to Group 2 or 4 devices. The issue is that with Groups 1, 3 or 5 devices the write cycle is initiated as soon as the rising edge of CLK is detected for the last data bit and the application firmware is not required to lower the CS line until: either the next command is to be sent (Group 1 or, 2) not at all (Group 3 and 5). So if a Group 2 or 4 device were to be placed into such an application the write cycle would not be initiated until just before the next command or not at all. In both cases the command following the write would be ignored. For case one, the part would be in a write cycle and would not recognize the command, and for case two, the device would see an invalid command and abort (no falling edge of CS after write command).

When converting from Group 2 or 4 devices to Group 1, 3 or 5 devices there are no compatibility issues related to write cycle CS functionality.

CS FUNCTIONALITY

In addition to the write cycle initiation compatibility question discussed in the previous section there are a couple of other conditions related to CS functionality that must be understood. These are related to both how the CS function works for the various devices, as well as to what conditions may occur, due to the way the firmware is written, which may cause problems. Table 2 details the differences in the way the CS pin functions for the various device groups. As can bee seen from the table (Item 1) devices in Groups 2 and 4 require that CS be brought low, after the write command is given, in order for the write cycle to be initiated.

This presents a compatibility problem only when converting from Group 3 or 5 devices to Group 2 or 4 (i.e. reducing EEPROM array size or moving from a 5V design to 2.5V or 1.8V design). In order to minimize this compatibility problem, CS should always be brought low after sending a write command, regardless of which device is being used.

Item 2 in Table 2 shows that Group 1 devices require a low to high transition on the CS pin after the write cycle has completed if data polling was used. If the CS line is not brought low after the write command is sent (i.e. data polling is not used), then no transition is required on CS after the write cycle completes (Item 3). To avoid this compatibility problem, CS should always be brought high at the end of a data polling routine.

Items 4 and 5 show that Group 1 devices require a low to high transition to occur after a write cycle completes in order for the next command to be recognized.

TABLE 2: CS FUNCTIONALITY

Item	Group 1	Group 2	Group 3	Group 4	Group 5	Description
1	No	Yes	No	Yes	No	Does CS have to go low to start the write Cycle?
2	Yes	No	No	No	No	Does CS, if data polling is used, have to have a low to high transition after the write cycle in order for the next command to be recognized?
3	Yes	N/A	N/A	Yes	Yes	If CS is not lowered after a write command, and is held high through the write cycle, will the next command be recognized?
4	No	Yes	Yes	Yes	Yes	If CS is brought high during write cycle will the next command be recognized?
5	No	Yes	Yes	Yes	Yes	If CS changes during write cycle, and is high at the end of the write cycle, will the next command be recognized?

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READY/$\overline{\text{BUSY}}$ POLLING

Ready/$\overline{\text{Busy}}$ polling is a method that allows the MCU to poll the serial EEPROM device during a write cycle to determine when the write cycle has completed. The basic operation is that once a write cycle has been initiated the serial EEPROM will drive the DO line low, if CS is brought high during the write cycle, until the write cycle is complete. Once the write cycle has completed the DO pin is driven high.

There are two methods of functional operation of the DO pin for ready busy polling. The first (or original) method applies to Group 1, 2, and 3 devices. For these devices when CS is brought high during a write cycle, the DO pin will drive low while the write is in progress and then drive high once complete. If the CS pin is brought high at any time after a write cycle has completed, the DO pin remains in a high impedance state.

For Group 4 and 5 devices the operation is the same except that when CS is brought high after a write cycle is complete, the DO pin will drive high to indicate a ready state. This was done because on the original devices it was possible to miss the Ready signal if data polling was not started until after the write cycle completed. The DO pin will continue to drive the ready signal out until a start condition is detected, at which time the DO pin will return to a high impedance state. This difference in operation only becomes a compatibility issue if the DI and DO lines are being tied together for two wire operation (see the next section for a separate discussion of this issue).

TYING DI AND DO TOGETHER

When using the new 93 series devices (Group 4 and 5) with DI and DO tied directly together a bus contention issue will arise and in most cases will render the bus inoperable. The problem is a result of the change that was made to the operation of the DO pin during Ready/$\overline{\text{Busy}}$ polling. The original 93 series devices (Group 1,2 and 3) all tri-state the DO pin any time CS is brought high after a write cycle has finished. The new 93 series devices (Group 4 and 5) do not tri-state DO in the same situation, but instead drive the DO pin high to indicate the ready state. Because the DO pin (and therefore the DI pin also when DO and DI are tied together) is being actively driven high by the serial EEPROM a potential for bus contention exists if the MCU attempts to drive the DI line low. The actual voltage level of the bus will be a function of the sink capability of the MCU I/O pin and the source capability of the serial EEPROM. To prevent this bus contention issue it is necessary to use a resistor (~10K Ohm typical) to tie DI to DO instead of a direct connection.

Another potential problem with tying DI and DO occurs if CS is brought high after the write cycle has been initiated and valid clock transitions occur on the CLK line during the write cycle. This can cause the device to see an inadvertent START condition when the write cycle ends (and the DO line drives high to the Ready state). This is caused by the fact that the Twc of the device is variable (depending upon process/Vcc/temperature variations) and, therefore, causes the write cycle to end in an asynchronous fashion with respect to the clock. For example, if CS is high when the write cycle ends and DO goes high (thereby pulling DI high), then a low to high transition on the CLK will be seen as a valid START condition when it may not have been intended to be a START condition.

NOISE IMMUNITY

Probably the single biggest compatibility issue (related to conversions) exists between the original 93 series devices and the new devices due to noise immunity. The new devices (Group 4 and 5) are much faster internally than the older devices which makes them more susceptible to noise. This noise susceptibility becomes an acute problem during power up/down, during which time the state of the CS pin may be allowed to float up by an MCU that is not fully powered up. If this occurs it is very possible that noise on the CLK and DI pins can occur in the correct sequence required to issue an EWEN command followed by a spurious erase or write command. The most common occurrence is that of the EWEN followed by an ERASE command with the address and data bits all set to '1', so the last byte of the array is erased to 'FF'. The solution for this problem is a pull down resistor on the CS pin, which will prevent the device from responding to the spurious 'commands' on the CLK and DI lines.

DEVELOPING ROBUST CODE AND HARDWARE

In order to design a system (both hardware and firmware) that will be portable when changing the particular 93 series device being interfaced with, the following suggestions should be considered:

- The CS pin should be brought low at the end of every command issued to the device.
- Utilize Ready/$\overline{\text{Busy}}$ polling to verify that the device has completed the write operation rather than a delay loop of fixed duration.
- Create a data polling routine that leaves the CS line low when it is finished.
- Do not allow transitions on the CLK line (if CS is high) while the device is in a write cycle.
- Utilize a resistor between DO and DI if implementing a two wire interface.
- Utilize a pull down resistor on the CS line to prevent spurious commands during power up/down.

SUMMARY

When converting from one 93 series device to another there are a few key items that must be examined from the firmware side, as well as from the hardware side. By careful attention to these items it is possible to simplify and expedite the conversion process, as well as develop robust code and designs that will minimize the requirement for future changes.

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