Universal Multichannel Industrial Signal Conditioning ADC

PRELIMINARY TECHNICAL DATA AD280

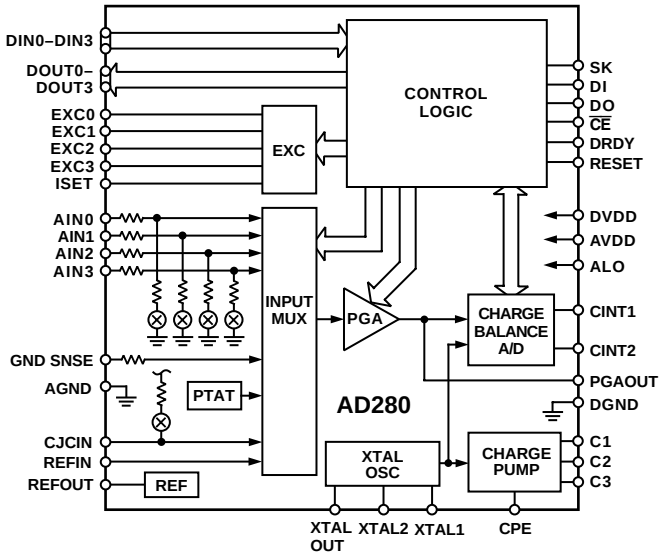
FEATURES

Four Input Channels, with Protection and Switchable Attenuation
Provision for Cold Junction Sensor
Programmable Excitation Sources for RTD Measurement and Open Input Detection
PGA with Programmable Gains from 1 to 128
High Resolution Integrating A/D Converter with Programmable Integration Period, Up to 18-Bit Usable Resolution
2.5 Volt Reference
Crystal Oscillator
Charge Pump Circuit to Allow Single +5 V Power
Serial Interface Compatible with Most Microcontrollers and Microprocessors

APPLICATIONS

Industrial Data Acquisition
DCS (Distributed Control Systems)
PLC (Programmable Logic Controllers)

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD280 is a front-end integrated circuit for use in industrial data acquisition applications. It has been specifically designed for the stringent requirements of industrial applications, with functions such as protection/protectability and high normal-mode rejection. The AD280 can be configured to accept up to four mV/V/TC inputs, or up to two RTD inputs (in 2-, 3- or 4-wire connection modes).

The AD280 is not a stand-alone product, but is intended to be used with a companion microcontroller or microprocessor. Descriptions of appropriate algorithms and control routines for this device are contained in this data sheet, as well as on a separate application note.

The four primary input channels are designed for high input impedance for input signals up to ±2.5 volts. Each also contains a programmable input attenuator for input ranges up to ±10 volts at reduced input impedance. The inputs contain internal protection to allow for overload without affecting the accuracy or operability of adjacent inputs. The input multiplexer also features a ground sense input and a separate input (with programmable excitation) for solid-state or thermistor temperature sensors for cold junction compensation of thermocouples. An internal PTAT (Proportional to Absolute Temperature) sensor permits measurement of internal die temperature.

The AD280 also offers four configurable excitation current sources. Two of these sources can be configured to provide excitation for RTDs, the amplitude of which can be set by an external resistor. All four excitation sources can be set to provide +25 nA or –25 nA for use in detecting open inputs. The excitation sources are separately pinned out to allow for external protection devices to achieve very high normal-mode voltage protection.

The input multiplexer feeds a programmable gain amplifier, with binary gains from 1 to 128. The PGA drives a high resolution integrating A/D converter, which is software programmable for integration time and can achieve usable resolution of up to 18 bits.

The AD280 features a serial interface, operable to 10 MHz, and is compatible with a wide variety of microcontrollers and microprocessors. An onboard crystal oscillator and charge pump circuit are provided. The charge pump circuit, requiring just two external capacitors, provides the negative bias for this device and allows full operation from a single +5 V supply.

Four general purpose digital outputs and four general purpose digital inputs are also provided; these may be used to implement external functions that may be required in some applications.

REV. 0

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AD280–SPECIFICATIONS[1] (@ T_A = –25°C to +85°C, V_{DD} = +5 V ± 10% unless otherwise noted)

Parameter	Min	Typ	Max	Units	Notes
INPUT CHARACTERISTICS					
Input Voltage Range					
High Impedance Mode	±3	±3.5		V	For Linear Operation Without Signal Clipping in High Impedance Mode, Pins AIN0–AIN3
Attenuator Mode	±11			V	For Linear Operation Without Signal Clipping in Attenuator Mode, Pins AIN0–AIN3
Input Impedance					
High Impedance Mode		20		MΩ	Pins AIN0–AIN3, Also GND SENSE and CJCIN when JC Excitation Is Disabled
Attenuator Mode	70	100	130	kΩ	Pins AIN0–AIN3
Bias Current		1		nA	Pins AIN0–AIN3, Also GND SENSE and CJCIN when JC Excitation Is Disabled
Bias Current over Temperature Range			2	nA	Pins AIN0–AIN3, Also GND SENSE and CJCIN when JC Excitation Is Disabled
Differential Bias Current		100		pA	Difference Between Perceived Bias Current at Any Input Pin When Selected
Input Capacitance		7		pF	Pins AIN0–AIN3, Also GND SENSE and CJCIN when JC Excitation Is Disabled
PROGRAMMABLE GAIN AMPLIFIER					
PGA Gains	1		128		In Binary Steps
Gain Ratio Accuracy		0.1	0.3	%/FSR	
Gain Ratio Temperature Stability		5		ppm/°C FSR	
Input Offset Voltage		10	50	µV	
Input Offset Voltage Temperature Stability		2	5	µV/°C	
A/D CONVERTER					
Conversion Period	1		200	ms	Programmable, Dependent Upon Crystal Oscillator Frequency
Resolution		±32,000		Counts	@ t_{INT} = 16.66 ms, f_{CLK} = 12 MHz
		±100,000		Counts	@ t_{INT} = 200 ms, f_{CLK} = 12 MHz
Integral Linearity		±0.0015	±0.003	% FSR	Including PGA Nonlinearity
Noise		±4		Counts	@ t_{INT} = 100 ms, f_{CLK} = 12 MHz
Normal-Mode Rejection		92		dB	@ t_{INT} = 16.66 ms, f_{CLK} = 12 MHz
		106		dB	@ t_{INT} = 100 ms, f_{CLK} = 12 MHz
Measurement Latency	0	25	50	µs	With C_{INT} = 4.7 nF (see Note 1)
Nominal Input Span		±2.5	±3	V	
Input Offset		±100		µV	See Note 2
Input Offset Drift		±20	±50	µV/°C	See Note 2
Span Error		±0.5		% FSR	See Note 2
Span Drift		±25	±50	ppm/°C	See Note 2
EXCITATION OUTPUTS					
Output Current					
Excitation Disabled			1	nA	EXC0–EXC3
Set for Positive Open Circuit Detection	–20	–25	–30	nA	EXC0–EXC3
Set for Negative Open Circuit Detection	20	25	30	nA	EXC0–EXC3
Set for RTD Excitation	0		2	mA	EXC0 and EXC1 Only, Magnitude Depends on Value of External Resistor
Temperature Stability, RTD Mode		±35		ppm/°C	EXC0 and EXC1 Only, Not Including Drift of External Resistor
REFERENCE OUTPUT AND INPUT					
Reference Voltage	2.475	2.5	2.525	V	
Reference Voltage Temperature Stability		25		ppm/°C	
Reference Pin Output Current			1	mA	Excluding Current Required by REFIN Pin
DIGITAL LEVELS					
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Voltage	2			V	
Output Logic 0 Voltage			0.45	V	@ I = 1 mA
Output Logic 1 Voltage	2.4			V	@ I = –60 µA

Parameter	Min	Typ	Max	Units	Notes
PTAT SENSOR (INTERNAL)					
Voltage @ +25°C		0.475		V	
Sensitivity		1.8		mV/°C	
Integral Linearity		±2		°C	
POWER SUPPLY					
V_{DD} (Analog and Digital)	4.75	5	5.25	V	
I_{DD} (Analog)		2.5	3	mA	
I_{DD} (Digital)		1	1.5	mA	With Charge Pump Disabled
A_{LO} Voltage	–4	–5	–5.25	V	With Charge Pump Disabled

NOTES
[1]Refers to the delay between receipt of a conversion command via the serial interface, and the actual start of the signal integration period.
[2]In the intended modes of operation, as described in this data sheet and accompanying applications literature, these errors and drifts are reduced to negligible levels via firmware techniques.

Specifications subject to change without notice.

Timing Characteristics

Parameter	Min	Typ	Max	Units	Notes
t_{CESK}	50			ns	Chip Enable to Shift Clock Delay, or Shift Clock to Chip Enable Setup
t_{DISU}	20			ns	Data Input Setup Time
t_{SKL}	20			ns	Shift Clock Low Time
t_{SKH}	20			ns	Shift Clock High Time
t_{DIH}	0			ns	Data Input Hold Time
t_{SKDV}			20	ns	Shift Clock to Data Valid Time
t_{DREL}			20	ns	Data Release Time
f_{CLK}			20	MHz	Clock Speed

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AVDD	AGND	–0.3	+6.5	V
AVDD	DGND	–0.3	+6.5	V
DVDD	AGND	–0.3	+6.5	V
DVDD	DGND	–0.3	+6.5	V
AGND	DGND	–0.3	+0.3	V
ALO	AGND	–0.3	+6.5	V
ALO	DGND	–0.3	+6.5	V
AIN0–3	AGND	–12	+12	V
EXC0–3	AGND	–12	+12	V
REFIN	AGND	–0.3	AVDD + 0.3	V
DIN0–3	DGND	–0.3	DVDD + 0.3	V
DOUT0–3	DGND	–0.3	DVDD + 0.3	V
GND SNS, CJCIN, REFOUT, PGAOUT, ISET, CINT1–2, C1–3	AGND	–0.3	+6.5	V
CPE, XTAL1–2, XTALOUT, RESET, DRDY, DI, DO, $\overline{CE}$, SK	DGND	–0.3	+6.5	V
Storage Temperature		–65	+150	°C
Junction Temperature			+175	°C
Lead Temperature (Soldering, 10 sec)			+300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD280BS	–25°C to +85°C	44-Lead Metric Plastic Quad Flatpack (MQFP)	S-44
AD280-EB		Evaluation Kit	

THERMAL CHARACTERISTICS

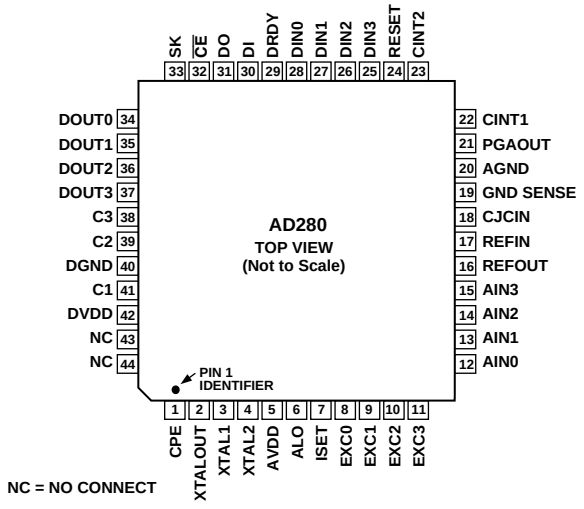
Thermal Resistance

44-Lead MQFP

θ_{JA} = 53.2°C/W

θ_{JC} = 19°C/W

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD280 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin #	Pin Name	Description
1	CPE	Charge Pump Enable. When tied to a Logic "1," enables the internal charge pump within the AD280, allowing single supply operation.
2	XTALOUT	Buffered Output from the Crystal Oscillator.
3	XTAL1	Connection for External Crystal.
4	XTAL2	Connection for External Crystal.
5	AVDD	Positive power supply connection for analog circuit; nominally +5 V ± 5%.
6	ALO	Negative Power Supply Connection; tied externally to C3 (Pin 38) Nominally –5 V ± 5% supplied externally if charge pump is not used (see Pin 1)
7	ISET	Connection for external resistor, which sets the magnitude of the current used for RTD excitation.
8, 9, 10, 11	EXC0–EXC3	Excitation outputs used to supply open circuit detection current (all four) or RTD excitation current (EXC0 and EXC1 only).
12–15	AIN0–AIN3	Analog Input Channels; single-ended inputs with respect to analog ground.
16	REFOUT	Reference Voltage Output. Nominally +2.5 V.
17	REFIN	Reference Voltage Input. Nominally connected to REFOUT.
18	CJCIN	Cold Junction Compensation Sensor Input. Can be connected to a thermistor or silicon temperature sensor for TC applications.
19	GND SENSE	Ground Sense Input. Used for measuring ground to compensate for ground loops or other offsets.
20	AGND	Analog Ground. All input signals are referenced to this pin.
21	PGAOUT	Output of the Programmable Gain Amplifier; supplied primarily for test and diagnostic purposes.
22, 23	CINT1, CINT2	Connection for External Integration Capacitor; Nominally 4.7 nF.
24	RESET	Reset Input to Internal Logic. When at Logic "0," forces internal logic into the command mode condition. Normally connected to a power-up reset circuit or RC reset circuit.
25–28	DIN3–DIN0	General purpose digital inputs, accessible via the serial interface.
29	DRDY	Data Ready Output. When at Logic "1," indicates that the most recent A/D conversion is complete and that data is available. This signal is also available via the serial interface, located in the status byte.
30	DI	Data Input for the Serial Interface.
31	DO	Data Output from the Serial Interface. In a three-state condition unless a data read command is being executed.
32	$\overline{CE}$	Chip Enable Input. This signal is used to frame each byte of a command or data transfer.
33	SK	Shift Clock Input. This signal clocks data to/from the AD280 via the serial interface.
34–37	DOUT0–DOUT3	General purpose digital inputs, accessible via the serial interface.
38	C3	Connection for the shunt capacitor required by the charge pump circuit (nominally 1 μF/10 V tantalum, low ESR (Effective Series Resistance), negative terminal connected to Pin 38).
39, 41	C2, C1	Connections for the series capacitor required by the charge pump (nominally 1 μF/10 V tantalum, low ESR (Effective Series Resistance), negative terminal connected to Pin 39).
40	DGND	Digital Ground.
42	DVDD	Power supply input for digital portion of the AD280. Nominally +5 V ± 5%.

FUNCTIONAL DESCRIPTION

The AD280 is a multifunction front end building block IC intended for applications in the industrial instrumentation and data acquisition fields. It contains an input multiplexer, PGA, A/D converter, excitation sources and serial interface, all optimized for the measurement of RTDs, thermocouples, volt and millivolt signals commonly found in industrial control environments. When used with a microcontroller and the appropriate closed loop algorithms and firmware, the AD280 can support up to four thermocouple (or millivolt or voltage) inputs, or up to 2 RTDs operating in either the 3-wire or 4-wire mode. The AD280 contains additional provisions for cold junction compensation of thermocouples, open lead detection and input protection from normal-mode faults.

Figure 1 illustrates an example application, utilizing the AD280 along with a microcontroller to create a two-chip, four-channel industrial signal conditioner with serial communications.

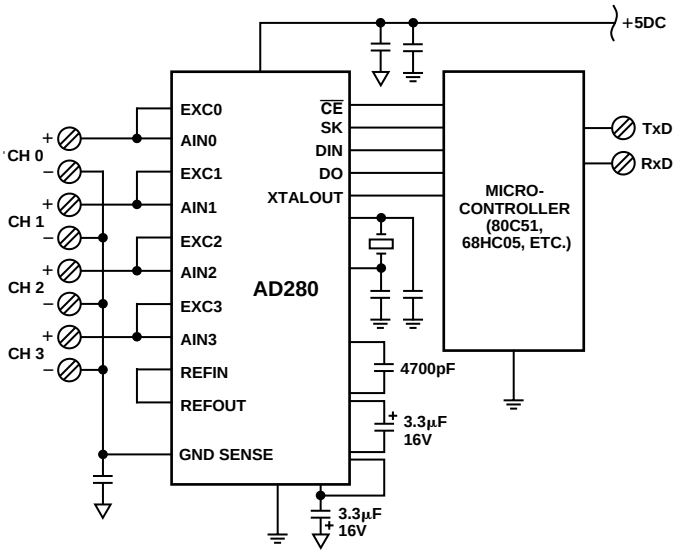


Figure 1. An Example Application

INPUT MULTIPLEXER

The AD280 contains an input multiplexer primarily designed to support four input channels, along with additional channels for measurement of ground, reference, a CJC sensor and a built-in PTAT signal. Each of the input channels (AIN0 through AIN3) constitutes a high input impedance (>20 MΩ) input for signals of up to ±3 volts, with series limiting resistance and an active clamping structure. The input terminals are specifically designed to allow for input overloads of up to ±11 volts without affecting the operation of any other channel.

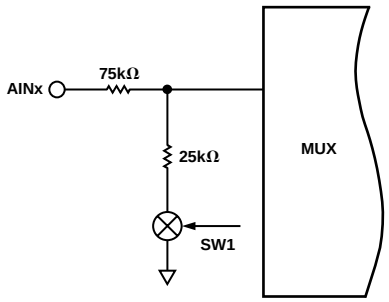


Figure 2. Input Attenuator Structure

Under program control, the inputs can be reconfigured as attenuated inputs. When enabled (by activating SW1 as shown in Figure 2), the input impedance drops to approximately 100 kΩ, and the linear input range therefore expands to ±10 volts via a 4:1 attenuator. Using this provision, the AD280 can be used to measure signals of up to ±10 volts without additional external components. A specialized ESD protection circuit at each signal input pin will clamp at approximately ±11 volts; protection for input voltages higher than this level can be achieved via the use of external series input resistors.

Table I. Multiplexer Control Bits

Input	PGA2	PGA1	PGA0
AIN0	0	0	0
AIN1	0	0	1
AIN2	0	1	0
AIN3	0	1	1
GND SENSE	1	0	0
PTAT	1	0	1
CJC	1	1	0
VREF	1	1	1

The input multiplexer also provides inputs dedicated to measuring both analog ground and the reference voltage; these inputs are provided to facilitate the use of closed loop autocalibration algorithms. The ground sense input has an internal series resistor, in order to balance the effects of bias current at the inputs. The multiplexer also provides an input designed for use in cold junction compensation for thermocouple applications. This input has a programmable excitation source, providing appropriate excitation for a 10 kΩ interchangeable thermistor. The excitation may be deactivated under digital control, allowing the input to be used for semiconductor temperature sensors such as the AD22100 or AD590.

The multiplexer also connects to an internal PTAT sensor, which may be used to sense and track the internal temperature of the die. While not practical for cold junction calibration purposes, this signal might be used for diagnostic purposes in some designs.

OSCILLATOR

The AD280 requires a clock signal for operating the internal charge balancing A/D converter, and for operating the optional internal charge pump used in single supply applications. The clock frequency affects the resolution of the A/D conversion process vs. the integration time; higher frequencies result in higher resolution. An internal oscillator allows for the connection of a crystal, and optionally allows for an externally derived clock.

The oscillator is a parallel resonant design known as a "Pierce" oscillator, and is similar to those found on most microcontrollers. Two external shunt capacitors are required to complete the circuit, as shown in Figure 2. The value of the capacitors and the tolerance of the crystal affect clock speed accuracy, although very precise clock speed is not required in most applications. For crystals in the 10 MHz to 12 MHz range, 22 pF capacitors are usually appropriate.

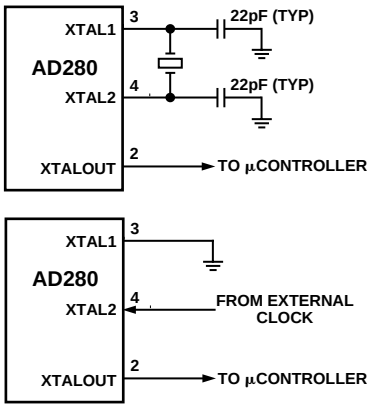


Figure 3. Oscillator Connections

To drive the AD280 from an externally derived clock, XTAL1 should be grounded, and the external clock should be applied to the XTAL2 pin.

The XTALOUT pin provides a buffered replica of the clock. This signal can be used to drive the clock input of a microcontroller, as shown in the applications diagram (Figure 1).

GROUND SENSE INPUT

The ground sense input is an analog input to the front end multiplexer, specifically designated for use in sensing (and thereby eliminating) ground offset errors in an AD280 application. While normally connected to AGND (Pin 20), this input can be used for "Kelvin sensing" at the reference terminal inputs of an application. Like the CJC input, this input is not designed for use as a field terminal input, and lacks the input protection features found in AIN0 through AIN3. In most applications, the voltage on the ground sense input will be periodically sampled, and the resulting data used to compensate the input signal data for offset.

COLD JUNCTION COMPENSATION INPUT

The AD280 provides an input explicitly for connection to a cold junction compensation temperature sensor. This input is a standard input to the front end multiplexer, but with the addition of a programmable excitation designed for use with thermistor temperature sensors.

When enabled, the input is connected to a 34.4 kΩ resistor (factory trimmed for value) which, in turn, is connected to the reference voltage. This kind of excitation is ideal for use with 10 kΩ nominal precalibrated thermistors such as the Betatherm 10KA3. The 34.4 kΩ resistor serves to help linearize the thermistor voltage, although further digital linearization is required for most applications. When disabled, the excitation circuit is effectively disconnected from the input.

This input may also be used with a wide variety of silicon temperature sensors, such as the AD590 or AD22100 series components, using the REFOUT pin as a source of bias. Furthermore, if no temperature sensor is required, this input may be used as an additional analog input for any desired purpose. This input does NOT exhibit the extended input voltage protection features found in AIN0 through AIN3.

EXCITATION CURRENT OUTPUTS

The AD280 contains four excitation output pins programmable for excitation level. These pins are separate from the analog input pins to allow for the use of protection devices in environments with the possibility of high level normal-mode fault conditions.

Table II. Excitation Control Bits

Output	MSB	LSB
OFF	0	0
+25 nA	0	1
–25 nA	1	0
RTD	1	1

All four excitation outputs can be individually programmed (via the serial interface) to supply either +25 nA or –25 nA for use in open circuit detection. All four may also be individually disabled. EXC0 and EXC1 may also be programmed for a higher excitation current, the magnitude of which is determined by the value of the I_{SET} resistor attached to Pin 7.

These excitation sources are implemented as high impedance current sources, with compliance to ±2.5 volts with respect to analog ground. In applications that do not require extended normal-mode voltage protection, they may simply be connected to their corresponding input signal pins (i.e., EXC0 connects to AIN0, EXC1 to AIN1, etc.) and will not interfere with signal measurement.

SETTING THE EXCITATION CURRENT LEVEL

The magnitude of the excitation current used for RTD sensors is set via a resistor connected between the I_{SET} pin and analog ground. This resistor sets the high level excitation magnitude for both EXC0 and EXC1, but has no effect on the open circuit detection current outputs of any of the EXC pins. The formula for determining the approximate excitation current is:

$$I_{EXC} = (2.5/R_{ISET}) \times 4$$

The temperature coefficient of the excitation current is directly affected by the TC of this resistor, so it is suggested that a high stability resistor (10 ppm/°C or less) be used. The total drift of the excitation source will not only include the drift of this resistor, but the reference drift as well.

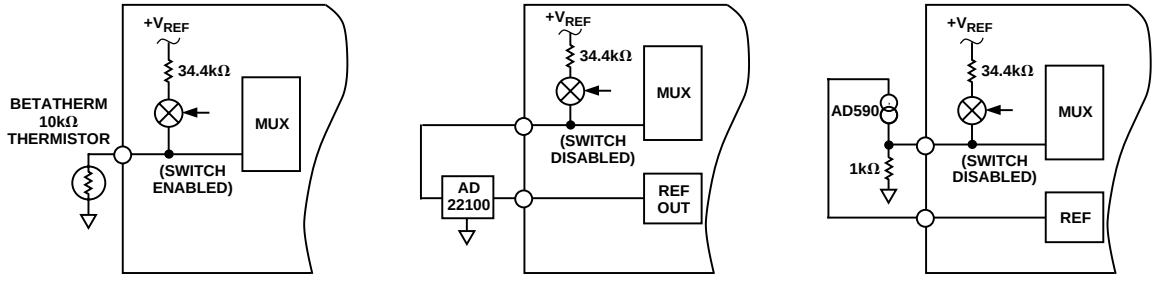


Figure 4. CJC Sensor Connections

The excitation current level can be set for any value up to 2 mA; however, it is suggested that the lowest practical level be used to minimize self-heating and general power dissipation. A good value for most 100 Ω platinum or nickel RTD types is 250 μA; higher currents (up to 2 mA) are usually used only for copper RTDs. If the high level excitation feature will not be used, this pin may be left open.

AUXILIARY DIGITAL INPUTS AND OUTPUTS

The AD280 provides for four general purpose digital inputs, and four general purpose digital outputs. These inputs and outputs are accessed via the serial interface, and can be used for any desired purpose. Some of the applications for these I/O pins include controlling external excitation circuits for specialized transducers, or for activating or monitoring other external devices. The general purpose outputs have a limited drive capability, sufficient for driving CMOS logic inputs; in some applications it may be necessary to buffer these outputs with external devices.

REFERENCE INPUT AND OUTPUT

The AD280 contains an internal bandgap reference voltage generator, the output of which is connected to Pin 16 (REFOUT). The reference is nominally +2.5 V. In most applications, it should be connected to REFIN, Pin 17. For applications requiring better stability than that provided by the internal reference, the REFOUT pin may be left unconnected and the REFIN pin may be driven from an external reference source such as the AD685.

The REFOUT signal may also be useful to drive external circuitry in some applications. Up to 1 mA may be drawn from this pin for external use.

PGA OUTPUT

The output of the Programmable Gain Amplifier is brought out to this pin, primarily for the purposes of diagnostics and testing, although there may be applications where it can be utilized. The nominal output swing of this pin is ±2.5 V, with a typical linear overrange capability to ±3 V.

EXTERNAL INTEGRATION CAPACITOR

The charge balancing A/D converter within the AD280 requires an external integration capacitor, connected to CINT1 and CINT2 (Pins 22 and 23). The nominal value of this capacitor is 4.7 nF. The value is not especially critical, so loose tolerance types (±20%) may be employed. The dielectric characteristics of this capacitor have relatively little effect on the performance or accuracy of this type of A/D converter, so expensive film capacitors are unnecessary; inexpensive ceramic types (NPO or X7R dielectrics) will suffice.

RESET INPUT

The RESET input to the AD280 is used to initialize the state of the serial interface. When brought low, this signal will place the serial interface into a "command" state, where it is ready to accept a command. The RESET input also has the effect of terminating an A/D conversion cycle in progress, and resetting the A/D converter control circuitry. This input may be driven from an external microcontroller supervisory circuit, or can be connected to a simple RC reset circuit.

The RESET input is not absolutely required, and is provided for convenience. If it is not used, the serial interface can be forced into the command state by shifting at least four consecutive bytes whose values are "0"s into the DI pin of the serial interface. The internal configuration registers can only be initialized through the interface, and are *not* cleared or reset by the RESET pin.

DRDY (DATA READY) OUTPUT PIN

The DRDY pin indicates the state of the A/D converter. When low, it indicates that an A/D conversion is in progress; when high, it indicates that a conversion is complete, and that the data from the most recent conversion is available over the serial interface. This pin replicates a signal that is also available for inspection via the serial interface; it is brought out as a separate pin in applications where it may be needed to trigger an interrupt.

ENHANCED PROTECTION

Although the AD280 is designed to provide protection to 10 volts beyond the power supply, there are many cases where significantly greater normal-mode overvoltage protection is required. The AD280 has been designed with this requirement in mind.

When operated in the high impedance mode (i.e., for input signals limited to ±3 volts), high normal-mode protection can be achieved through the use of large value series input resistors. The effect of the bias current present at the inputs to the AD280, working against a high external impedance, can be negated by balancing the inputs, i.e., always using a similarly valued resistance in series with the GND SENSE input.

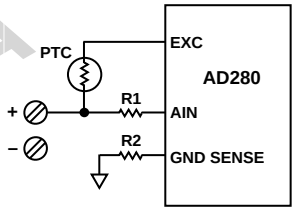


Figure 5. Enhanced Input Normal-Mode Protection via Large Value Input and Balancing Resistors and PTC Devices

It should be noted, however, that when employing high value series input resistors, it is advisable to avoid extra capacitance directly at the input terminals. The PGA's bias current is present at the inputs only when the multiplexer is addressed for that input; at other times, the input current falls to a negligible value, consisting of just the leakage current of the multiplexer itself. Relatively low values of capacitance at the input terminals will therefore begin to slowly charge from the bias current when the channel is selected, and discharge through the source impedance of the input signal when deselected. This charging/discharging behavior can cause large errors at very high gains.

The excitation sources may also be protected via the use of a simple external circuit as shown in Figure 5. In this example, a PTC (positive temperature coefficient) protection element is used to protect the excitation source. When used together with a high value external resistor to protect the input pin, complete protection for a universal input (TC, RTD, mV or V) can be afforded.

CHARGE PUMP

The AD280 contains an internal charge pump circuit, which eliminates the need for a negative power supply voltage. The charge pump operates at 1/64th of the clock frequency. Because of clock noise and the high current spikes generated by any charge pump, it can be expected that the use of the charge pump will somewhat degrade the performance (accuracy and resolution) of the AD280; for the most stringent and demanding applications, an external negative supply is preferred.

The charge pump requires the use of two external capacitors, as shown in Figure 6. One of these capacitors is a shunt element, and is connected from Pin 38 to ground. The other is a series element, and is connected between Pin 39 and Pin 41. These capacitors should be low ESR Tantalum types for the lowest supply ripple and best performance; standard tantalum types, or most aluminum types, should be avoided. A suggested capacitor value is 3.3 μF, although the charge pump is unconditionally stable, and larger values may be used.

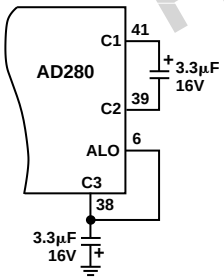


Figure 6. Charge Pump Connections

INTERFACE EXAMPLES

Figure 7 is an example of how the AD280 can be configured to accept an array of input configurations for thermocouples, RTD's, millivolt and voltage inputs. In this example, the excitation sources are connected in such a way that just EXC0 and EXC1 would be enabled for the RTD interconnect, but all four could be enabled at the +25 nA or –25 nA level for open lead detection. Although not shown, it would also be quite possible to connect a single RTD and two other single-ended inputs, such as thermocouples, millivolt or voltage signals.

SERIAL PERIPHERAL INTERFACE

The AD280 features a Serial Peripheral Interface (SPI) that enables bidirectional half duplex communication with a microcontroller or microcomputer. The interface consists of five signals:

$\overline{CE}$	Chip Enable (Active Low)
DI	Data Input
DO	Data Output
SK	Shift Clock
DRDY	Data Ready

Since the DO pin will always be three-stated, except during a "read" command, it may be tied to DI (Data Input) in applications where the microcontroller or other interface circuitry can be operated bidirectionally.

The DRDY signal is a duplication of the DRDY bit in the status byte. It is provided as an external pin in applications where a signal is required to generate an interrupt at the end of the conversion cycle.

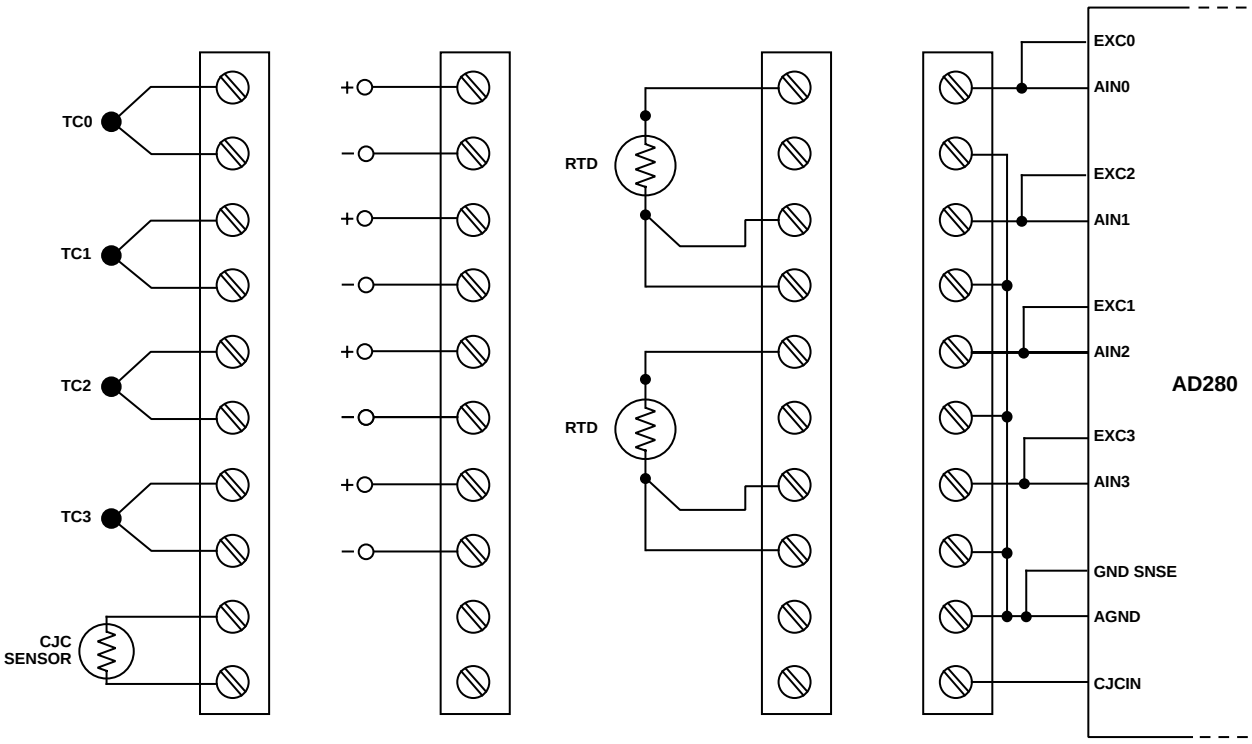


Figure 7. Example of "Universal" Input Connection Arrangement for the AD280

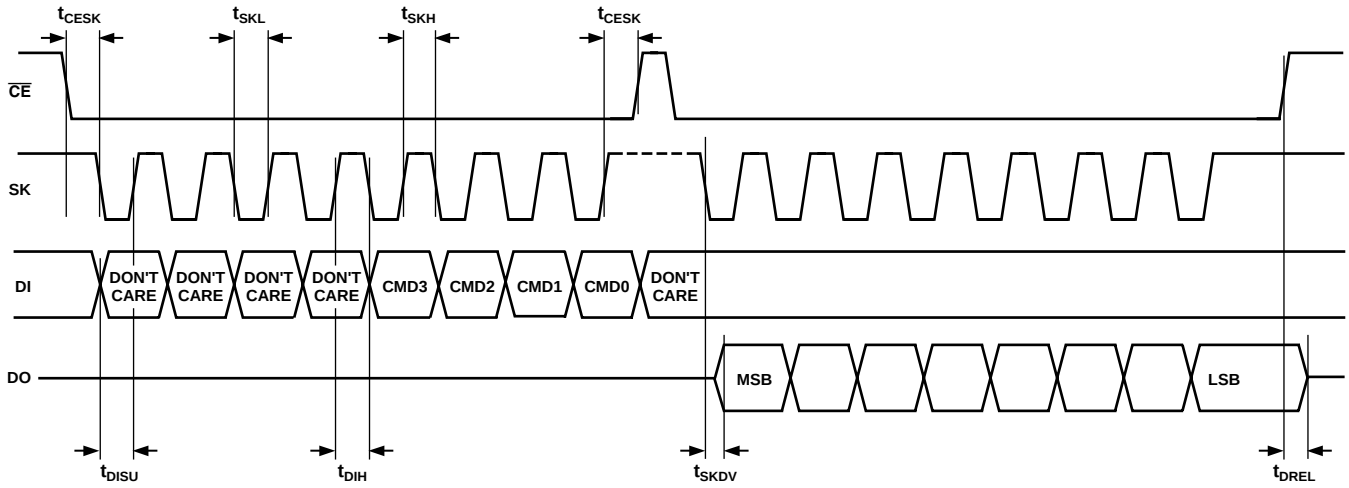


Figure 8. Read Cycle

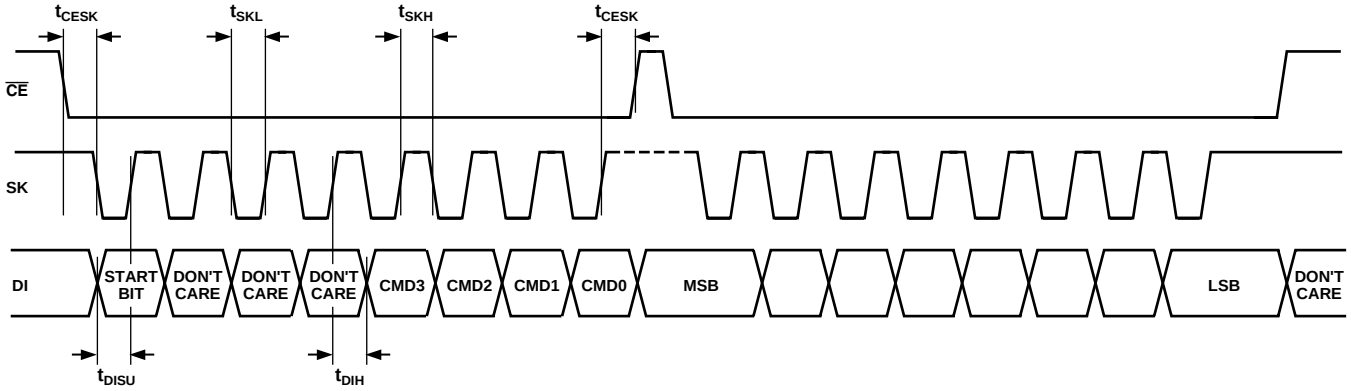


Figure 9. Write Cycle

All communications with the AD280 are composed of byte transfers. Each byte transfer is bracketed by the dropping of the $\overline{CE}$ line, and the SK input is used to shift data in and out of the device. Input data is clocked in on the rising edge of SK, and output data is valid at the falling edge of SK. *Note that SK must be high at both the rising and falling edges of $\overline{CE}$.*

There are six "write" registers and four "read" registers within the AD280, as shown in Figure 10. To initiate a communication sequence, the microcontroller, which contains a 4-bit command code, writes a command byte to the AD280. The AD280 command register (CMD) is the first of the six "write" registers. It will be loaded with the 4-bit command code that determines the type of communication, and the number of bytes in the communication sequence.

Table III shows the possible command codes. After RESET, the AD280 will be in "command mode," where it expects to receive a command byte from the microcontroller. If the command code specifies a "write" sequence, the microcontroller will then transmit one or more parameter bytes to the AD280. If the command code specifies a "read" sequence, the microcontroller will receive one or more parameter bytes from the AD280. The only exception is the "start conversion" command code, which requires no data bytes. An undefined command code will be treated as a NOP (no operation) and ignored.

If a communications sequence is interrupted, the AD280 may get stuck waiting for a data transfer that never occurs. There are two ways to force the AD280 back into "command mode": one is to activate the RESET IN signal and the other is to write four consecutive bytes with all bits set to "0."

There are five "write" registers which constitute configuration parameters. The two lowest bytes (CFG0 and CFG1) contain the 16-bit binary integer value that determines the length of integration time for A/D conversions. The next byte, CFG2, contains four bits to control the input attenuation for each channel and four bits to drive the auxiliary digital output signals. CFG3 contains three bits to control the multiplexer, three bits to control the programmable gain amplifier, and one bit for CJC excitation. CFG4 contains eight bits to control the excitation sources.

When written, the contents of these bytes will be latched and will hold their values until overwritten with new values. At power-up, the contents of these latches will be undefined. They must be loaded before an A/D conversion can be performed. Any attempt to write to these latches during the course of an A/D conversion will cause the conversion to be aborted. The write cycle will, however, be considered valid and the data will be latched.

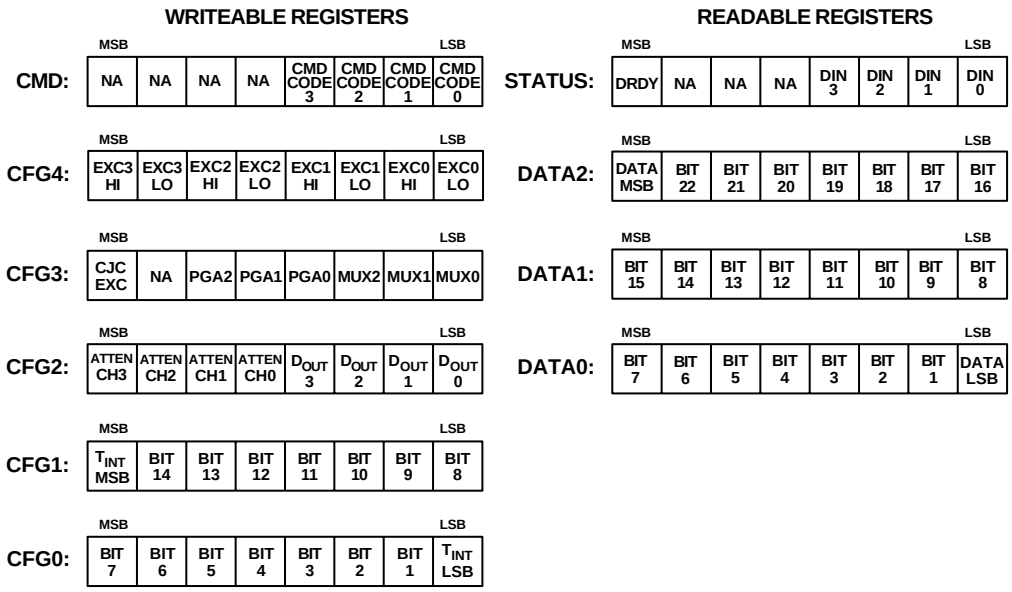


Figure 10. AD280 Internal Registers

Table III. Command Codes and Corresponding Functions

Command Code CC3	CC2	CC1	CC0	Function	Parameter
0	0	0	0	NO OPERATION	None
0	0	0	1	READ STATUS	1
0	0	1	0	READ DATA0	1
0	0	1	1	READ DATA1	1
0	1	0	0	READ DATA2	1
0	1	0	1	READ DATA0/DATA1/DATA2	3
0	1	1	0	NO OPERATION	None
0	1	1	1	NO OPERATION	None
1	0	0	0	WRITE CFG0	1
1	0	0	1	WRITE CFG1	1
1	0	1	0	WRITE CFG0/CFG1	2
1	0	1	1	WRITE CFG2	1
1	1	0	0	WRITE CFG3	1
1	1	0	1	WRITE CFG4	1
1	1	1	0	WRITE CFG2/CFG3/CFG4	3
1	1	1	1	START CONVERSION	None

The four "read" registers in the AD280 consist of three data bytes (DATA0, DATA1, DATA2) and a STATUS byte. The three data bytes constitute a 24-bit twos-complement binary integer that is proportional to the signal data. The status byte contains the auxiliary digital input data, along with an image of the DRDY signal, which is a copy of the separate external DRDY line.

The data bytes and status byte may be read at any time. If read during an A/D conversion, the data bytes will contain the results of the LAST conversion completed. They will not be updated with the NEW conversion data until the next conversion is complete. The user is responsible for reading the data when it is valid. The data is valid after one conversion is complete (i.e., when DRDY goes high), and remains valid until the next conversion is complete. The data must be read early enough in the conversion cycle to assure that it is not updated during the data transfer. Normally, it is most efficient to use the following sequence:

1. Wait for the conversion to complete.
2. Set the configuration parameters for the next conversion.
3. Wait for settling of the MUX and PGA (1 mS max). Read the data from the previous conversion while waiting.
4. Trigger the A/D for the next conversion.

All AD280 registers may be read or written in a "single byte" mode by using the appropriate commands. In the single byte mode, the command code specifies which individual register is to be read or written. The byte must be read or written immediately after the command code is sent to the AD280.

In addition to byte-at-a-time access, "multiple byte" mode allows certain register combinations to be read or written without the need to transmit a command byte for each register. The command code specifies the number of bytes that follow. Up to three bytes of data, in ascending order, may be transferred after the command byte. This capability substantially reduces the time required to access the AD280, since in most cases the register groupings will always be read or written together. It is important to note that in all cases, regardless of whether single or multiple byte mode is used, each byte transferred will require the complete sequence of the $\overline{CE}$ (Chip Enable) and SK (Shift Clock) pins.

SETTING THE A/D INTEGRATION PERIOD

The integration period of the AD280's A/D converter is set by writing to the CONFIG0 and CONFIG1 registers. These two bytes constitute a 16-bit binary integer which represents the upper 16 bits of a 21-bit counter clocked by the AD280's clock. The formula for the integration period is:

$$D_{CONFIG0/1} = (F_{CLK} \times T_{INT})/32$$

where $D_{CONFIG0/1}$ represents a 16-bit integer. For example, when using a 10 MHz clock frequency, and when an integration period of 16.666 ms is desired, the required integer is 5209_{10}, or 1459_{16}. Practical integration periods range from 1 ms to 200 ms, depending upon clock speed.

The accuracy of the integration period is limited by the clock speed and resolution of the CONFIG0/1 registers; faster clock frequencies will result in more accurate integration periods, with corresponding improvement in normal mode rejection.

A/D RESOLUTION

The resolution of the A/D converter is dependent upon the integration period and the clock speed. For a given integration period, the nominal full-scale output of the A/D will be ±50% of the number of clock cycles that occur in the integration period. For example, a clock speed of 10 MHz and an integration period of 10 ms will produce an output of approximately ±50,000 counts. All ranges have an overrange capability of (typically) 20%, so the A/D will typically remain linear up to ±60,000 counts (in the example just illustrated). The exception to this overrange capability is when the attenuators are used to achieve a 10 V input range; in this case, the special ESD circuits will clamp the input at approximately ±11 volts, thereby reducing the overrange to 10%.

EVALUATION KIT

An evaluation kit, consisting of an evaluation board with an AD280 and support components is available (Part Number AD280-ED). This kit includes a software demo program written to operate under Windows® 95.

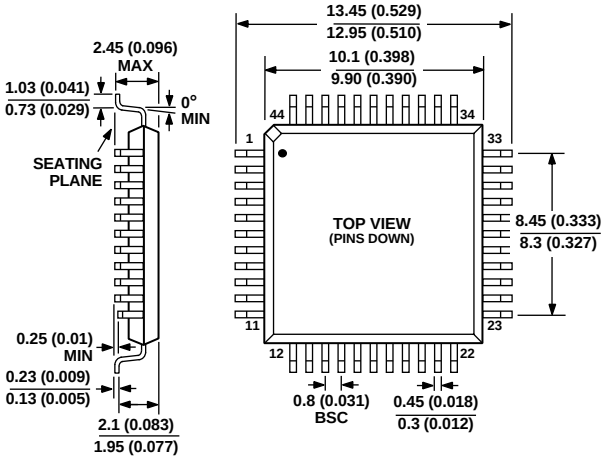
Windows is a registered trademark of Microsoft Corporation.

C3032–8–4/98

OUTLINE DIMENSIONS

Dimensions shown in mm and (inches).

44-Lead Metric Plastic Quad Flatpack (MQFP)
(S-44)



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