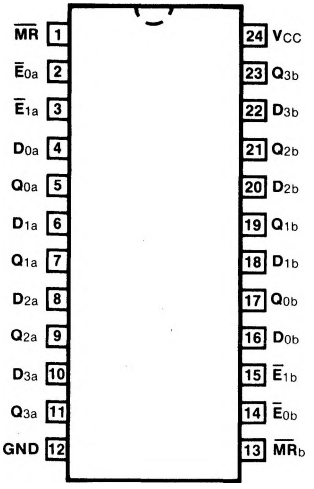
9308
93L08
DUAL 4-BIT LATCH

DESCRIPTION — The '08 is a dual 4-bit D-type latch designed for general purpose storage applications in digital systems. Each latch contains both an active LOW Master Reset input an active LOW Enable inputs. The 54/74116 is a pin for pin equivalent of the 9308.

CONNECTION DIAGRAM
PINOUT A



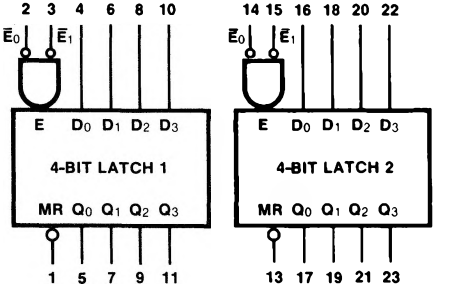
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9308PC, 93L08PC		9N
Ceramic DIP (D)	A	9308DC, 93L08DC	9308DM, 93L08DM	6N
Flatpak (F)	A	9308FC, 93L08FC	9308FM, 93L08FM	4M

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
D_{0a} — D_{3a} D_{0b} — D_{3b}	Parallel Latch Inputs	1.5/1.5	0.75/0.375
$\bar{E}_{0a}$, $\bar{E}_{1a}$, $\bar{E}_{0b}$, $\bar{E}_{1b}$	AND Enable Inputs (Active LOW)	1.0/1.0	0.5/0.25
$\overline{MR}_a$, $\overline{MR}_b$	Master Reset Inputs (Active LOW)	1.0/1.0	0.5/0.25
Q_{0a} — Q_{3a} Q_{0b} — Q_{3b}	Parallel Latch Outputs	20/10	10/5.0 (3.0)

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

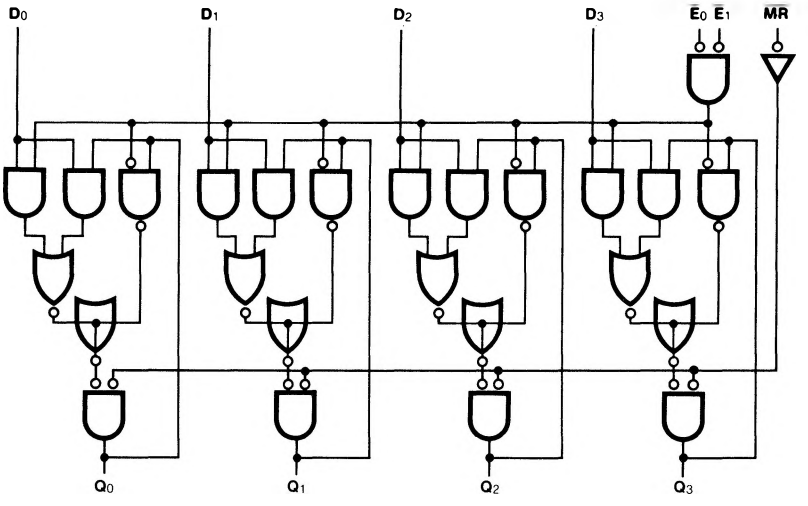
FUNCTIONAL DESCRIPTION — Data can be entered into the latch when both of the enable inputs are LOW. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes HIGH, the data present in the latch at that time is held in the latch and is no longer affected by data input. The master reset overrides all other input conditions and forces the outputs of all the latches LOW when a LOW signal is applied to the Master Reset input.

TRUTH TABLE

$\overline{MR}$	$\overline{E}_0$	$\overline{E}_1$	D	Q_n	OPERATION
H	L	L	L	L	Data Entry
H	L	L	H	H	Data Entry
H	L	H	X	Q_{n-1}	Hold
H	H	L	X	Q_{n-1}	Hold
H	H	H	X	Q_{n-1}	Hold
L	X	X	X	L	Reset

Q_{n-1} = Previous Output State
Q_n = Present Output State
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		100		29	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		C_L = 15 pF, R_L = 400 Ω		C_L = 15 pF			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_n$ to Q_n		30 22		45 38	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n		15 18		27 29	ns	Figs. 3-1, 3-5
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		22		30	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H)	Setup Time HIGH, D_n to $\overline{E}_n$	10		8.0		ns	Fig. 3-13
t_h (H)	Hold Time HIGH, D_n to $\overline{E}_n$	-2.0		0		ns	
t_s (L)	Setup Time LOW, D_n to $\overline{E}_n$	12		18		ns	Fig. 3-13
t_h (L)	Hold Time LOW, D_n to $\overline{E}_n$	8.0		4.0		ns	
t_w (L)	$\overline{E}_n$ Pulse Width LOW	18		30		ns	Fig. 3-21
t_w (L)	$\overline{MR}$ Pulse Width LOW	18		32		ns	Fig. 3-16
t_{rec}	Recovery Time, $\overline{MR}$ to $\overline{E}_n$	8.0		10		ns	Fig. 3-16