DESCRIPTION

The 8T10 is a high speed Quad D flip-flop with tri-state outputs for use in bus-organized systems. The high current sink capability permits up to 20 standard loads to be interconnected on a single bus. The outputs present a high impedance to the bus when disabled (Control Input "1") and active drive when enabled (Control Inputs "0").

All four D-type flip-flops operate from a common clock with data being transferred on the low-to-high transition of the pulse.

A common clear input resets all flip-flops upon application of a logic "1" level.

Data will be stored if either one or both inputs to the Input Disable NOR gate is a logic "1".

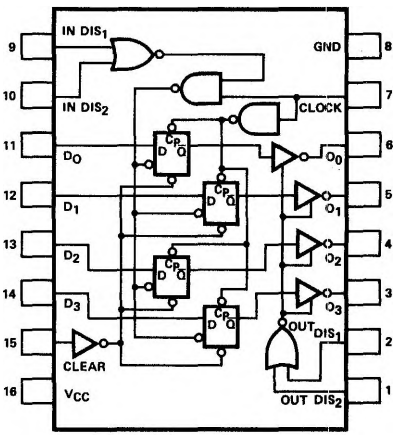
TRUTH TABLE

D_n	IN_{DIS}	OUT_{DIS}	0_{n+1}
0	0	0	0
1	0	0	1
X	1	0	0_n
X	X	1	High Z

0_n refers to the output state before a clock pulse.

0_n + 1 refers to the output state after a clock pulse.

LOGIC DIAGRAM



V_{CC}=16
GND=8

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS								NOTES
	MIN.	TYP.	MAX.	UNITS	D_n	IN DIS 1	IN DIS 2	OUT DIS 1	OUT DIS 2	CLEAR	CLOCK	OUTPUT	
"1" Output Voltage	2.4	3.0		V	2.0V	0.8V	0.8V	0.8V	0.8V	0.8V	Pulse	-5.2mA	6
"0" Output Voltage			0.4	V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	Pulse	32mA	7
Output Leakage Current (High Impedance State)	-40		+40	μA		0.8	0.8V	+2.0V	+2.0V	0.8V	Pulse	+0.4V/ +2.4V	
"1" Input Current													
D_n Inputs			40	μA	4.5V	0.4V	0.4V	0.4V	0.4V	0.4V			
All Other Inputs			50	μA		4.5V	4.5V	4.5V	4.5V	4.5V	4.5V		
"0" Input Current													
D_n Inputs	-.100		-3.2	mA	0.4V								
All Other Inputs	-.100		-2.0	mA		0.4V	0.4V	0.4V	0.4V	0.4V	0.4V		
Input Voltage Rating	+5.5V				10mA	10mA	10mA	10mA	10mA	10mA	10mA		

T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS								NOTES
	MIN.	TYP.	MAX.	UNITS	D_n	IN DIS 1	IN DIS 2	OUT DIS 1	OUT DIS 2	CLEAR	CLOCK	OUTPUT	
Propagation Delay (t_{on}, t_{off})													
Clock to Output													
C_L = 30pf		18	25	ns									12
C_L = 300pf		24	35	ns									12
Disable to Output													
High Z to Logic 0, t_{pZL} State (C_L = 300pf)		20	30	ns									10, 12
Logic 0 to High Z, t_{pLZ} High Z (C_L = 300pf)		20	30	ns									11, 12
Clear to Output													
C_L = 30pf		15	22	ns									12
C_L = 300pf		21	30	ns									12
Set Up Time, t_{setup}													
Data	+5	-1		ns									12
Input Disable		−6	0	ns									12
Hold Time, t_{hold}													
Data		-1	+5	ns									12
Reset Pulse Width	15			ns									12
Clock Frequency	35	50		MHz									12
Clock Pulse Width													
Positive		8	12	ns									12
Negative		8	12	ns									12
Power/Current Consumption			619/	mW/mA	0.4V	0.4V	0.4V	4.5V	0.4V	0.4V	4.5V		8
Output Short Circuit Current	-40		118 -120	mA	4.5V	0.4V	0.4V	0.4V	0.4V	0.4V		0.0V	8, 9

NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. V_{CC} = 5.25V.
9. Not more than one output should be shorted at a time.
10. Measured to 1.5V level of output waveform.
11. Measured to 10% level of output waveform.
12. Refer to AC Test Circuits.

AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY t_{on}, t_{off} (CLOCK TO OUTPUT)

DATA SETUP TIME, t_{setup}

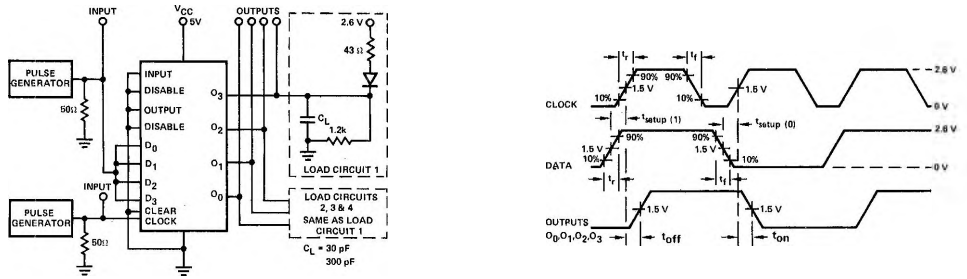


FIGURE 1

AC TEST CIRCUITS AND WAVEFORMS (Cont'd)

PROPAGATION DELAY (CLEAR TO OUTPUT)

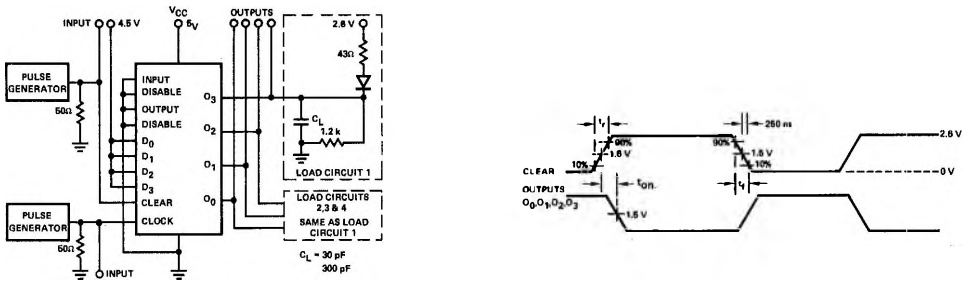


FIGURE 2

PROPAGATION DELAY (DATA HOLD TIME)

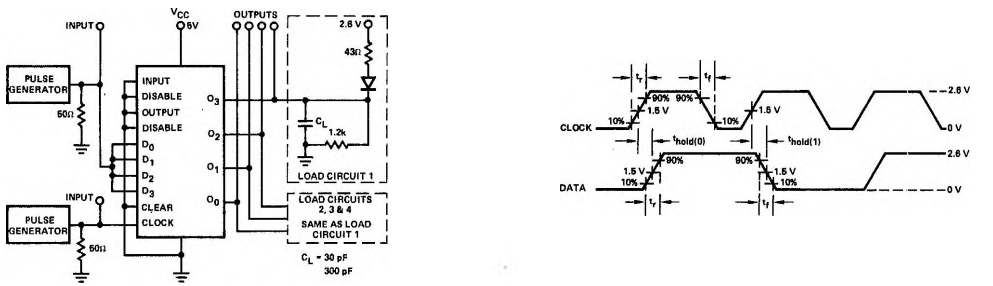


FIGURE 3

PROPAGATION DELAY (DISABLE TO OUTPUT)

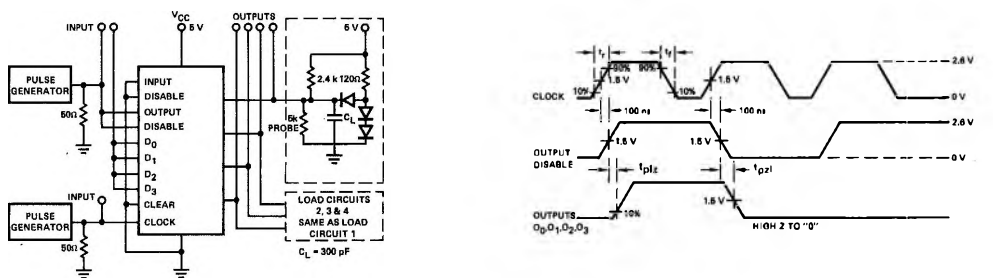
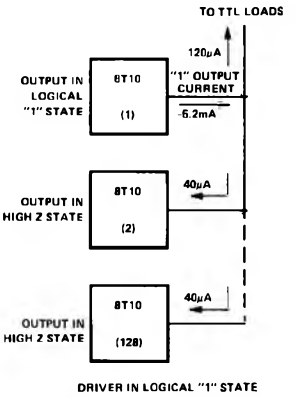
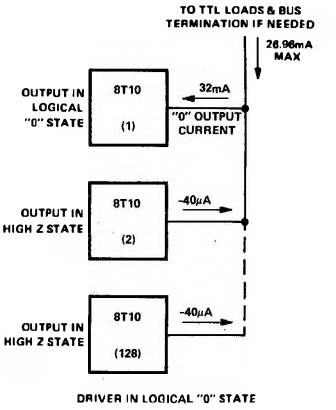


FIGURE 4

TYPICAL APPLICATIONS



DRIVER IN LOGICAL "1" STATE



DRIVER IN LOGICAL "0" STATE

MULTIPLEXING EIGHT LED DISPLAYS