8755
16,384 BIT EPROM WITH I/O

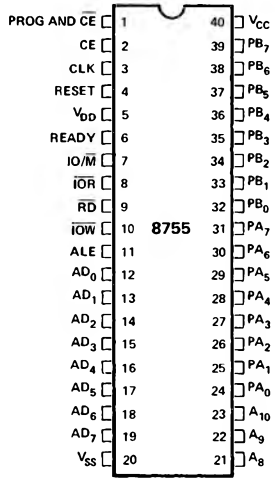
*Directly Compatible With 8085 CPU

- 2048 Words x 8 Bits
- Single +5V Power Supply (V_{CC})
- U.V. Erasable and Electrically Reprogrammable
- Internal Address Latch
- 2 General Purpose 8 bit I/O Ports
- Each I/O Port Line Individually Programmable as Input or Output
- Multiplexed Address and Data Bus
- 40 Pin DIP

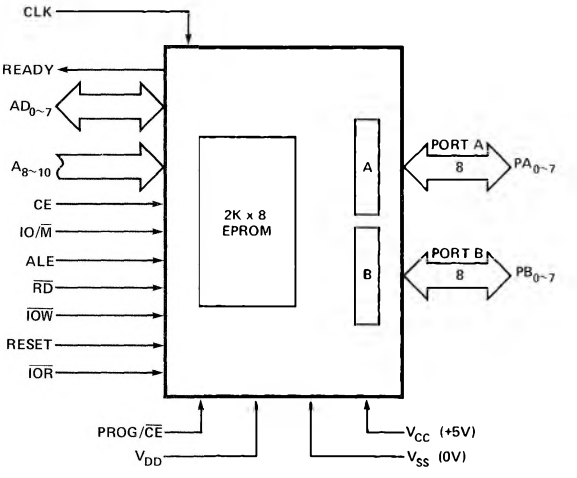
The 8755 is an erasable and electrically reprogrammable ROM (EPROM) and I/O chip to be used in the MCS-85™ microcomputer system. The PROM portion is organized as 2048 x 8. It has maximum access time of 400 ns to permit use with no wait states in 8085 CPU.

The I/O portion consists of two general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or output.

PIN CONFIGURATION



BLOCK DIAGRAM



8755 FUNCTIONAL PIN DESCRIPTION

Symbol	Function
ALE	When Address Latch Enable is high, AD_{0-7}, IO/$\overline{M}$, A_{8-10}, CE, and $\overline{CE}$ enter the address latches. The signals (AD, IO/M, A_{8-10}, CE) are latched in at the trailing edge of ALE.
AD_{0-7}	Bi-directional Address/Data bus. The lower 8-bits of the PROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B are selected based on the latched value of AD_0. If $\overline{RD}$ or $\overline{IOR}$ is low when the latched Chip Enables are active, the output buffers present data on the bus.
A_{8-10}	These are the high order bits of the PROM address. They do not affect I/O operations.
$\overline{CE}$/PROG CE	CHIP ENABLE INPUTS: $\overline{CE}$ is active low and CE is active high. Both chip enables must be active to permit accessing the PROM. $\overline{CE}$ is also used as a programming pin (see section on programming).
IO/$\overline{M}$	If the latched IO/$\overline{M}$ is high when $\overline{RD}$ is low, the output data comes from an I/O port. If it is low the output data comes from the PROM.
$\overline{RD}$	If the latched Chip Enables are active when $\overline{RD}$ goes low, the AD_{0-7} output buffers are enabled and output either the selected PROM location or I/O port. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD_{0-7} output buffers are tri-stated.
$\overline{IOW}$	If the latched Chip Enables are active, a low on $\overline{IOW}$ causes the output port pointed to by the latched value of AD_0 to be written with the data on AD_{0-7}. The state of IO/$\overline{M}$ is ignored.
CLK	The CLK is used to force the READY into its high impedance state after it has been forced low by $\overline{CE}$ low, CE high, and ALE high.
READY	READY is a 3-state output controlled by CE, $\overline{CE}$, ALE and CLK. READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK (see Figure 2.).
PA_{0-7}	These are general purpose I/O pins. Their input/output direction is determined by the contents of Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and $\overline{IOW}$ is low and a 0 was previously latched from AD_0. Read operation is selected by either $\overline{IOR}$ low and active Chip Enables and AD_0 low, or IO/$\overline{M}$ high, $\overline{RD}$ low, active Chip Enables, and AD_0 low.
PB_{0-7}	This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD_0.
RESET	In normal operation, an input high on RESET causes all pins in Ports A and B to assume input mode (clear DDR register).
$\overline{IOR}$	When the Chip Enables are active, a low on $\overline{IOR}$ will output the selected I/O port onto the AD bus. $\overline{IOR}$ low performs the same function as the combination of IO/$\overline{M}$ high and $\overline{RD}$ low. When $\overline{IOR}$ is not used in a system, $\overline{IOR}$ should be tied to V_{CC} ("1").
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.
V_{DD}	V_{DD} is a programming voltage, and it is normally grounded. For programming, a high voltage is supplied with V_{DD}, = 25V, typical.

FUNCTIONAL DESCRIPTION

PROM Section

The 8755 contains an 8-bit address latch which allows it to interface directly to MCS-48 and MCS-85 Microcomputers without additional hardware.

The PROM section of the chip is addressed by the 11-bit address and CE. The address, $\overline{CE}$ and CE are latched into the address latches on the falling edge of ALE. If the latched Chip Enables are active and IO/$\overline{M}$ is low when $\overline{RD}$ goes low, the contents of the PROM location addressed by the latched address are put out on the AD_{0-7} lines.

I/O Section

The I/O section of the chip is addressed by the latched value of AD_{0-1}. Two 8-bit Data Direction Registers determine the input/output status of each pin in the corresponding port. A 0 specifies an input mode, and a 1 specifies an output mode. The table summarizes port and DDR designation. Contents of the DDR's cannot be read.

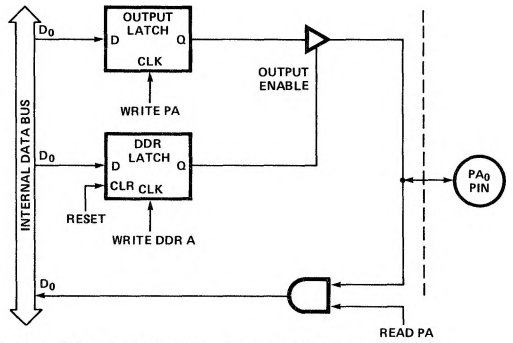
AD_1	AD_0	Selection
0	0	Port A
0	1	Port B
1	0	Port A Data Direction Register (DDR A)
1	1	Port B Data Direction Register (DDR B)

When $\overline{IOW}$ goes low and the Chip Enables are active, the data on the AD is written into I/O port selected by the latched value of AD_{0-1}. During this operation all I/O bits of the selected port are affected, regardless of their I/O mode and the state of IO/$\overline{M}$. The actual output level does not change until $\overline{IOW}$ returns high. (glitch free output).

A port can be read out when the latched Chip Enables are active and either $\overline{RD}$ goes low with IO/$\overline{M}$ high, or $\overline{IOR}$ goes low. Both input and output mode bits of a selected port will appear on lines AD_{0-7}.

To clarify the function of the I/O Ports and Data Direction Registers, the following diagram shows the configuration of one bit of PORT A and DDR A. The same logic applies to PORT B and DDR B.

8755
ONE BIT OF PORT A AND DDR A:



WRITE PA = ($\overline{IOW}$=0) • (CHIP ENABLES ACTIVE) • (PORT A ADDRESS SELECTED)
WRITE DDR A = ($\overline{IOW}$=0) • (CHIP ENABLES ACTIVE) • (DDR A ADDRESS SELECTED)
READ PA = {[(IO/$\overline{M}$=1) • ($\overline{RD}$=0)] + ($\overline{IOR}$=0)} • (CHIP ENABLES ACTIVE) • (PORT A ADDRESS SELECTED)

Note that hardware RESET or writing a zero to the DDR latch will cause the output latch's output buffer to be disabled, preventing the data in the Output Latch from being passed through to the pin. This is equivalent to putting the port in the input mode. Note also that the data can be written to the Output Latch even though the Output Buffer has been disabled. This enables a port to be initialized with a value prior to enabling the output.

The diagram also shows that the contents of PORT A and PORT B can be read even when the ports are configured as outputs.

ERASURE CHARACTERISTICS

The erasure characteristics of the 8755 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level flourescent lighting could erase the typical 8755 in approximately 3 years while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 8755 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8755 window to prevent unintentional erasure.

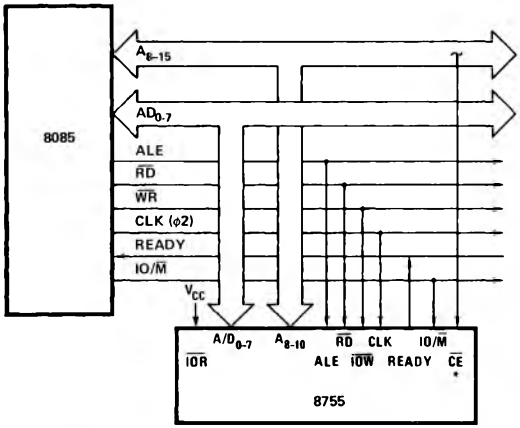
The recommended erasure procedure (see page 3-55) for the 8755 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000μW/cm^2 power rating. The 8755 should be placed within one inch from the lamp tubes during erasure. Some lamps have a filter on their tubes and this filter should be removed before erasure.

PROGRAMMING

Initially, and after each erasure, all bits of the EPROM portions of the 8755 are in the "1" state. Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The 8755 is programmed on the Intel® Universal PROM Programmer (UPP). The UPP and its related personality cards for the 8755 are described beginning on page 13-45 of the 1977 Intel Data Catalog.

SYSTEM APPLICATIONS



*USE $\overline{CE}$ FOR FIRST 8755 IN SYSTEM, AND CE FOR OTHERS. BY CONNECTING CE OF EACH 8755 CHIP TO EACH OF A_{11} THROUGH A_{15}, THE MINIMUM SYSTEM CAN USE 5-8755's (10K BYTES) WITHOUT REQUIRING CE DECODER.

FIGURE 1. 8755 IN 8085 SYSTEM (STANDARD I/O).

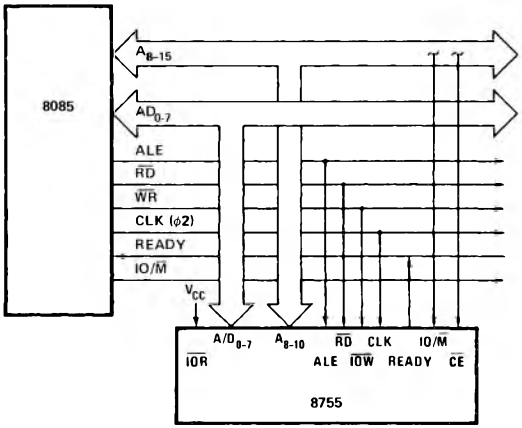


FIGURE 2. 8755 IN 8085 SYSTEM (MEMORY-MAPPED I/O).

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... -0.5V to +7V
Power Dissipation 1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{IL}	Input Leakage		10	μA	V_{IN} = V_{CC} to 0V
I_{LO}	Output Leakage Current		±10	μA	0.45V ≤V_{OUT} ≤V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	

A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{CYC}	Clock Cycle Time	320		ns	C_{LOAD} = 150 pF (See Figure 3)
T_1	CLK Pulse Width	80		ns	
T_2	CLK Pulse Width	120		ns	
t_f,t_r	CLK Rise and Fall Time		30	ns	
t_{AL}	Address to Latch Set Up Time	50		ns	150 pF Load
t_{LA}	Address Hold Time after Latch	80		ns	
t_{LC}	Latch to READ/WRITE Control	100		ns	
t_{RD}	Valid Data Out Delay from READ Control		150	ns	
t_{AD}	Address Stable to Data Out Valid		400	ns	
t_{LL}	Latch Enable Width	100		ns	
t_{RDF}	Data Bus Float after READ	0	100	ns	
t_{CL}	READ/WRITE Control to Latch Enable	20		ns	
t_{CC}	READ/WRITE Control Width	250		ns	
t_{DW}	Data In to WRITE Set Up Time	150		ns	
t_{WD}	Data In Hold Time After WRITE	0		ns	
t_{WP}	WRITE to Port Output		400	ns	
t_{PR}	Port Input Set Up Time	50		ns	
t_{RP}	Port Input Hold Time	50		ns	
t_{RYH}	READY HOLD TIME	0	120	ns	
t_{ARY}	ADDRESS (CE) to READY		160	ns	
t_{RV}	Recovery Time between Controls	300		ns	
t_{RDE}	Data Out Delay from READ Control	10		ns	

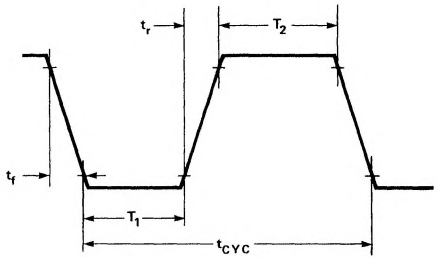


FIGURE 3. CLOCK SPECIFICATION FOR 8755

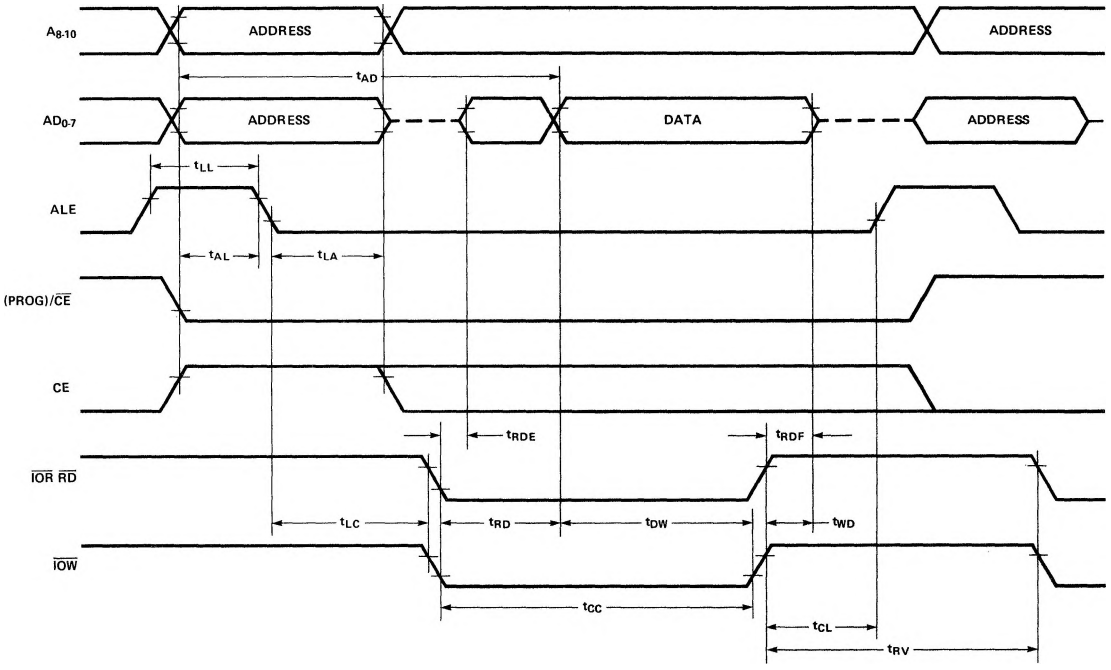
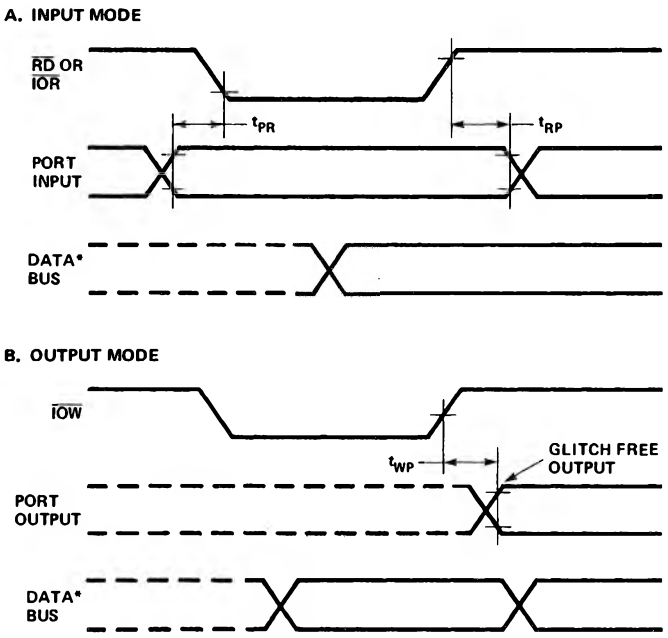


FIGURE 4. PROM READ, I/O READ, AND WRITE TIMING.

Please note that $\overline{CE1}$ must remain low for the entire cycle. This is due to the fact that the programming enable function common to this pin will disrupt internal data bus levels if $\overline{CE1}$ is taken high during the read.



*DATA BUS TIMING IS SHOWN IN FIGURE 4.

FIGURE 5. I/O PORT TIMING.

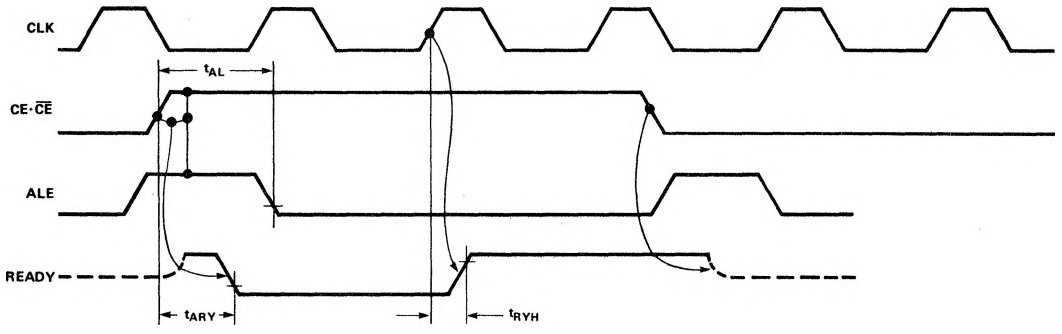


FIGURE 6. WAIT STATE TIMING (READY = 0).