signetics

1024-BIT BIPOLAR PROGRAMMABLE ROM (256x4 PROM)

82S126
82S129

FEBRUARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S126 (Open Collector Outputs) and the 82S129 (Tri-State Outputs) are Bipolar 1024-Bit Read Only Memories, organized as 256 words by 4 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S126 and 82S129 devices are supplied with all outputs at logical "0". Outputs are programmed to a logic "1" level at any specified address by fusing a Ni-Cr link matrix.

The 82S126 and 82S129 are fully TTL compatible, and include on-chip decoding and two chip enable inputs for ease of memory expansion. They feature either Open Collector or Tri-State outputs for optimization of word expansion in bussed organizations.

Both 82S126 and 82S129 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S126/129, B or F. For the military temperature range (−55°C to +125°C) specify S82S126/129, F only.

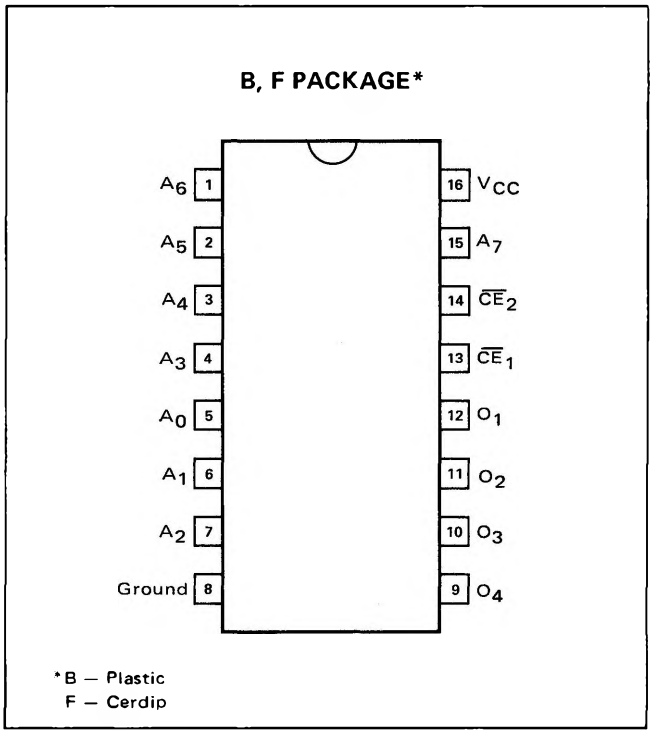
FEATURES

- **ORGANIZATION – 256 X 4**
- **ADDRESS ACCESS TIME:**
  S82S126/129 – 70ns, MAXIMUM
  N82S126/129 – 50ns, MAXIMUM
- **POWER DISSIPATION – 0.5mW/BIT TYPICAL**
- **INPUT LOADING:**
  S82S126/129 – (−150μA) MAXIMUM
  N82S126/129 – (−100μA) MAXIMUM
- **TWO CHIP ENABLE INPUTS**
- **ON-CHIP ADDRESS DECODING**
- **OUTPUT OPTION:**
  OPEN COLLECTOR – 82S126
  TRI-STATE – 82S129
- **NO SEPARATE "FUSING" PINS**
- **UNPROGRAMMED OUTPUTS ARE "0" LEVEL**
- **16-PIN CERAMIC DIP**

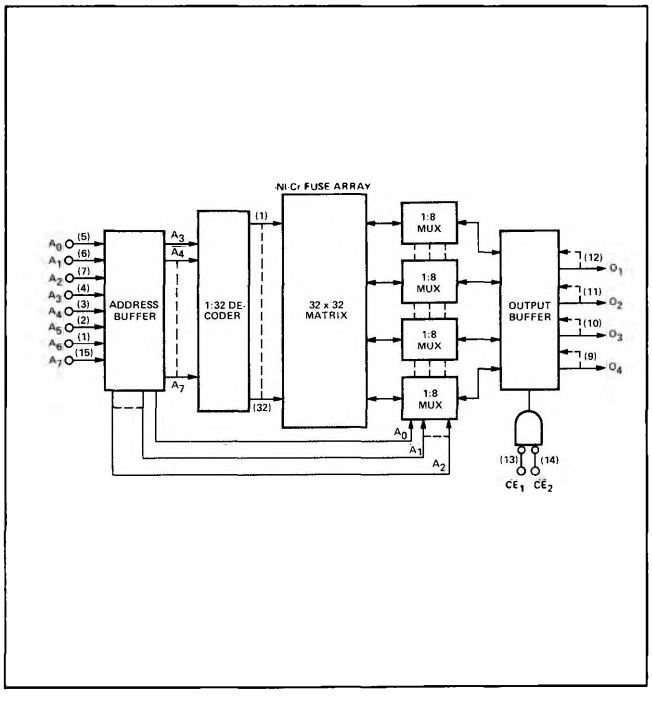
APPLICATIONS

PROTOTYPING/VOLUME PRODUCTION
SEQUENTIAL CONTROLLERS
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE
RANDOM LOGIC
CODE CONVERSION

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S126)	+5.5	Vdc
V_O	Off-State Output Voltage (82S129)	+5.5	Vdc
T_A	Operating Temperature Range		
	(N82S126/129)	0° to +75°	°C
	(S82S126/129)	−55° to +125°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

S82S126/S82S129 $-55°C \leqslant T_A \leqslant +125°C$, $4.5V \leqslant V_{CC} \leqslant 5.5V$
N82S126/N82S129 $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

PARAMETER		TEST CONDITIONS[1]	S82S126/129			N82S126/129			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{OL}	"0" Output Voltage	I_{OUT} = 16mA			0.5			0.5	V
I_{OLK}	Output Leakage Current (82S126)	$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V_{OUT} = 5.5V			60			40	μA
$I_{O(OFF)}$	Hi-Z State Output Current (82S129)	$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V_{OUT} = 5.5V			60			40	μA
		$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V_{OUT} = 0.5V			−60			−40	μA
V_{OH}	"1" Output Voltage (82S129)	$\overline{CE}_1$ = $\overline{CE}_2$ = "0", I_{OUT} = −2.0mA, "1" STORED	2.4			2.4			V
C_{IN}	Input Capacitance	V_{IN} = 2.0V, V_{CC} = 5.0V		5			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, V_{CC} = 5.0V		8			8		pF
I_{IL}	"0" Input Current	V_{IN} = 0.45V			−150			−100	μA
I_{IH}	"1" Input Current	V_{IN} = 5.5V			50			40	μA
V_{IL}	"0" Level Input Voltage				.80			.85	V
V_{IH}	"1" Level Input Voltage		2.0			2.0			V
I_{CC}	V_{CC} Supply Current			105	125		105	120	mA
V_{IC}	Input Clamp Voltage	I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	V
I_{OS}	Output Short Circuit Current (82S129)	V_{OUT} = 0V	−15		−85	−20		−70	mA

SWITCHING CHARACTERISTICS

S82S126/129 $-55°C \leqslant T_A \leqslant +125°C$, $4.5V \leqslant V_{CC} \leqslant 5.5V$
N82S126/129 $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

PARAMETER		TEST CONDITIONS	S82S126/129			N82S126/129			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
	Propagation Delay								
T_{AA}	Address to Output	C_L = 30pF, R_1 = 270Ω, R_2 = 600Ω		35	70		35	50	ns
T_{CD}	Chip Disable to Output			15	35		15	20	ns
T_{CE}	Chip Enable to Output			15	35		15	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

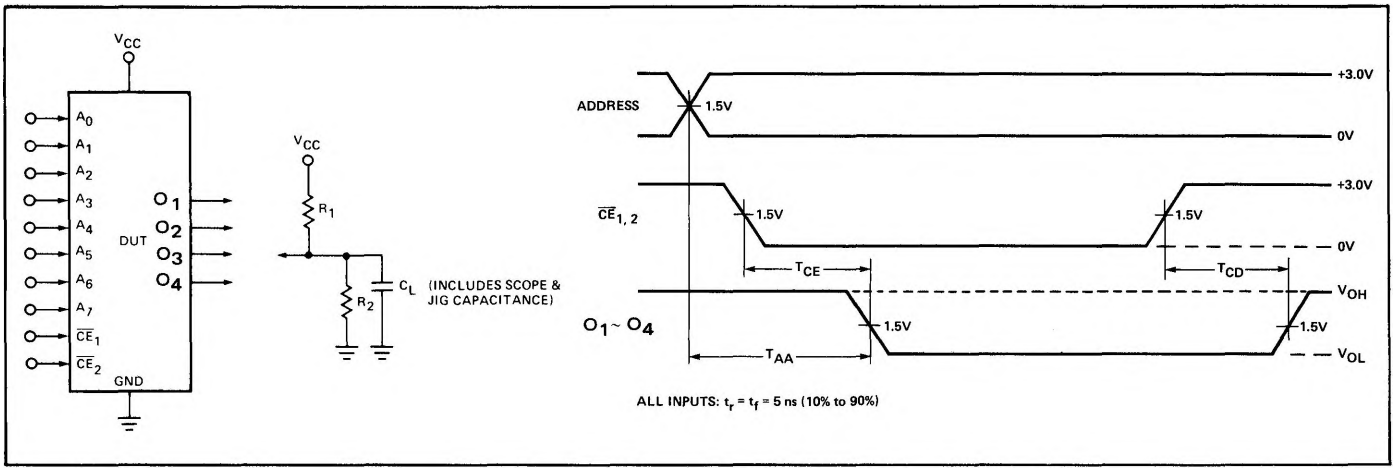
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	I_{CCP} = 350 ± 50mA (Transient or steady state)	8.5	8.75	9.0	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	V_{CCP} = +8.75 ± .25V	300	350	400	mA
Input Voltage						
V_{IH}	Logical "1"		2.4		5.5	V
V_{IL}	Logical "0"		0	0.4	0.8	V
Input Current						
I_{IH}	Logical "1"	V_{IH} = +5.5V			50	μA
I_{IL}	Logical "0"	V_{IL} = +0.4V			-500	μA
V_{OUT}[2]	Output Programming Voltage	I_{OUT} = 200 ± 20mA (Transient or steady state)	16.0	17.0	18.0	V
I_{OUT}	Output Programming Current	V_{OUT} = +17 ± 1V	180	200	220	mA
T_R	Output Pulse Rise Time		10		50	μs
t_P	$\overline{CE}$ Programming Pulse Width		1		2	ms
t_D	Pulse Sequence Delay		10			μs
T_{PR}	Programming Time	$V_{CC} = V_{CCP}$			2.5	sec
T_{PS}	Programming Pause	V_{CC} = 0V	5			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming Duty Cycle				33	%

PROGRAMMING PROCEDURE

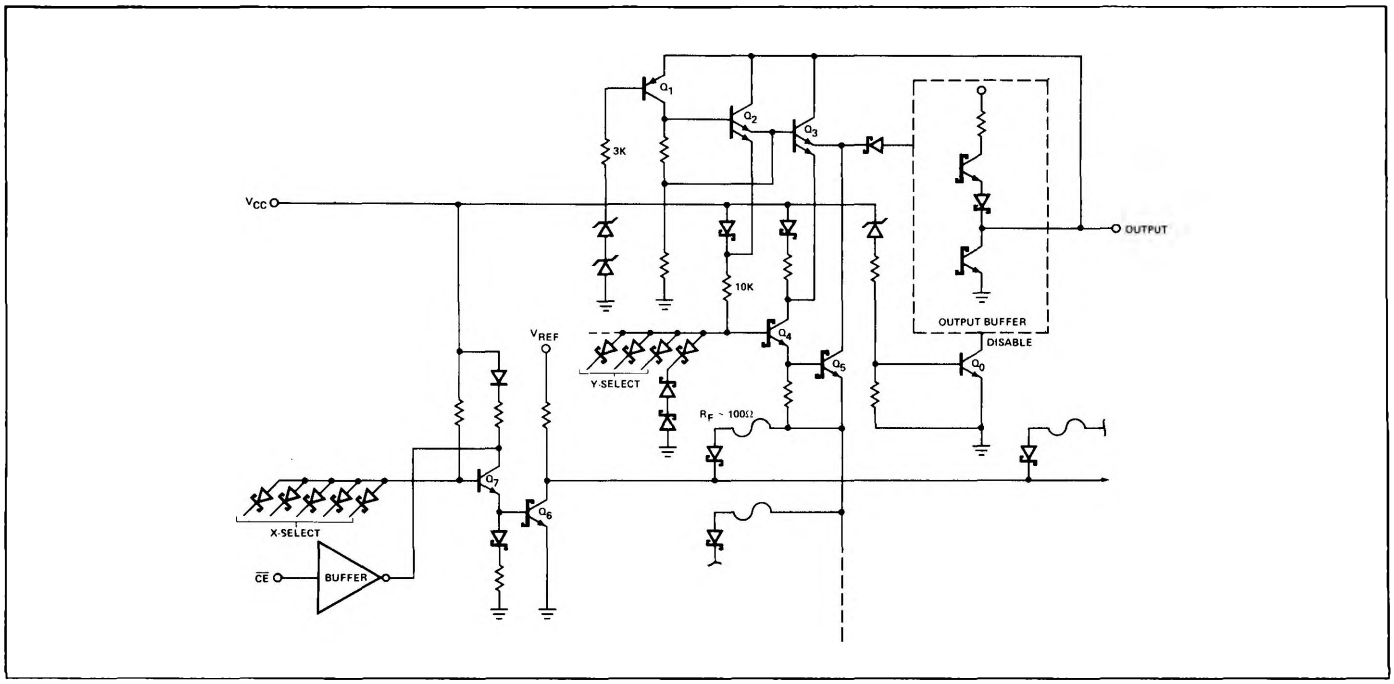
1. Terminate all device outputs with a 10KΩ resistor to V_{CC}.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP} = 8.75 ± .25V.
3. After 10μs delay, apply V_{OUT} = +17 ± 1V to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse both $\overline{CE}$ inputs to logic "0" for 1 to 2 ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to V_{CCH} = +5.5 ± .2V, and apply a logic "0" level to both $\overline{CE}$ inputs. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the "1" state.
7. Raise V_{CC} to V_{CCP} = 8.75 ± .25V, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

NOTES:
1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period (V_{CC} = 0V) of 4ms.

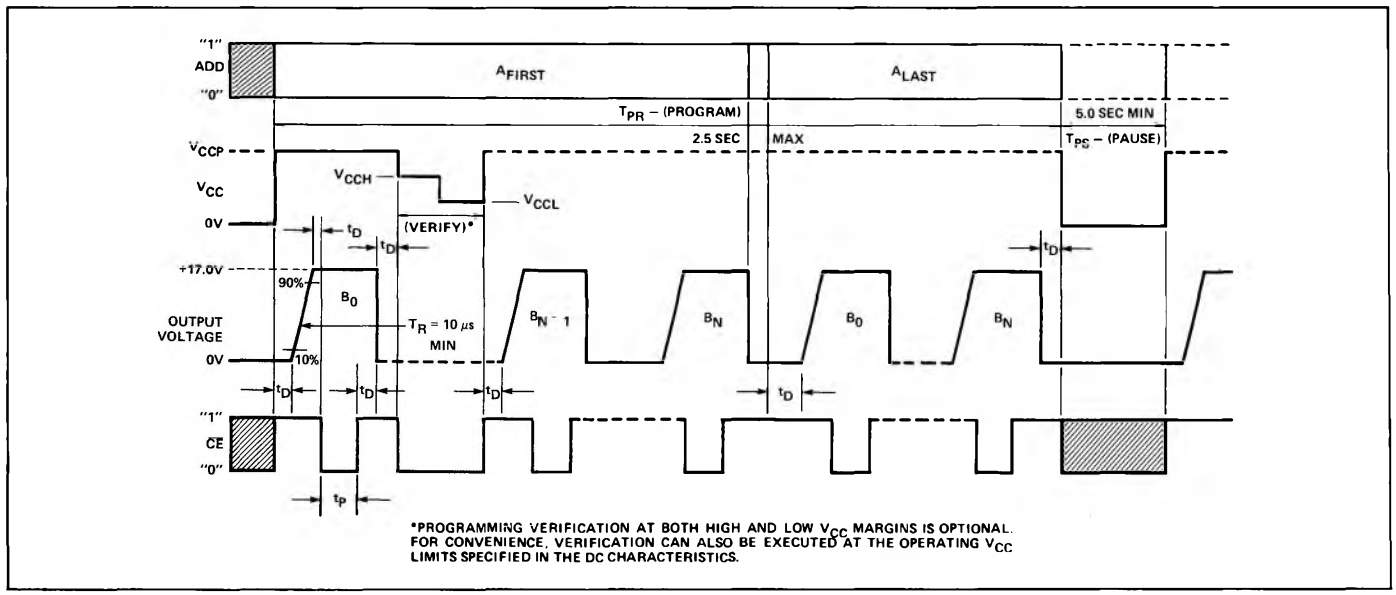
AC TEST FIGURE AND WAVEFORM



TYPICAL FUSING PATH

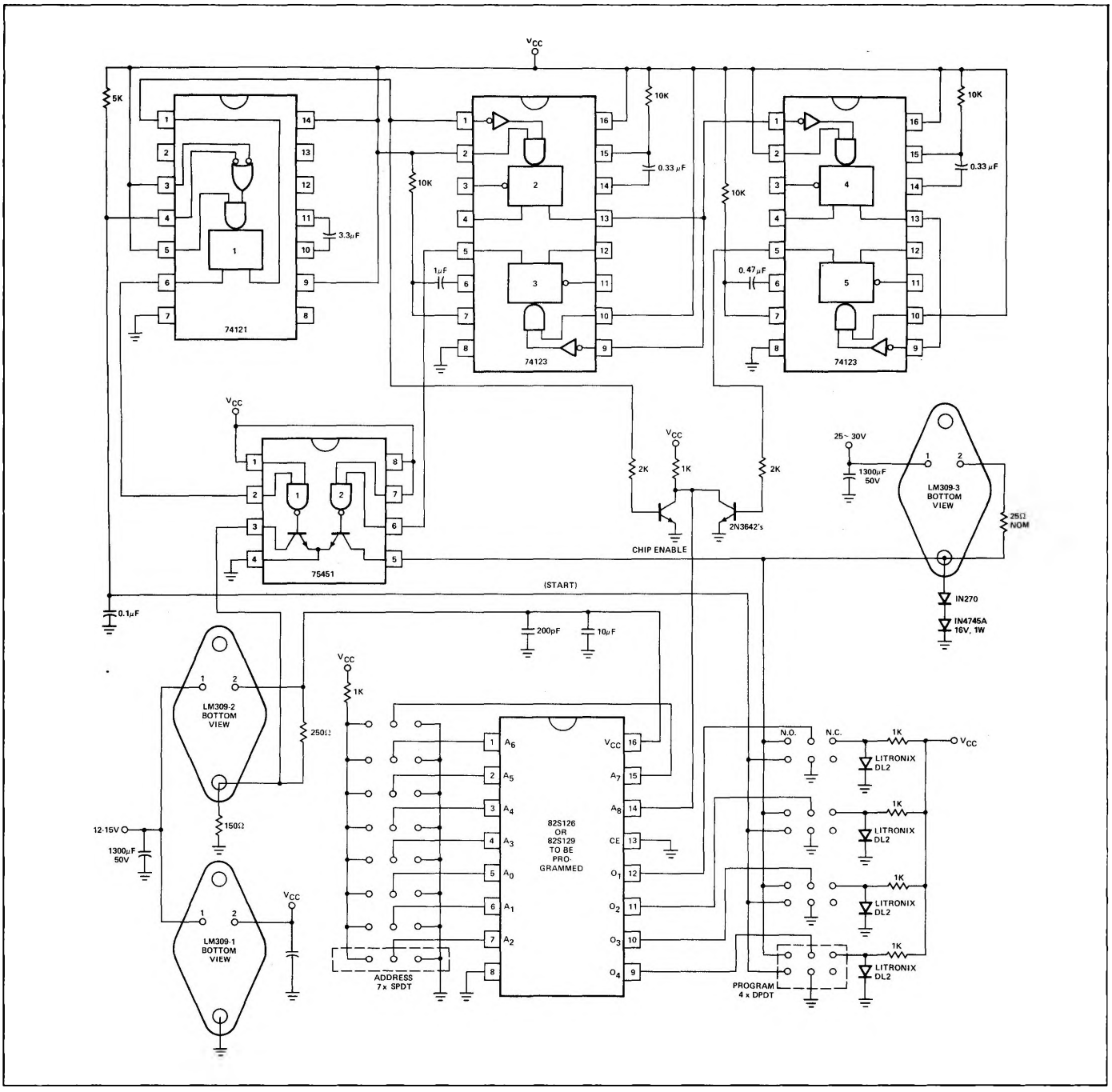


TYPICAL PROGRAMMING SEQUENCE



*PROGRAMMING VERIFICATION AT BOTH HIGH AND LOW V_{CC} MARGINS IS OPTIONAL. FOR CONVENIENCE, VERIFICATION CAN ALSO BE EXECUTED AT THE OPERATING V_{CC} LIMITS SPECIFIED IN THE DC CHARACTERISTICS.

MANUAL PROGRAMMER



TIMING SEQUENCE