DESCRIPTION

The 82S10/11, with a typical access time of 30ns, is ideal for cache buffer applications and for systems requiring very high speed main memory.

The 82S10/11 family requires single +5V power supply and features very low current pnp input structures. They include on-chip decoding and a chip enable input for ease of memory expansion, and feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

All devices are available in the commercial temperature range (0°C to +75°C) and are specified as N82S10/110/11/111. The 82S10 and 82S11 are also available in the military temperature range (-55°C to +125°C) and are specified as S82S10/11.

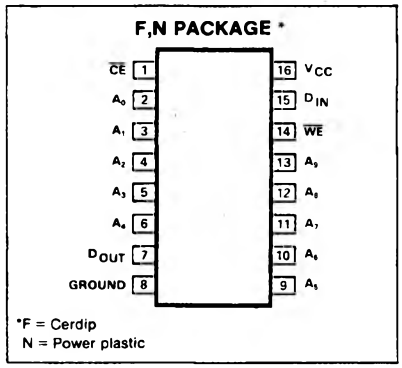
FEATURES

- **Address access time:**
  N82S10/11: 45ns max
  S82S10/11: 70ns max
  N82S110/111: 35ns max
- **Write cycle time:**
  N82S10/11: 45ns max
  S82S10/11: 75ns max
  N82S110/111: 40ns max
- **Power dissipation: 0.5W/bit typ**
- **Input loading:**
  N82S10/11: -250μA max
  S82S10/11: -250μA max
  N82S110/111: -250μA max
- **Output options:**
  82S10/110: Open collector
  82S11/111: Tri-state
- **On-chip address decoding**
- **Non-inverting output**
- **Blanked output during Write**
- **Fully TTL compatible**

APPLICATIONS

- **High speed main frame**
- **Cache memory**
- **Buffer storage**
- **Writable control store**

PIN CONFIGURATION

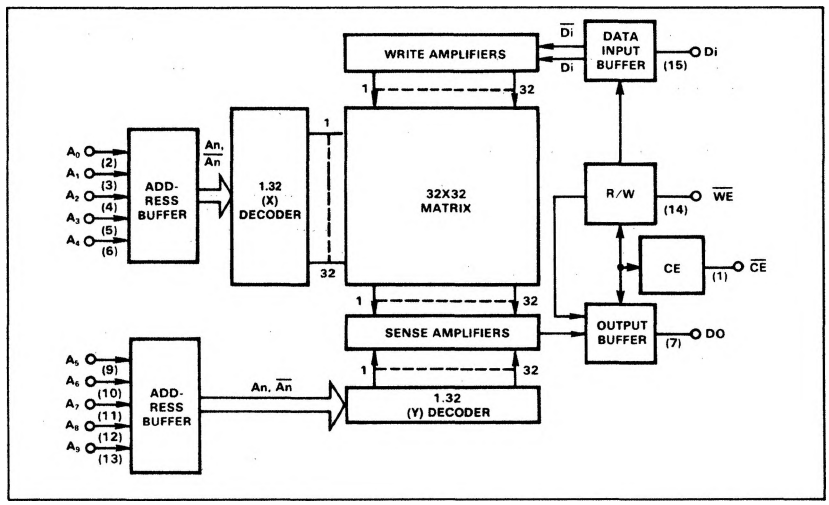


TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D	D_{OUT}	
				82S10/110	82S11/111
Read	0	1	X	Stored data	Stored data
Write "0"	0	0	0	1	High-Z
Write "1"	0	0	1	1	High-Z
Disabled	1	X	X	1	High-Z

X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S10/110)	+5.5	
V_O	Off-state (82S11/111)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S10/11/110/111	0 to +75	
	S82S10/11	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS[2]

N82S10/110/11/111: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S10/11: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITIONS	N82S10/11/110/111			S82S10/11			UNIT
			Min	Typ[3]	Max	Min	Typ[3]	Max	
	Input voltage								V
V_{IL}	Low[1]	V_{CC} = Min			.85			.80	
V_{IH}	High[1]	V_{CC} = Max	2.1			2.1			
V_{IC}	Clamp[1,4]	V_{CC} = Min, I_{IN} = -12mA		-1.0	-1.5		-1.0	-1.5	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[1,5]	I_{OL} = 16mA		0.35	0.45		0.35	0.50	
V_{OH}	High (82S11/111)[1,6]	I_{OH} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		-10	-250		-10	-250	
I_{IH}	High	V_{IN} = 5.5V		1	25		1	40	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage (82S10/110)[7]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S11/111)	V_{OUT} = 5.5V		1	60		1	100	μA
		V_{OUT} = 0.45V[7]		-1	-60		-1	-100	
I_{OS}	Short circuit (82S11/111)[8]	V_{OUT} = 0V	-20		-100	-20		-100	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = Max							mA
		$0 < T_A < 25°C$		120	155		120	155	
		$T_A \geq 25°C$		95	130		95	130	
		$T_A \leq 0°C$			170			170	
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		7			4		
C_{OUT}	Output	V_{OUT} = 2.0V							

AC ELECTRICAL CHARACTERISTICS[2]

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$
N82S10/110/11/111: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S10/11: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

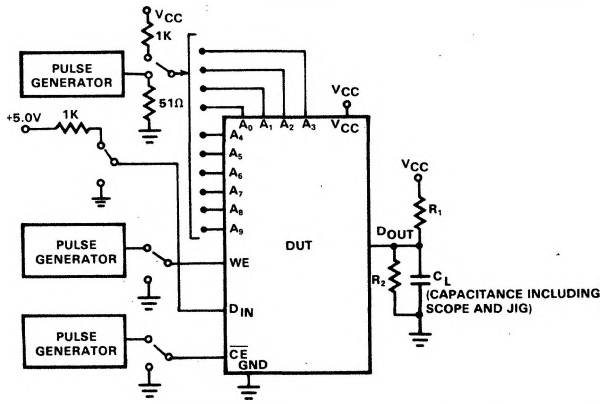
PARAMETER	TO	FROM	N82S10/11			N82S110/111			S82S10/11			UNIT
			Min	Typ[3]	Max	Min	Typ	Max	Min	Typ[3]	Max	
Access time T_{AA} Address T_{CE} Chip enable				 30 15	 45 30			 35 25		 30 15	 70 45	ns
Disable time T_{CD} T_{WD}	 Output Output	 Chip enable Write enable		 15 20	 30 30			 25 25		 15 20	 45 45	ns
T_{WR} Write recovery time				20	30			25		20	45	ns
Setup and hold time T_{WSA} Setup time T_{WHA} Hold time	Write enable	Address	 5 5	 0 0		 5 10			 15 10	 0 0		ns
T_{WSD} Setup time T_{WHD} Hold time	Write enable	Data in	40 5	30 0		30 5			55 5	35 0		
T_{WSC} Setup time T_{WHC} Hold time	Write enable	$\overline{CE}$	5	0		5			5	0		
Pulse width T_{WP} Write enable[10]			35	25		25			50	25		ns

NOTES

1. All voltage values are with respect to network ground terminal.
2. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
   Typical thermal resistance values of the package at maximum temperature are:
   Θ_{JA} junction to ambient at 400fpm air flow - 50°C/watt
   Θ_{JA} junction to ambient - still air - 90°C/watt
   Θ_{JA} junction to case - 20°C/watt
3. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
4. Test each input one at a time.
5. Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
7. Measured with V_{IH} applied to $\overline{CE}$.
8. Duration of the short circuit should not exceed 1 second.
9. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
10. Minimum required to guarantee a Write into the slowest bit.

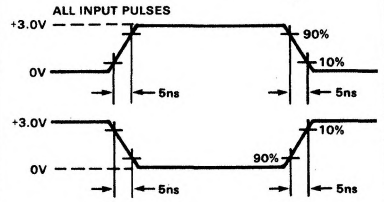
TEST LOAD CIRCUIT

LOADING CONDITION



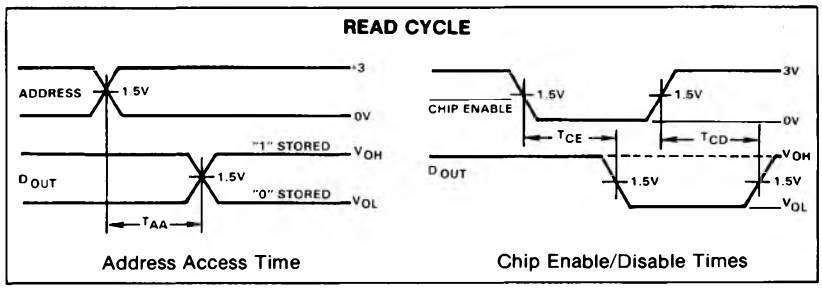
VOLTAGE WAVEFORM

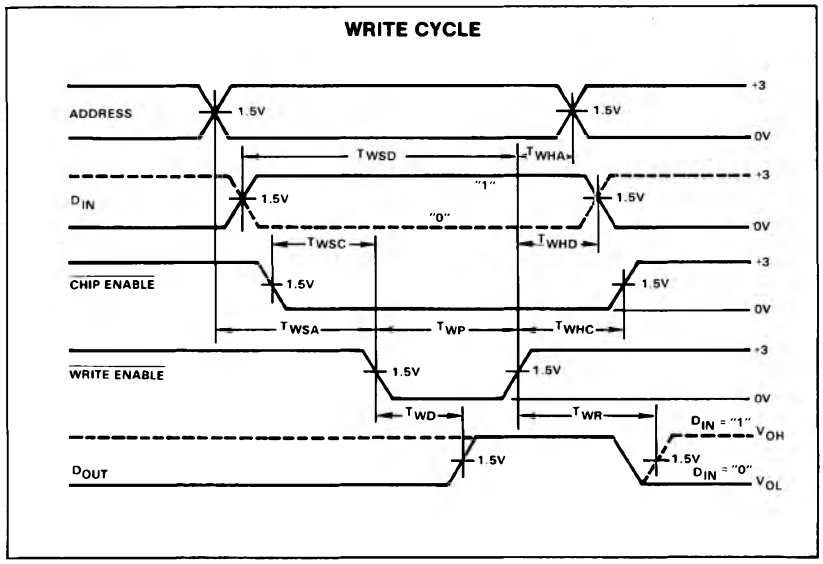
INPUT PULSES



Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

TIMING DIAGRAMS





MEMORY TIMING DEFINITIONS

T_{WR}	Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming Address still valid—not as shown.)
T_{CE}	Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes high and Data Output is in off state.
T_{AA}	Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
T_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output is in off state.
T_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.