

DIVIDE-BY-TWELVE COUNTER/STORAGE ELEMENT

8288

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8288 Divide by Twelve Counter is a four-bit subsystem consisting of divide by two and divide by six counters in a 14 pin package. For Divide-by-Twelve operation, output A is connected externally to the clock 2 input.

The 8288 has strobed paralleled data entry capability so that the counter may be preset to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at a "0" level. For additional flexibility, the 8288 is provided with a common reset. A "0" on the reset line produces "0" at all four outputs.

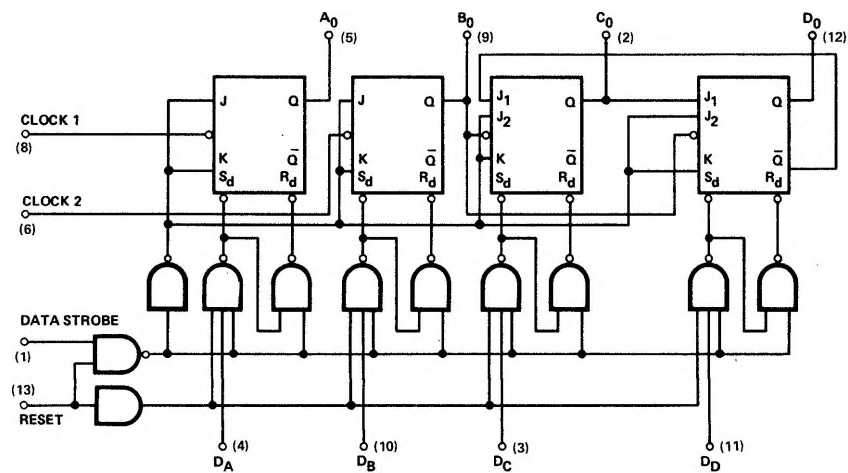
The counting operation is performed on the falling (negative going) edge of the input clock pulse, however, there is no restriction on transition time since the individual binaries are level sensitive. The data strobe and reset functions are asynchronous with respect to the clock. The 8288 is compatible with all Signetics 8000 series elements.

TRUTH TABLE*

OUTPUT				
Count	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1

*Connected for Divide-by-Twelve operation (output A connected to CP2)

LOGIC DIAGRAM



V_{CC} = (14) A, F PACKAGES
GND = (7)
() = Denotes Pin Numbers

SIGNETICS DIGITAL 8000 SERIES TTL/MSI – 8288
ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
"1" Output Voltage	2.6	3.5		V	0.8V	2.0V	2.0V				6, 7
"0" Output Voltage			0.4V	V	0.8V	0.8V	0.8V				6, 8
"0" Input Current											
Data Strobe	-0.1		-1.6	mA	0.4V		5.25V				
Data Inputs	-0.1		-1.2	mA		0.4V					
Reset	-0.1		-3.2	mA	5.25V		0.4V				
Clock 1	-0.1		-3.2	mA				0.4V			
Clock 2	-0.1		-1.6	mA					0.4V		
"1" Input Current											
Data Strobe			40	μA	4.5V		0V				
Data Input			40	μA		4.5V					
Reset			80	μA			4.5V				
Clock 1			80	μA				4.5V			
Clock 2			80	μA					4.5V		
Power/Current Consumption		184/35	236/45	mW/mA			0V	0V	0V		11
Input Voltage Rating											
Data Strobe	5.5			V	10mA						
Data Inputs	5.5			V		10mA					
Reset	5.5			V			10mA				
Output Short Circuit Current	-10		-60	mA	0V					0V	

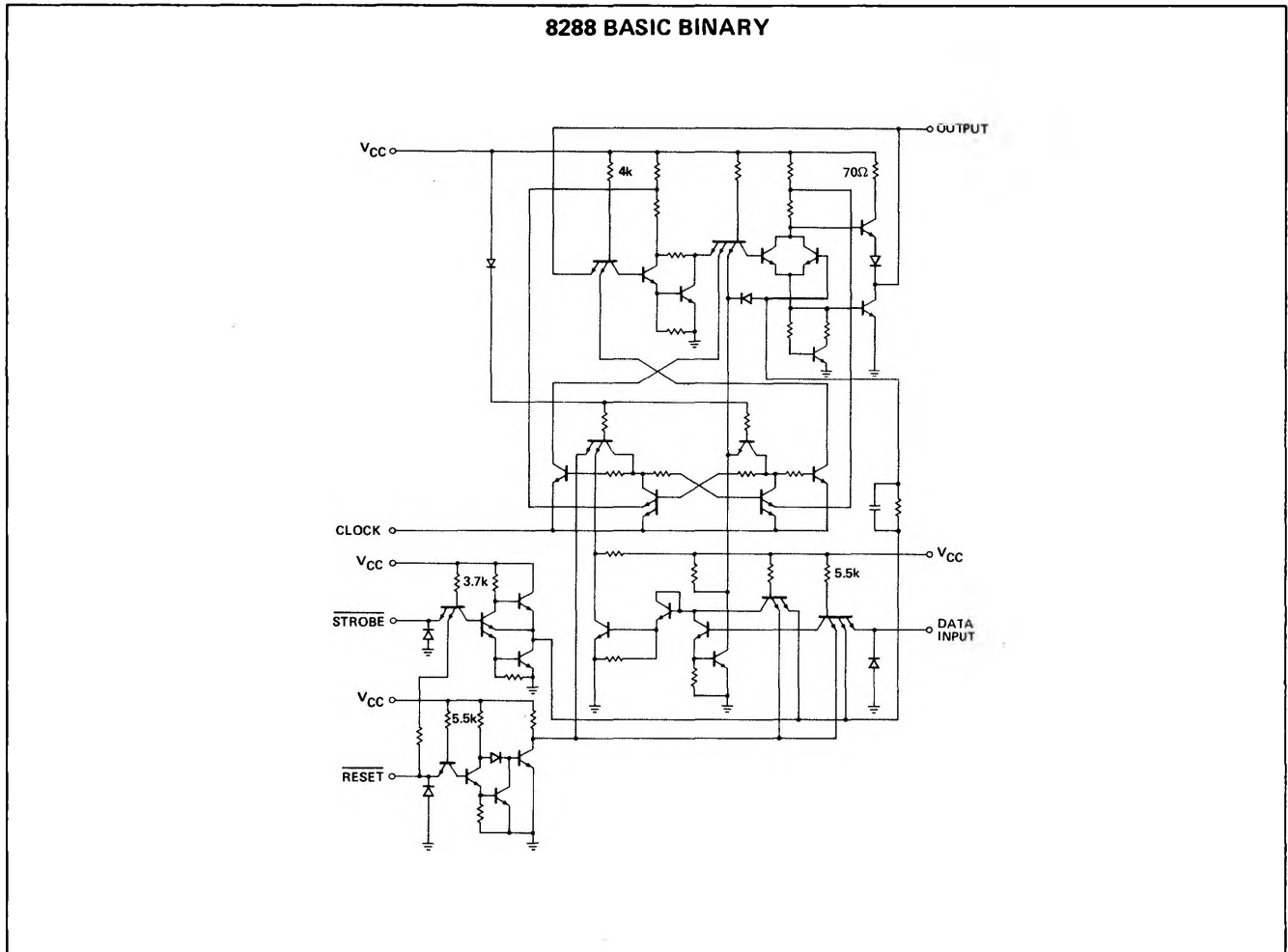
 $T_A = 25^\circ\text{C}$ and $V_{CC} = 5.0\text{V}$

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
Clock Mode t_{ON} Delay		15	25	ns							9
Bit A, B, C, D											
Clock Mode t_{OFF} Delay		15	25	ns							9
Bit A, B, C, D											
Data/Strobe t_{ON} Delay		20	35	ns							9
Bit A, B, C, D											
Data/Strobe t_{OFF} Delay		25	40	ns							9
Bit A, B, C, D											
Toggle Rate	20	25		MHz							9
Strobe Hold Time		25	35	ns		0.8V	2.0V	2.0V	Output A		
Reset Hold Time		20	35	ns	2.0V	0.8V		2.0V	Output A		
Strobe Release Time		30	40	ns							
Reset Release Time		50	75	ns							

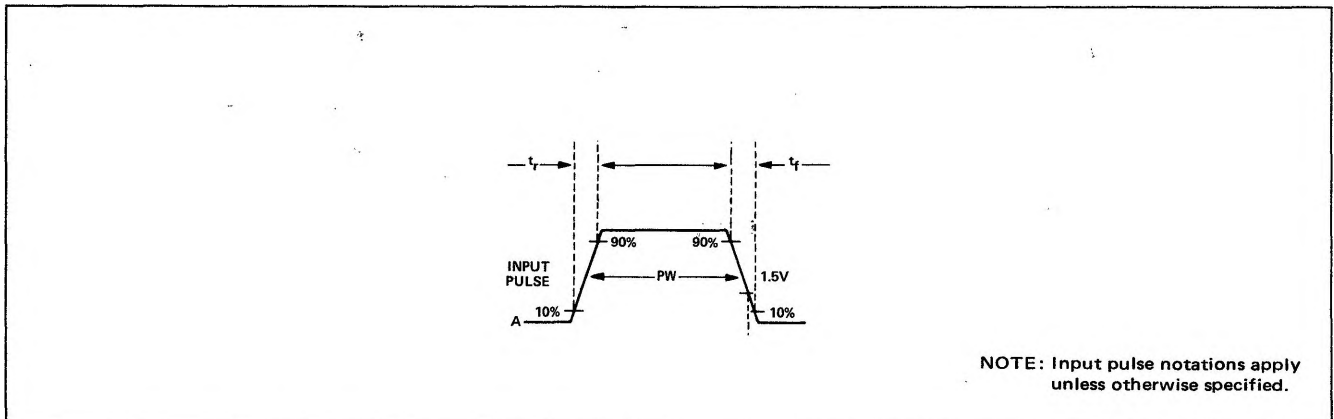
NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition:
"UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each output and the associated data input independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC} .
9. Refer to AC Test Figures.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. $V_{CC} = 5.25$ volts.

SCHEMATIC DIAGRAM

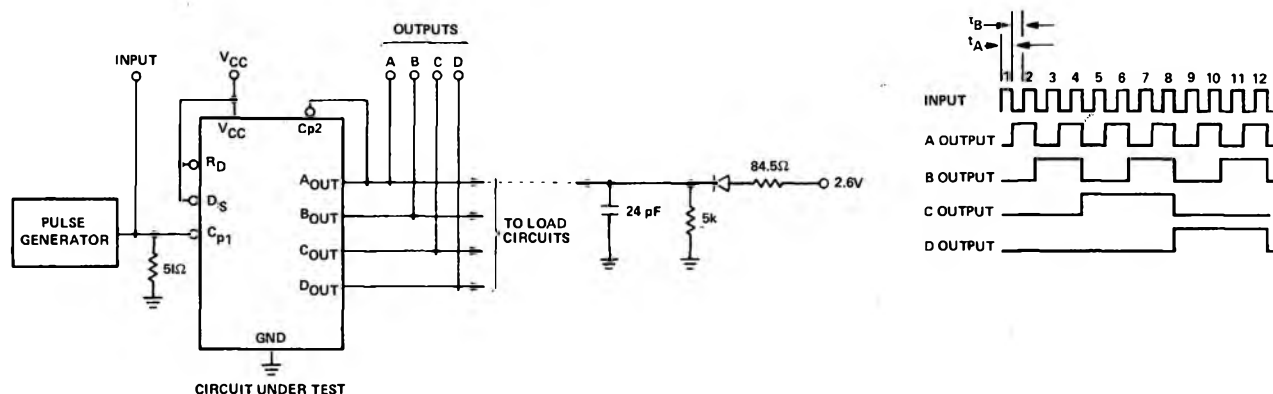


AC TEST FIGURES AND WAVEFORMS



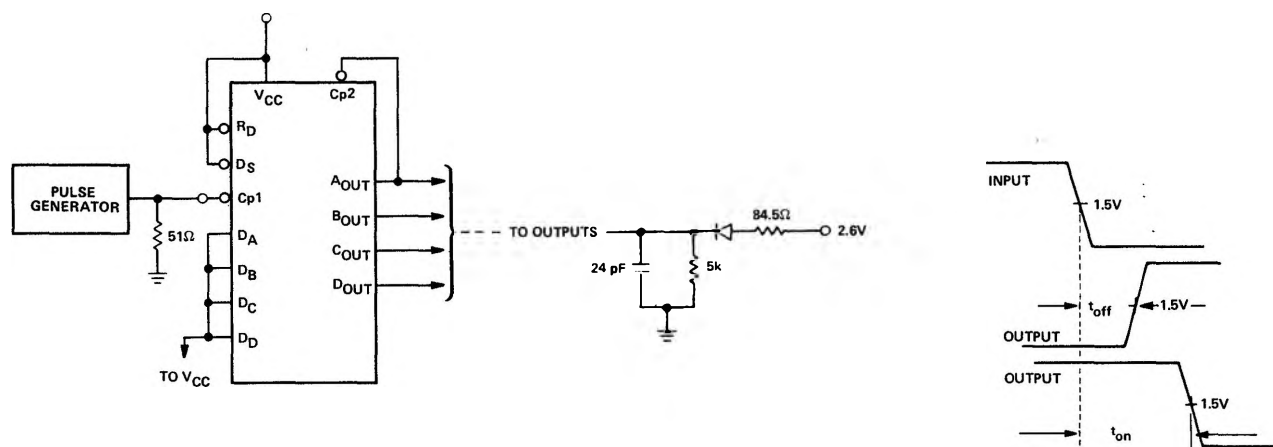
AC TEST FIGURES AND WAVEFORMS (Cont'd)

TOGGLE RATE



INPUT PULSE:
Amplitude = 3.4V
 $t_A = 100\text{ns}$
 $t_r = 20\text{ns}$
 $t_B = 300\text{ns}$

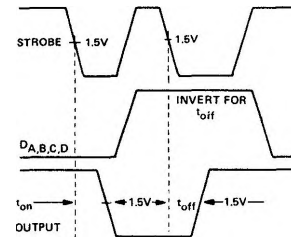
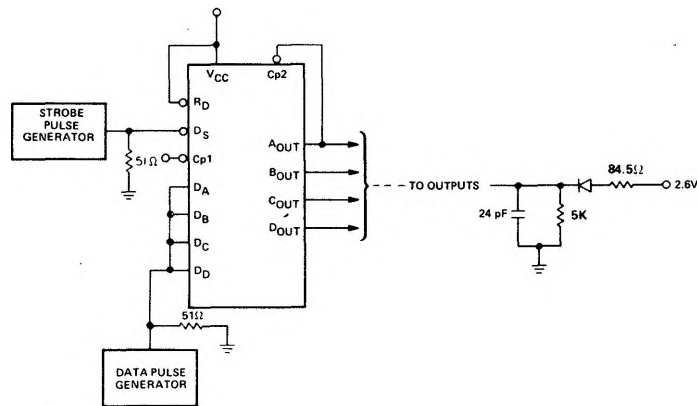
CLOCK MODE t_{on}/t_{off} DELAY



1. t_{on} and t_{off} are measured from the clock input of each binary to the Q output of that binary.
2. Each Q output will be loaded with the following load circuit:

INPUT PULSE:
Amplitude = 2.6V
P.W. = 30ns
 $t_r = t_f = 5\text{ns}$

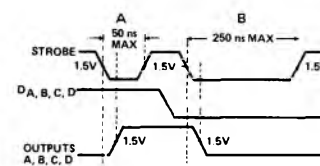
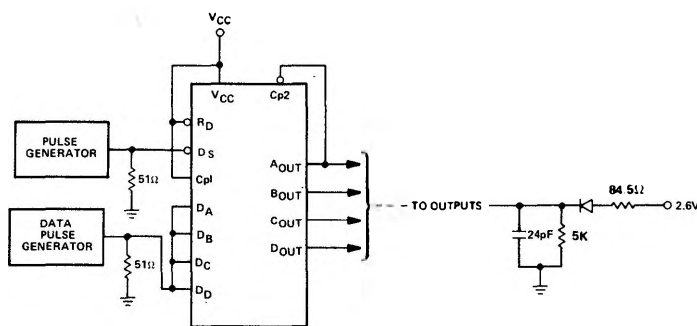
AC TEST FIGURES AND WAVEFORMS (Cont'd)

DATA/STROBE t_{on} t_{off} 

NOTES:

1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent.
 $f = 1\text{MHz}$, $V_{ac} = 25\text{mF}_{rms}$
3. All diodes are 1N914.

STROBE HOLD TIME

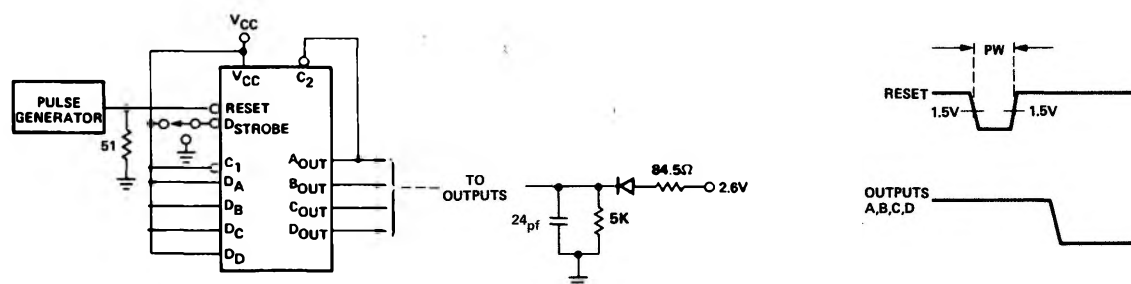


- A With all outputs initially "0", output shall have a "0" to "1" transition.
- B With all outputs initially "1", outputs shall have a "1" to "0" transition.

Amplitude = 2.6V (from Pulse Generator)
 $t_r = t_f = 50\text{ ns}$

AC TEST FIGURES AND WAVEFORMS (Cont'd)

MINIMUM RESET PULSE WIDTH



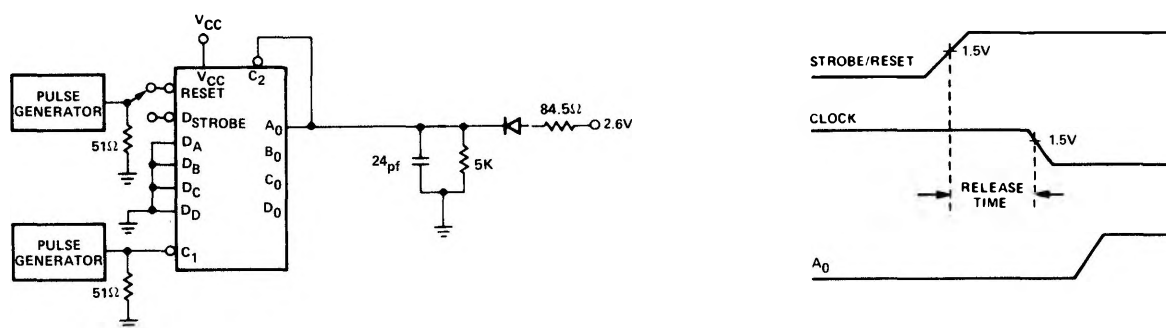
INPUT PULSE:

Amplitude = 2.6V

 $t_r = t_f = 5\text{ns max.}$

Note: Outputs must be previously brought high by placing a "0" on the D strobe input.
A pulse generator may be substituted for the switch.

STROBE/RESET RELEASE TIME



Clock, Strobe/Reset Amplitude = 2.6V
 $t_r = t_f = 5\text{ns max. PRR} = 1\text{MHz 50% Duty Cycle.}$

NOTES:

1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. $f = 1\text{MHz}$, $V_{ac} = 25\text{mV}_{rms}$.
3. All diodes are 1N916.