4-BIT COMPARATOR
8269

REFER TO PAGE 16 FOR A, F AND $Q$ PACKAGE PIN CONFIGURATIONS.

## DIGITAL 8000 SERIES TTL/MSI

## DESCRIPTION

The 8269, a 4 BIT COMPARATOR, is an array of gates designed to perform the numerical comparison of two four-bit binary numbers. The outputs indicate whether the two numbers are equal in value, or which number is the greater. The 8269 is a functional and pin-for-pin replacement for the DM8200.

TRUTH TABLE

| INPUT |  |  |  | OUTPUT |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $A_{n}$ |  | $B_{n}$ | STROBE | X | Y |
| A | $>$ | B | 0 | 1 | 0 |
| A | $<$ | B | 0 | 0 | 1 |
| A | $=$ | B | 0 | 1 | 1 |
| A | $\$$ | B | 1 | 0 | 0 |

LOGIC DIAGRAM


ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

| CHARACTERISTICS | LIMITS |  |  |  | TEST CONDITIONS |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN. | TYP. | MAX. | UNITS |  |
| "1" Output Voltage <br> "0" Output Voltage <br> "1" Input Current <br> "0" Input Current <br> Power Consumption <br> Short Circuit Output Current | 2.6 <br> $-0.1$ <br> - 18 | $\begin{aligned} & 3.5 \\ & 0.2 \end{aligned}$ | $\begin{gathered} 0.4 \\ 80 \\ -3.2 \\ 278 / 53 \\ -55 \end{gathered}$ | $\begin{gathered} V \\ V \\ \mu A \\ m A \\ m W / m A \\ m A \end{gathered}$ | $\begin{aligned} & \mathrm{I}_{\text {out }}=800 \mu \mathrm{~A} \\ & \mathrm{I}_{\text {out }}=16 \mathrm{~mA} \\ & \mathrm{~V}_{\text {in }}=4.5 \mathrm{~V} \\ & \mathrm{~V}_{\text {in }}=0.4 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=5.25 \mathrm{~V} \\ & \mathrm{~V}_{\text {out }}=0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=5.25 \mathrm{~V} \end{aligned}$ |

$\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{C}}=5.0 \mathrm{~V}$

| CHARACTERISTICS | LIMITS |  |  |  | TEST CONDITIONS |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN. | TYP. | MAX. | UNITS |  |
| Propagation Delay <br> tpd1 (Data Input to Output) tpdO (Data Input to Output) tpd1 (Strobe to Output) tpdO (Strobe to Output) |  |  | $\begin{aligned} & 40 \\ & 30 \\ & 27 \\ & 18 \end{aligned}$ | ns ns ns ns | Test Figure 1 <br> Test Figure 1 <br> Test Figure 2 <br> Test Figure 2 |

## NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal.
Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP"Level = "1","DOWN" Level = " 0 ".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to $\mathrm{V}_{\mathrm{CC}}$.
8. Manufacturer reserves the right to make design and process changes and improvements.

## AC TEST FIGURE AND WAVEFORMS



FIGURE 1


FIGURE 2

