## 2-INPUT 4-BIT DIGITAL MULTIPLEXER

## DIGITAL 8000 SERIES TTL/MSI

capability is especially useful for transferring data into parallel adders where both true data for adding or multiplying and also complemented data for subtracting or dividing are needed.

The 8234 and 8235 designs have open collector outputs which permit direct wiring to other open collector outputs (collector logic) to yield "free" four-bit words. As many as one hundred four-bit words can be multiplexed by using fifty 8234/8235s in the WIRED-AND mode.
The inhibit state $S_{0}=S_{1}=1$ can be used to facilitate transfer operations in an arithmetic section.

## DESCRIPTION

These devices are 2-input, 4-Bit Digital Multiplexers designed for general purpose data-selection applications.

The 8233 features non-inverting data paths; and, the 8234 features inverting data paths.

The 8235 is designed for input to adders, registers and general paralleled data handling due to its capability to perform CONDITIONAL COMPLEMENTING (TRUE/ COMPLEMENT). When the two inputs for each bit position ( $\mathrm{Ai}, \mathrm{Bi}$ ) are connected together, the of output will provide either the True or Complement of the input data. This

## LOGIC DIAGRAM AND TRUTH TABLES



| $S_{0}$ | $S_{1}$ | $f_{n}$ |
| :---: | :---: | :---: |
| 0 | 0 | $B$ |
| 1 | 0 | $A$ |
| 0 | 1 | $B$ |
| 1 | 1 | 0 |

```
VCC}=(16
GND = (8)
( ) = Denotes Pin Numbers
```

8234


| $\mathrm{S}_{\mathbf{0}}$ | $\mathrm{S}_{\mathbf{1}}$ | $\mathrm{f}_{\mathrm{n}}$ |
| :---: | :---: | :---: |
| 0 | $\mathbf{0}$ | $\overline{\mathrm{~B}}$ |
| 1 | 0 | $\bar{A}$ |
| $\mathbf{0}$ | 1 | $\overline{\mathrm{~B}}$ |
| 1 | 1 | 1 |

$$
\begin{aligned}
V_{C C} & =(16) \\
\text { GND } & =(8) \\
(\quad) & =\text { Denotes Pin Numbers }
\end{aligned}
$$

8235


| $\mathrm{S}_{0}$ | $\mathrm{~S}_{\mathbf{1}}$ | $\mathrm{f}_{\mathrm{n}}$ |
| :---: | :---: | :---: |
| 0 | $\mathbf{0}$ | $\overline{A_{n}} \mathrm{~B}_{\mathrm{n}}$ |
| 0 | 1 | $\mathrm{~B}_{\mathrm{n}}$ |
| 1 | 0 | $\overline{A_{n}}$ |
| 1 | 1 | 1 |

$v_{C C}=(16)$
GND $=(8)$
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

$\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$

| CHARACTERISTICS | LIMITS |  |  |  | TEST CONDITIONS |  |  |  | OUTPUTS | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | INPUTS |  |  |  |  |  |
|  | MIN. | TYP. | MAX. | UNITS | $A_{n}$ | $B_{n}$ | $s_{0}$ | $S_{1}$ |  |  |
| Power/Current |  |  |  |  |  |  |  |  |  |  |
| Consumption: |  |  |  |  |  |  |  |  |  |  |
| 8233 |  | 200/38 | 252/48 | $\mathrm{mW} / \mathrm{mA}$ |  | OV |  | OV |  | 15 |
| 8234 |  | 160/31 | 210/40 | $\mathrm{mW} / \mathrm{mA}$ |  | OV |  | OV |  | 15 |
| 8235 |  | 230/44 | 310/59 | $\mathrm{mW} / \mathrm{mA}$ |  | 4.5 V |  | 4.5 V |  | 15 |
| 8233 Turn-On Times |  |  |  |  |  |  |  |  |  |  |
| $A_{n}, B_{n}$ to $f_{n}$ |  | 16 | 25 | ns |  |  |  |  |  | 8,14 |
| $S_{0}$ to $f_{n}$ |  | 27 | 38 | ns |  |  |  |  |  | 8,14 |
| $S_{1}$ to $f_{n}$ |  | 27 | 38 | ns |  |  |  |  |  | 8.14 |
| 8233 Turn-Off Times |  |  |  |  |  |  |  |  |  |  |
| $A_{n}, B_{n}$ to $f_{n}$ |  | 16 | 25 | ns |  |  |  |  |  | 8,14 |
| $S_{0}$ to $f_{n}$ |  | 27 | 38 | ns |  |  |  |  |  | 8,14 |
| $S_{1}$ to $f_{n}$ |  | 27 | 38 | ns |  |  |  |  |  | 8,14 |
| 8234 Turn-On Times |  |  |  |  |  |  |  |  |  |  |
| $A_{n}, B_{n}$ to $f_{n}$ |  | 16 | 25 | ns |  |  |  |  |  | 8,14 |
| $S_{0}$ to $f_{n}$ |  | 27 | 38 | ns |  |  |  |  |  | 8,14 |
| $S_{1}$ to $f_{n}$ |  | 27 | 38 | ns |  |  |  |  |  | 8,14 |
| 8234 Turn-Off Times |  |  |  |  |  |  |  |  |  |  |
| $A_{n}, B_{n}$ to $f_{n}$ |  | 16 | 25 | ns |  |  |  |  |  | 8,14 |
| $S_{0}$ to $f_{n}$ |  | 27 | 38 | ns |  |  |  |  |  | 8,14 |
| $S_{1}$ to $f_{n}$ |  | 27 | 38 | ns |  |  |  |  |  | 8,14 |
| 8235 Turn-On Times |  |  |  |  |  |  |  |  |  |  |
| $A_{n}$ to $f_{n}$ |  | 16 | 25 | ns |  |  |  |  |  | 8,14 |
| $B_{n}$ to $f_{n}$ |  | 24 | 35 | ns | 「 |  |  |  |  | 8,14 |
| $S_{0}$ to $f_{n}$ |  | 27 | 38 | ns | , |  |  |  |  | 8,14 |
| $S_{1}$ to $f_{n}$ |  | 27 | 38 | ns |  |  |  |  |  | 8,14 |
| 8235 Turn-Off Times |  |  |  |  |  |  |  |  |  |  |
| $A_{n}$ to $f_{n}$ |  | 16 | 25 | ns |  |  |  |  |  | 8,14 |
| $B_{n}$ to $f_{n}$ |  | 24 | 35 | ns |  |  |  |  |  | 8,14 |
| $S_{0}$ to $f_{n}$ |  | 27 | 38 | ns |  |  |  |  |  | 8,14 |
| $S_{1}$ to $f_{n}$ |  | 27 | 38 | ns |  |  |  |  |  | 8,14 |

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to $\mathrm{V}_{\mathrm{CC}}$.
8. One DC fan-out is defined as 0.8 mA
9. One AC fan-out is defined as 50 pF .
10. Manufacturer reserves the right to make design and process changes and improvements.
11. This test guarantees operation free of input latch-up within the specified operating supply voltage range.
12. Measurements apply to each gate element independently.
13. Connect an external $1 \mathrm{k} \pm 1 \%$ resistor from $\mathrm{V}_{\mathrm{CC}}$ to the output for this test.
14. Reference AC Test Circuit, Waveforms and Test Tables.
15. $V_{C C}=5.25 \mathrm{~V}$.

## SCHEMATIC DIAGRAMS



SCHEMATIC DIAGRAMS (Cont'd)


PROPAGATION DELAY TEST TABLE

| PRODUCT | PATH | PARAMETER | $\mathrm{S}_{1}$ | $\mathrm{S}_{2}$ | $\mathrm{S}_{3}$ | $\mathrm{S}_{4}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ALL | $A_{0}$ to $f_{0}$ | $\frac{t_{\text {on }}}{t_{\text {off }}}$ | a | b | b | c |
| $\begin{aligned} & 8233 \\ & 8234 \end{aligned}$ | $B_{0}$ to fo | $\frac{t_{\text {on }}}{t_{\text {off }}}$ | c | a | C | b |
| $\begin{aligned} & 8233 \\ & 8234 \end{aligned}$ | $\mathrm{S}_{0}$ to $\mathrm{f}_{0}$ | $\frac{t_{\mathrm{on}}}{t_{\mathrm{off}}}$ | b | b | a | b |
| $\begin{aligned} & 8233 \\ & 8234 \end{aligned}$ | $\mathrm{S}_{0}$ to $\mathrm{f}_{0}$ | $\frac{t_{\text {on }}}{t_{\text {off }}}$ | b | c | a | c |
| 8235 | $\mathrm{B}_{0}$ to fo | $\frac{t_{\text {on }}}{t_{\text {off }}}$ | c | a | c | b |
| 8235 | Bo to fo | $\frac{t_{\text {on }}}{t_{\text {off }}}$ | b | c | a | b |
| 8235 | $\mathrm{S}_{1}$ to $\mathrm{f}_{0}$ | $\frac{t_{\text {on }}}{t_{\text {off }}}$ | b | b | C | a |
| $\begin{aligned} & 8233 \\ & 8234 \end{aligned}$ | $S_{1}$ to $f_{0}$ | $\frac{t_{\mathrm{on}}}{t_{\mathrm{off}}}$ | b | c | b | a |

## AC TEST FIGURE AND WAVEFORMS



PULSE REQUIREMENTS


